

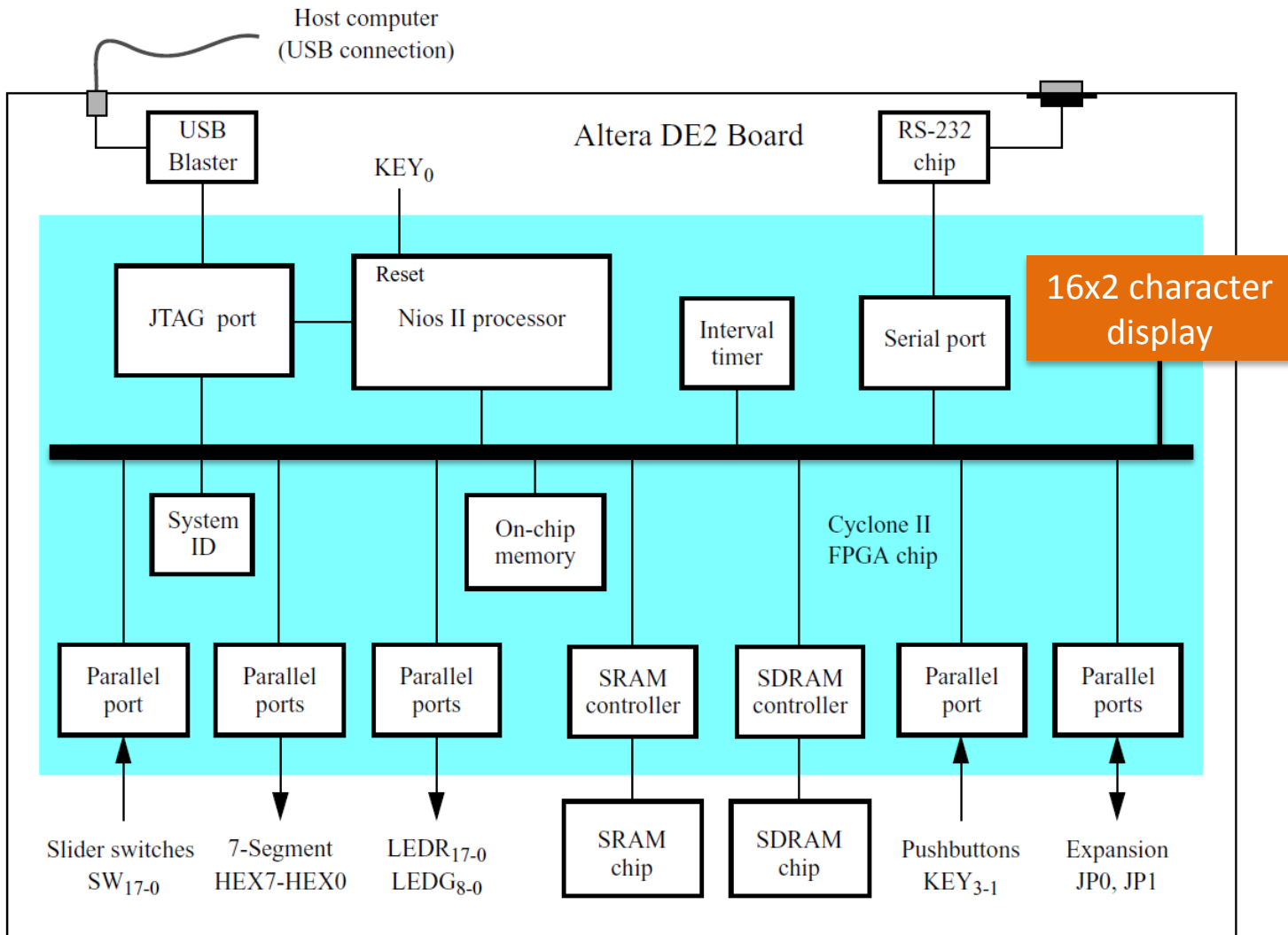
# SISTEMI EMBEDDED

## AA 2013/2013

Manipulating an existing  
Nios II processor

# Guided example (1a)

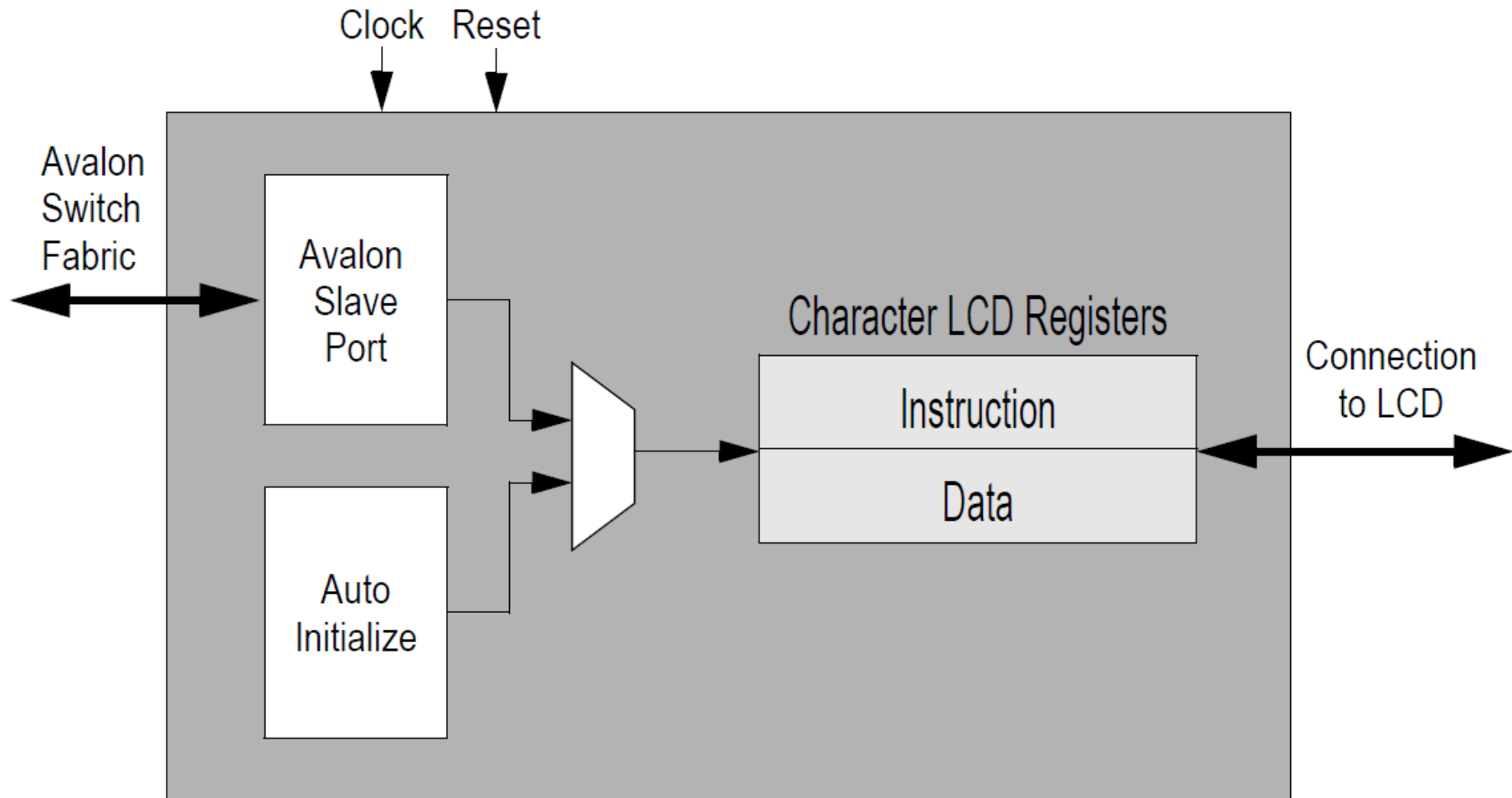
- Expanding the DE2 Basic Computer adding the **16x2 Character Display** peripheral



# Guided example (1b)

- Expanding the DE2 Basic Computer adding the **16x2 Character Display** peripheral

## Architecture of the 16x2 character display peripheral



# Guided example (1c)

- Expanding the DE2 Basic Computer adding the **16x2 Character Display** peripheral

Port declaration of  
the 16x2 character  
LCD module

```
module character_lcd_0 (
```

```
// Inputs
```

```
clk,  
reset,  
address,  
chipselct,  
read,  
write,  
writedata,
```

```
// Bidirectionals
```

```
LCD_DATA,
```

```
// Outputs
```

```
LCD_ON,  
LCD_BLON,  
LCD_EN,  
LCD_RS,  
LCD_RW,
```

```
readdata,  
waitrequest
```

```
);
```

# Guided example (2)

- Expanding the DE2 Basic Computer adding the **16x2 Character Display** peripheral
  - Create a new project in Quartus II
  - Launch SoPC Builder
    - Open system\_nios.sopc from DE2\_Basic\_Computer folder and save it in the new project folder
    - Add the 16x2 character display and configure it
    - Modify the **System\_ID = 2** (System ID Peripheral)
    - Generate the expanded Nios II processor
  - Back to Quartus II
    - Import pin assignment from de2.qsf
    - Open the DE2\_Basic\_Computer.v, save it as a *<top\_level\_entity>.v* and add the file to the project

# Guided example (3)

- Expanding the DE2 Basic Computer adding the **16x2 Character Display** peripheral
  - Modify the module name
  - Add the LCD ports and connect them to the corresponding Nios II processor signals (to and from the 16x2 character display peripheral)
  - Generate the sdram\_pll
    - **DRAM\_CLK** must lead the **system\_clock** to compensate for clock skew due to DE2 PCB connections
  - Add constraint for **CLOCK\_50** as clock
  - Compile the design

# Guided example (4)

- Expanding the DE2 Basic Computer adding the **16x2 Character Display** peripheral
  - Move to the Nios II SBT – Eclipse
    - Create a new Nios II Application and BSP from Template;  
**use the new system\_nios.sopcinfo**
    - Write a program to test the LCD display
    - Program the FPGA w/ the new soc file
    - Run the LCD test application!

# SoPC Builder: new nios\_system.sopc

Altera SOPC Builder - nios\_system.sopc\* (E:\Data\Teaching\SE\Lab\Home\DE2\My\_DE2\_First\_Computer\nios\_system.sopc)

File Edit Module System View Tools Nios II Help

System Contents System Generation

Component Library

Project

- New component...

Library

- RGBto greyscale convertor
- Bridges
- Configuration & Programming
- DSP
- Interface Protocols
- Legacy Components
- Memories and Memory Controllers
- Microcontroller Peripherals
- Peripherals
- PLL
- Processors
- Qsys Interconnect
- SLS
- University Program
  - Clock Signals for DE-Series Board P
  - Audio & Video
    - 16x2 Character Display
    - Audio
    - Audio and Video Config
  - Video
  - Bridges
  - Communications
  - Generic IO
  - Memory
  - Verification

Target

Device Family: Cyclone II

Clock Settings

Name	Source	MHz	
clk	External	50,0	<div>Add</div> <div>Remove</div>

Use	Conn...	Name	Description	Clock	Base	End	IRQ	Tags
<input checked="" type="checkbox"/>		<input type="checkbox"/> CPU	Nios II Processor	[clk]				
		instruction_master	Avalon Memory Mapped Master	clk				
		data_master	Avalon Memory Mapped Master	[clk]				
		jtag_debug_module	Avalon Memory Mapped Slave	[clk]				
<input checked="" type="checkbox"/>		<input type="checkbox"/> SDRAM	SDRAM Controller	clk	0x00000000	0x007fffff		
<input checked="" type="checkbox"/>		<input type="checkbox"/> SRAM	SRAM/SSRAM Controller	clk	0x08000000	0x0807ffff		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Onchip_memory	On-Chip Memory (RAM or ROM)	multiple	multiple	multiple		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Red_LEDs	Parallel Port	clk	0x10000000	0x1000000f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Green_LEDs	Parallel Port	clk	0x10000010	0x1000001f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> HEX3_HEX0	Parallel Port	clk	0x10000020	0x1000002f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> HEX7_HEX4	Parallel Port	clk	0x10000030	0x1000003f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Slider_switches	Parallel Port	clk	0x10000040	0x1000004f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Pushbuttons	Parallel Port	clk	0x10000050	0x1000005f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Expansion_JP1	Parallel Port	clk	0x10000060	0x1000006f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Expansion_JP2	Parallel Port	clk	0x10000070	0x1000007f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> JTAG_UART	JTAG UART	[clk]				
		avalon_jtag_slave	Avalon Memory Mapped Slave	clk	0x10001000	0x10001007		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Serial_port	RS232 UART	clk	0x10001010	0x10001017		
<input checked="" type="checkbox"/>		<input type="checkbox"/> Interval_timer	Interval Timer	clk	0x10002000	0x1000201f		
<input checked="" type="checkbox"/>		<input type="checkbox"/> vsvid	System ID Peripheral	clk	0x10002020	0x10002027		
<input checked="" type="checkbox"/>		<input type="checkbox"/> character_lcd_0	16x2 Character Display	[clock_reset]				
		avalon_lcd_slave	Avalon Memory Mapped Slave	clk	0x10002030	0x10002031		

Remove Edit...

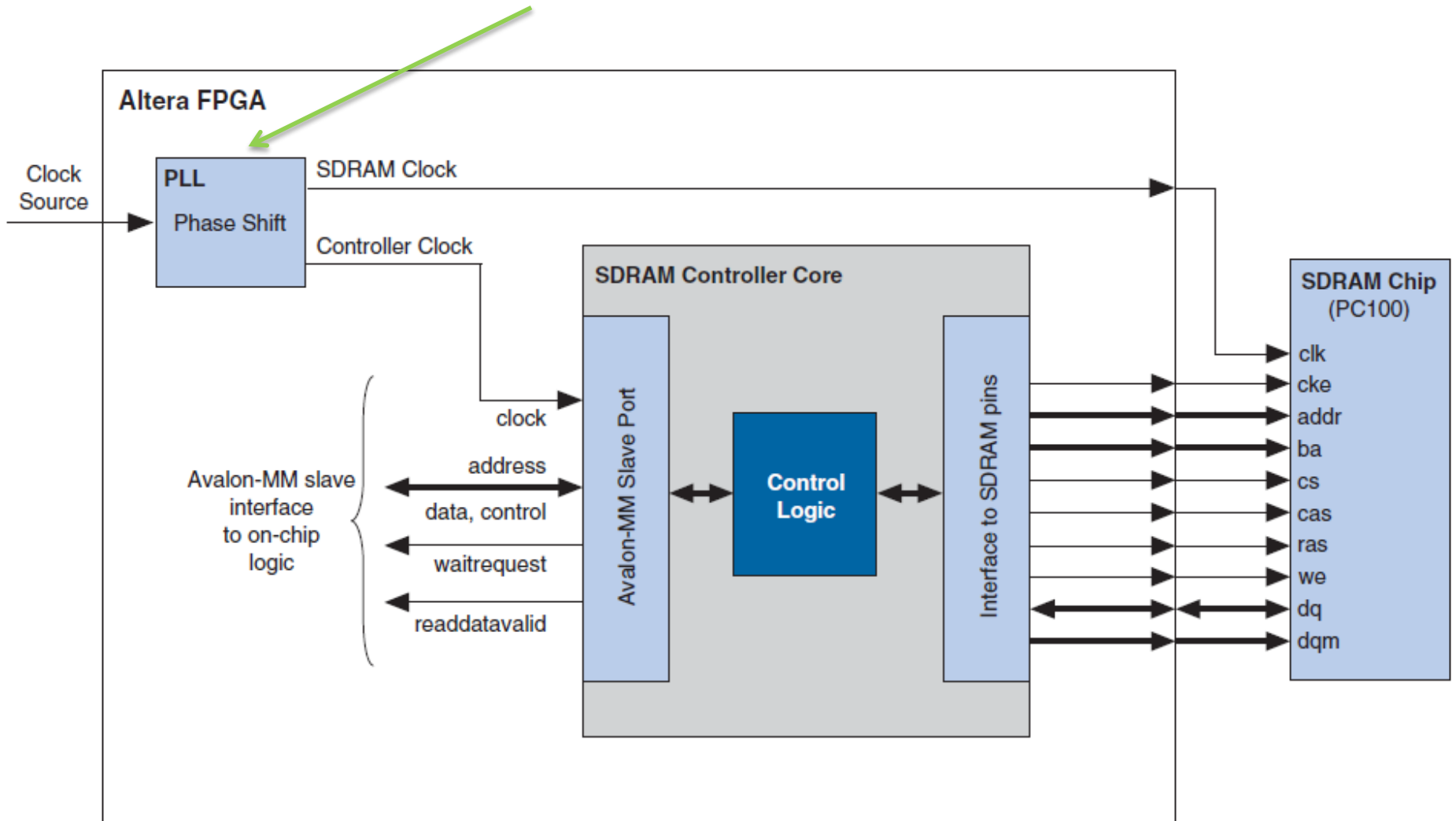
Address Map... Filters... Filter: Default



# SDRAM controller

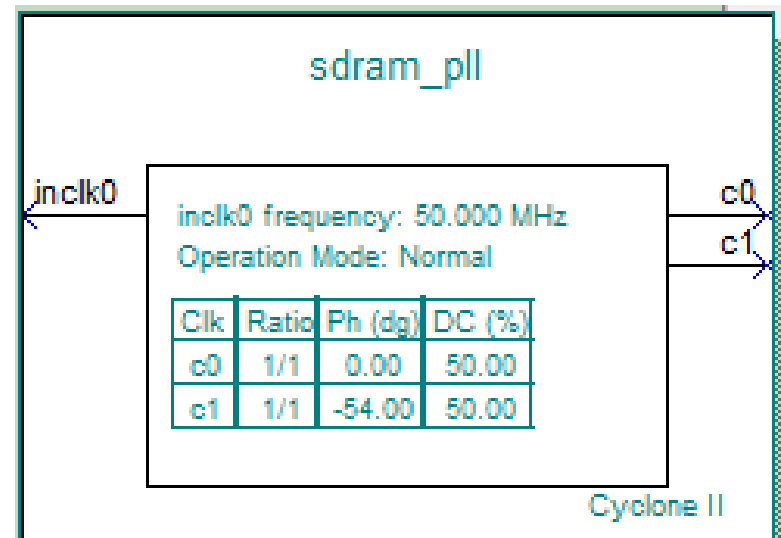
A PLL can be used to compensate for the clock skew introduced by PCB connections

*DE2 board SDRAM Clock must lead Controller Clock by 3 ns (Phase shift)*



# SDRAM Clock

- Require instantiating and configuring a PLL
  - Can be done using the MegaWizard Plug-in Manager [I/O Library]
  - C0 and c1 have the same frequency as inclok0, i.e. 50 MHz but are shifted each other by 3 ns



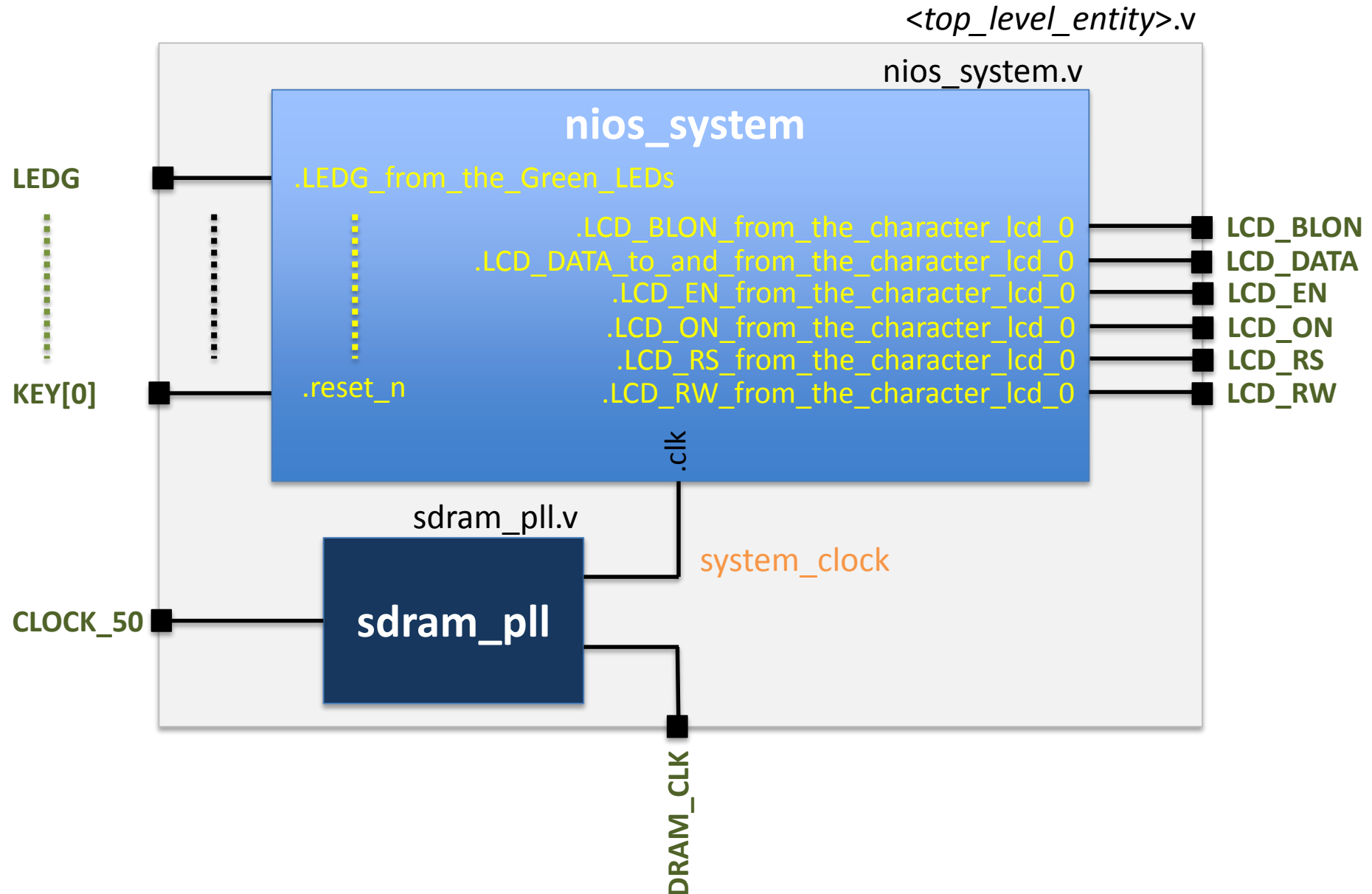
# Assembling the SoPC system (1)

The ports of the nios\_system and sdram\_pll have to be connected each other or to the external signals of the FPGA

External signals of the FPGA connected to the 16x2 character display

Signal Name	FPGA Pin No.	Description
LCD_DATA[0]	PIN_J1	LCD Data[0]
LCD_DATA[1]	PIN_J2	LCD Data[1]
LCD_DATA[2]	PIN_H1	LCD Data[2]
LCD_DATA[3]	PIN_H2	LCD Data[3]
LCD_DATA[4]	PIN_J4	LCD Data[4]
LCD_DATA[5]	PIN_J3	LCD Data[5]
LCD_DATA[6]	PIN_H4	LCD Data[6]
LCD_DATA[7]	PIN_H3	LCD Data[7]
LCD_RW	PIN_K4	LCD Read/Write Select, 0 = Write, 1 = Read
LCD_EN	PIN_K3	LCD Enable
LCD_RS	PIN_K1	LCD Command/Data Select, 0 = Command, 1 = Data
LCD_ON	PIN_L4	LCD Power ON/OFF
LCD_BLON	PIN_K2	LCD Back Light ON/OFF

# Assembling the SoPC system (2)



# Character LCD API

- Header file: altera\_up\_character\_lcd.h
- Device type: alt\_up\_character\_lcd\_dev
- Function prototypes:
  - alt\_up\_character\_lcd\_dev\* alt\_up\_character\_lcd\_open\_dev(const char\* name);
  - void alt\_up\_character\_lcd\_init(alt\_up\_character\_lcd\_dev \*lcd);
  - int alt\_up\_character\_lcd\_set\_cursor\_pos (alt\_up\_character\_lcd\_dev \*lcd, unsigned x\_pos, unsigned y\_pos);
  - void alt\_up\_character\_lcd\_string(alt\_up\_character\_lcd\_dev \*lcd, const char \*ptr);
  - ...

# Test the new Nios II system

- Write a simple program that writes a string on the 16x2 character display

# References

- Altera, “Using the SDRAM Memory on Altera’s DE2 Board,” *tut\_DE2\_sdram\_verilog.pdf*
- with Verilog Design
- Altera, “16x2 Character Display for Altera DE2-Series Boards,” *Character\_LCD.pdf*