

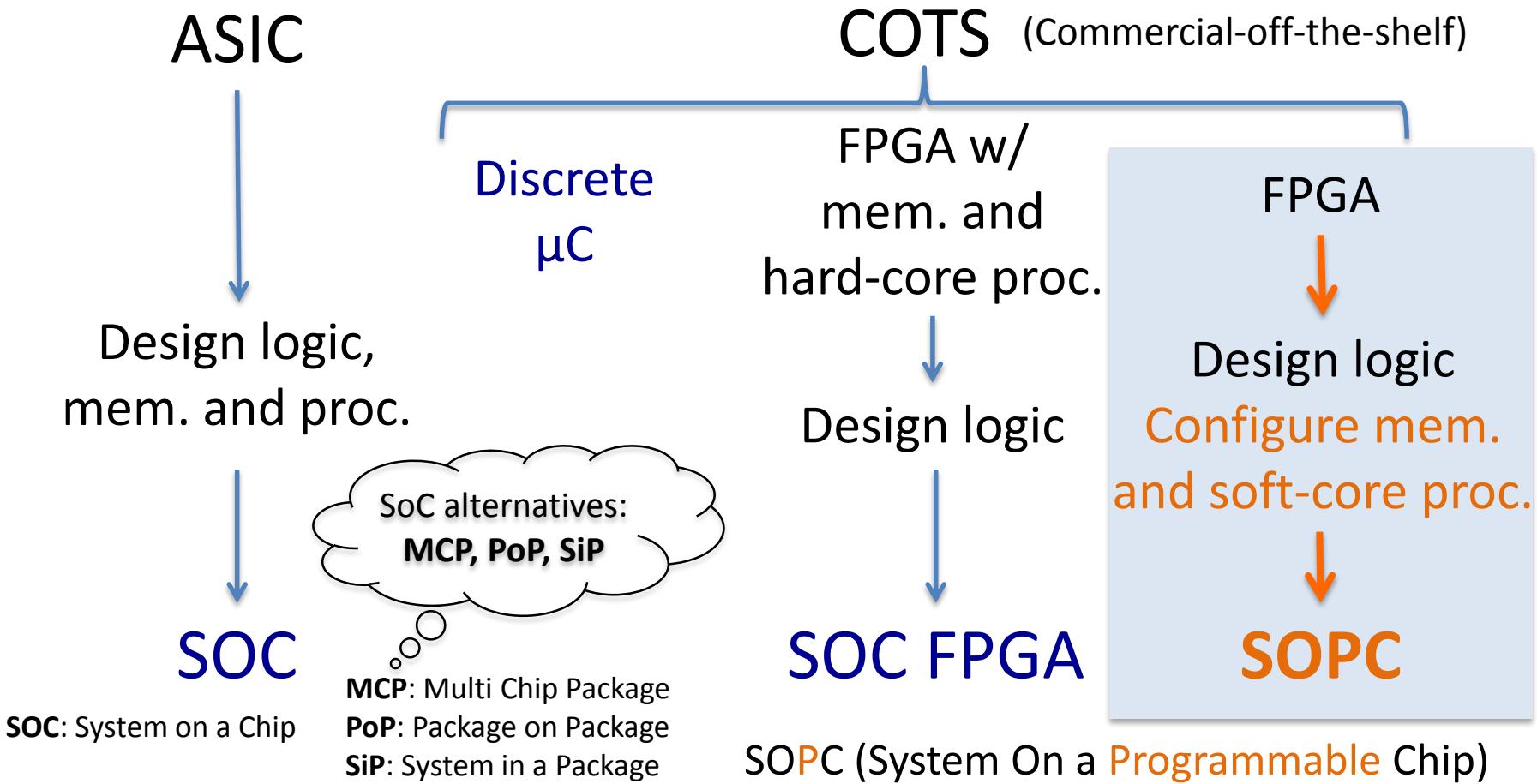
SISTEMI EMBEDDED

AA 2012/2013

SOPC Design Flow

An **embedded system** is a computer that is **not** general-purpose like a personal computer

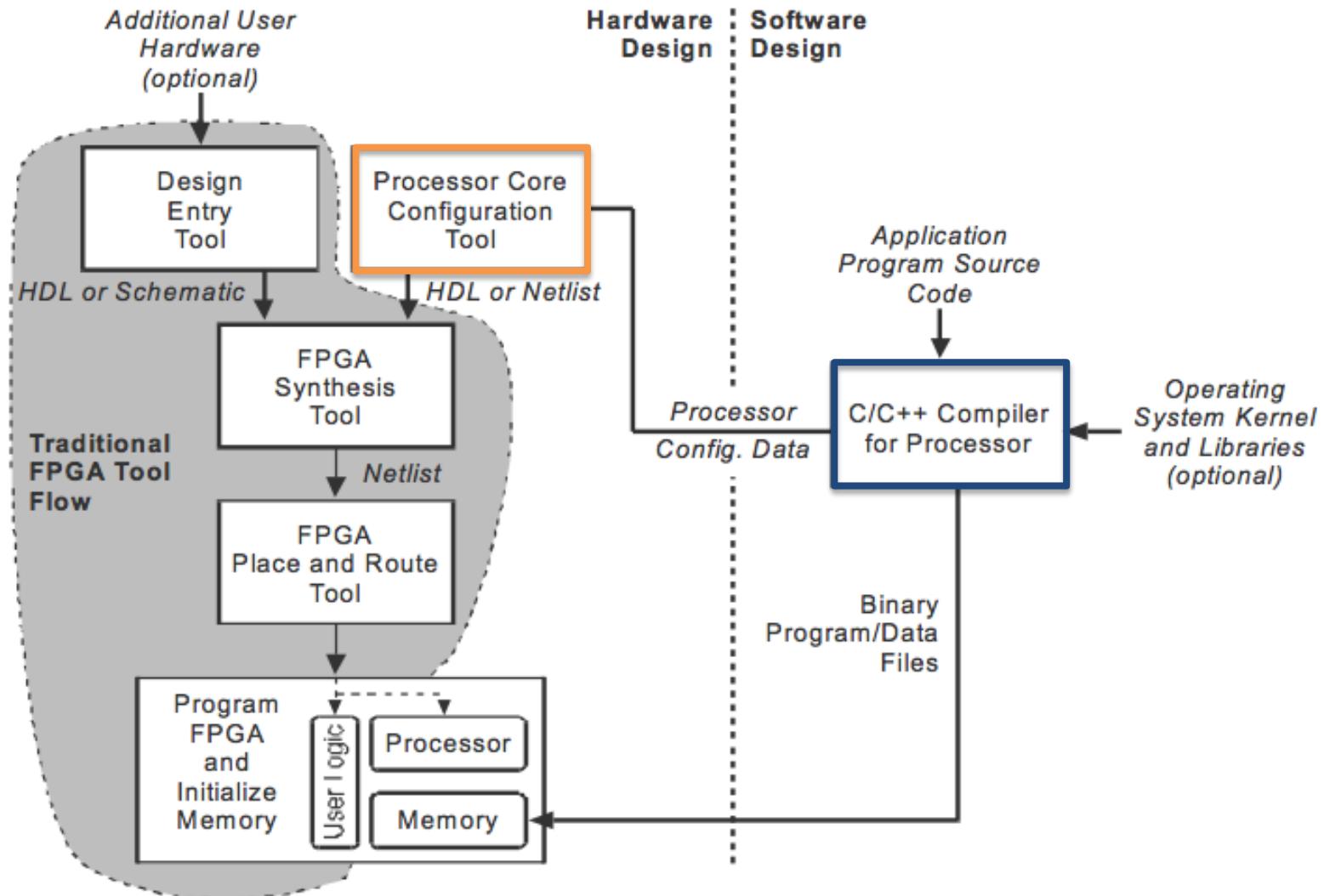
Hardware design options:



System-on-Programmable-Chip

- Configure soft-core processor:
 - Core configuration
 - Instruction/Data Cache, Pipeline Stages, JTAG Debug Modules, Custom Instructions, etc.
 - Peripheral configuration (what and where)
 - Peripheral selection
 - Standard peripherals from Altera and third-party vendors: GPIOs, Timers, Serial Communication Interfaces, Memory Interfaces, etc.
 - Custom peripherals
 - Address mapping

SOPC Design Flow



Altera's CAD tools

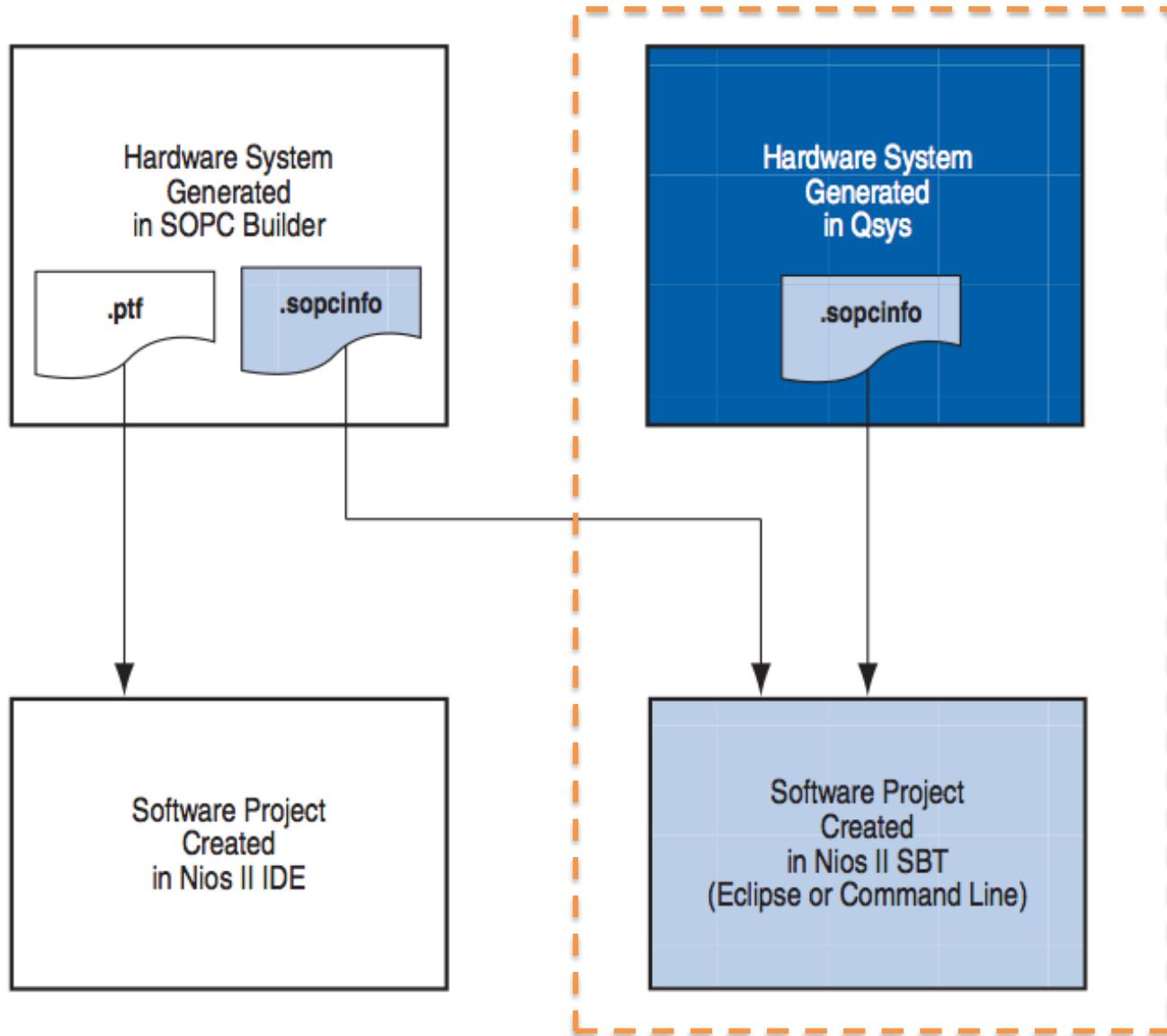
- Logic Design: **Quartus II**
- Nios II Configuration: **SOPC Builder - Qsys**
- Software Development:
Nios II Embedded Design Suite (EDS) – Eclipse

Embedded System course

- Quartus II Web Edition Software (12.1sp1)
 - <http://www.altera.com/products/software/quartus-ii/web-edition/qts-we-index.html>
- University Program Installer
 - <http://www.altera.com/education/univ/software/monitor/unv-monitor.html>
- Nios II Documentation
 - <http://www.altera.com/literature/lit-nio2.jsp>
- DE2: Development & Education board
 - Cyclone II EP2C35F672C6 (33216 LE; 105 M4K)

	Nios II/e	Nios II/s	Nios II/f
#LE	600-700	1200-1400	1400-1800
#M4K	2	2 + cache	3 + cache

Nios II HW/SW Design Flow



Nios II SBT Design Flow

- Creating a project
 - Nios II Application and BSP from Template
 - Target hardware information (`.sopcinfo`, CPU)
 - Project template
 - Board Support Package (BSP)
- Code editing (`.c`, `.h`)
- Building the Project (`.elf`)
- Configuring the FPGA
 - Quartus II programmer (`.sof`)
- Running/ Debugging the Project on Nios II
 - Run/Debug configurations

Board Support Package (BSP)

- Library and header files (**e.g. system.h**) specific to the target processor
- Automatically generated through .sopcinfo and CPU
- Hides memory map, available devices, device implementation and processor configuration
 - Device drivers
 - Hardware Abstraction Layer (HAL)
 - RTOS: Micrium MicroC/OS-II