

SISTEMI EMBEDDED

Course Presentation – Spring 2017

Federico Baronti

Dip. Ing. Informazione

Via G. Caruso, 16 – Stanza B-1-09

050 2217581 – federico.baronti@unipi.it

<http://www.iet.unipi.it/f.baronti/>

Office hours:

Friday 15-18. Please, contact me in advance before showing up.

Class Schedule

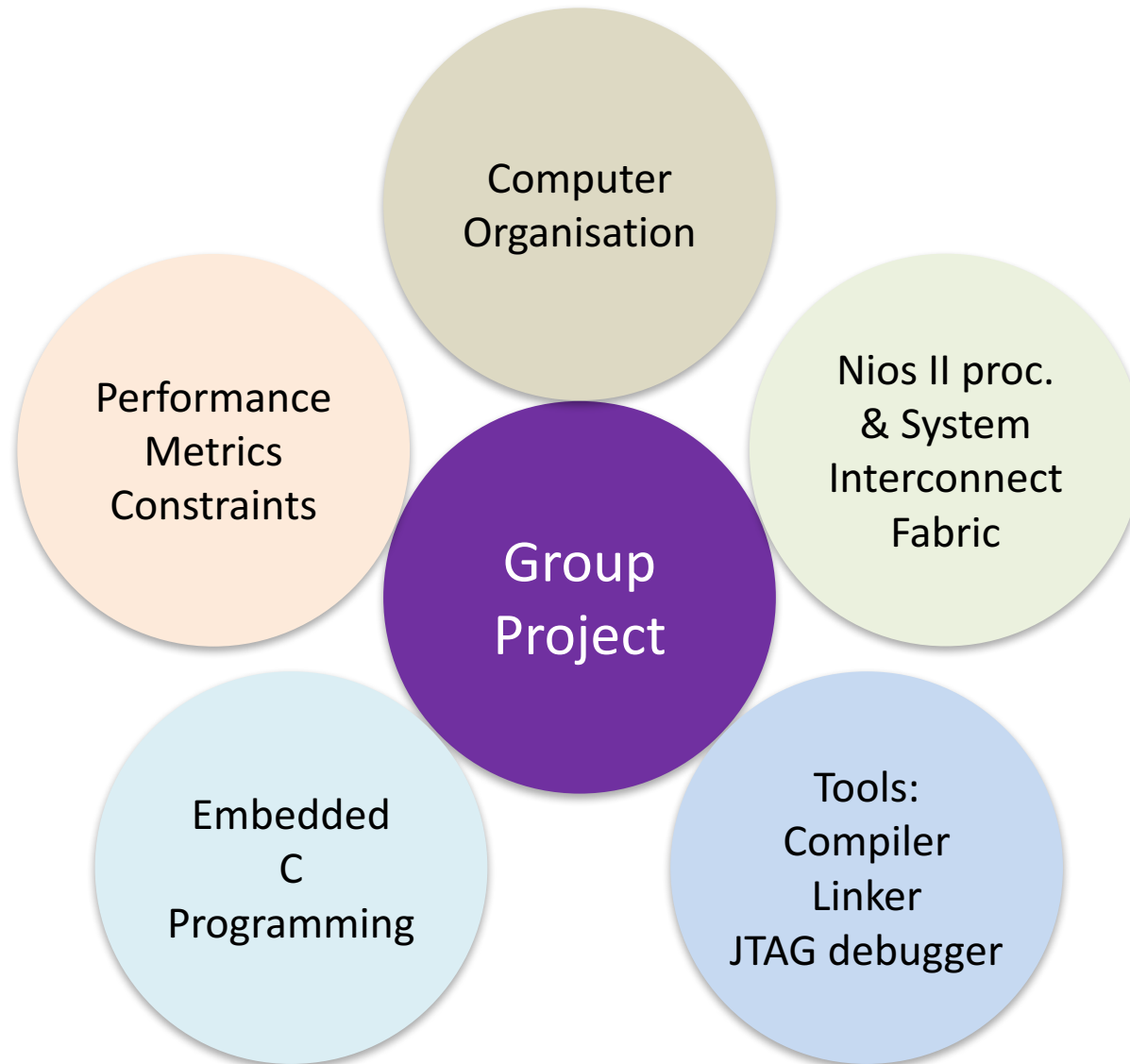
2M Elettronica						
	Lu	Ma	Me	Gi	Ve	Sa
8:30/9:30			Sistemi embedded B23			
9:30/10:30	Nanoelettronica C33	Nanoelettronica B24	Sistemi embedded B23			
10:30/11:30	Nanoelettronica C33	Nanoelettronica B24	Sistemi di elaborazione SI 7			
11:30/12:30	Nanoelettronica C33		Sistemi di elaborazione SI 7			
12:30/13:30		Optional Lab	Sistemi di elaborazione SI 7			
13:30/14:30	Sistemi di elaborazione ADII 1	Sistemi embedded B26				
14:30/15:30	Sistemi di elaborazione ADII 1	Sistemi embedded B26	Nanoelettronica B25			
15:30/16:30	Sistemi embedded B26	Sistemi embedded B26	Nanoelettronica B25			
16:30/17:30	Sistemi embedded B26		Nanoelettronica B25			
17:30/18:30	Sistemi embedded B26					

Course Objectives

Learn expertise and methodologies to design and program an embedded system

We'll use as a reference a **System on Programmable Chip (SoPC)** platform based on an Intel (formerly Altera) FPGA

Course Organization



Course Requirements

- Digital Electronics
- Digital Logic Design
 - HDL Coding
- Software Programming
 - Basic knowledge of C or C++ Language

Group Project

- Design an SoPC on a Cyclone II FPGA hosted on the Terasic DE 2 board
 - Computer implementation
 - May require the design of one or more custom peripherals
 - Software programming
- Project assignment during the 5th week
- See Projects of previous years to gather an idea

Course Material (1)

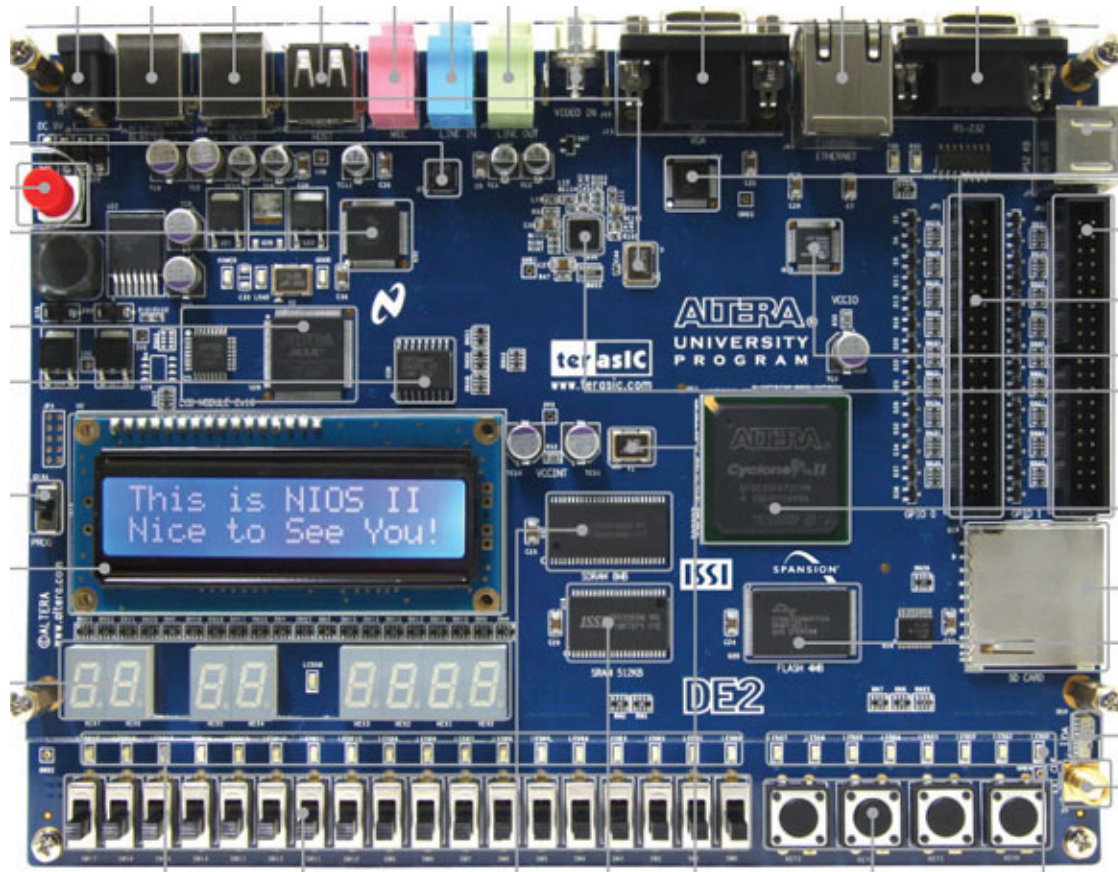
- Available at the course web page:
<http://www.iet.unipi.it/f.baronti/didattica/SE/2016/Sistemi%20Embedded.html>
- Slides used during the lessons
- Text book:
 - C. Hamacher, Z. Vranesic, S. Zaky, N. Manjikian
"Computer Organization and Embedded Systems,"
McGraw-Hill International Edition
- Documentation from Altera

Course Material (2)

- Quartus II Web Edition Software (**13.0sp1**)
<http://dl.altera.com/13.0sp1/>
 - Quartus II Software (includes Nios II EDS)
 - ModelSim-Altera Edition (includes Starter Edition)
 - Devices: Cyclone II, Cyclone III, Cyclone IV device support (includes all variations)
- University Program Installer (**13.0**)
 - <https://www.altera.com/support/training/university/materials-software.html> - University-Program-Installer
- Nios II Documentation
 - <http://www.altera.com/literature/lit-nio2.jsp>

Course Material (3)

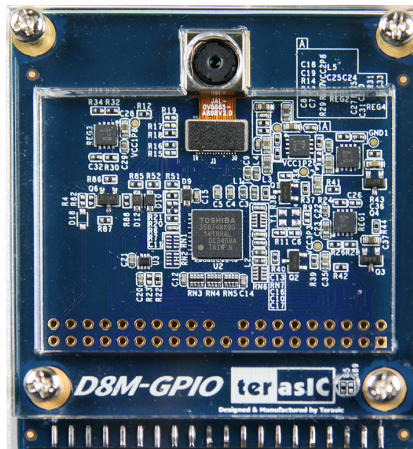
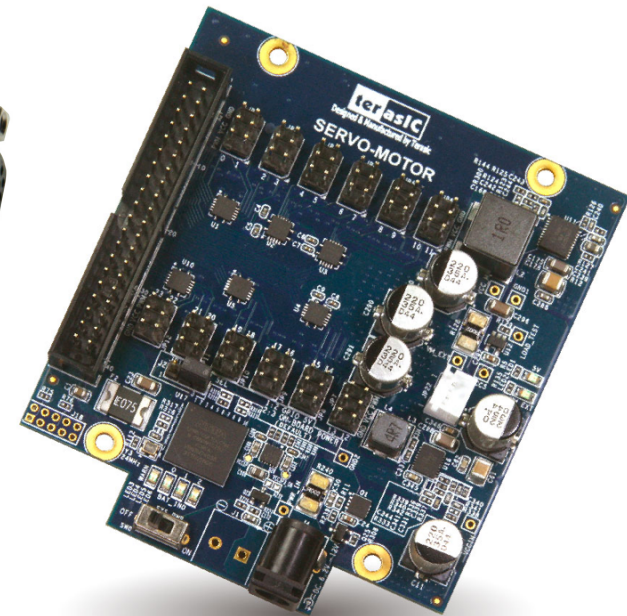
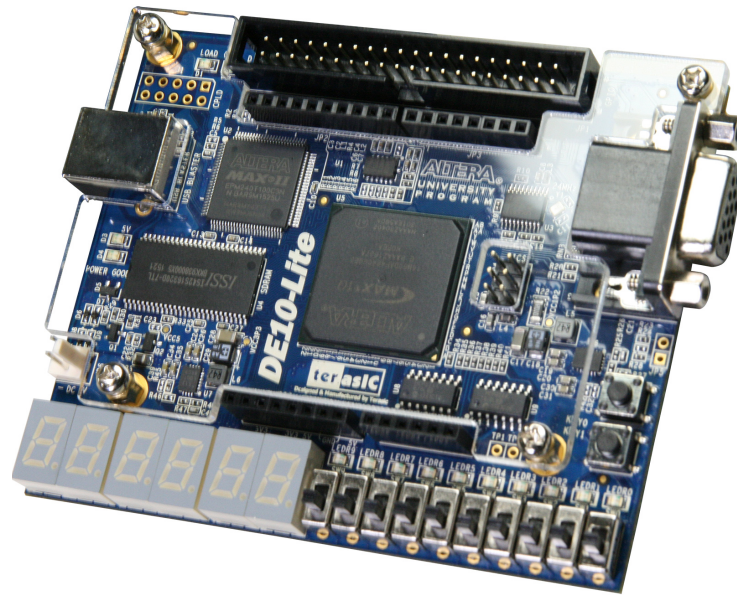
- 10x DE2: Development & Education board
 - Cyclone II EP2C35F672C6 (33216 LE; 105 M4K)



Course Material (4)

NEW

- 4x DE10-Lite Board w/ MAX 10 FPGA
 - 2x Touch display (LT24), 8 M Pixel Camera (D8M-GPIO), Servo Motor Kit (SVK)



Exam Evaluation

- Project Evaluation (~40 %): the same marking for all the group members
 - Presentation and Demo (~30 %) - Due on last class (May 30, 2017)
 - Project report (~70 %) – Due a “week” before the selected exam date
- Oral Test (~60 %)
 - Project discussion (~50 %)
 - Assessment of understanding and mastering the course contents (~50 %)