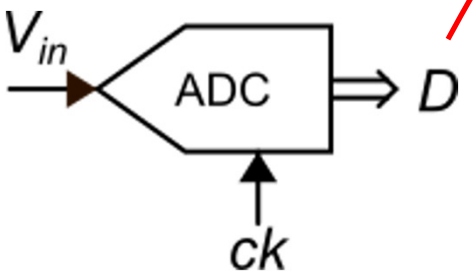
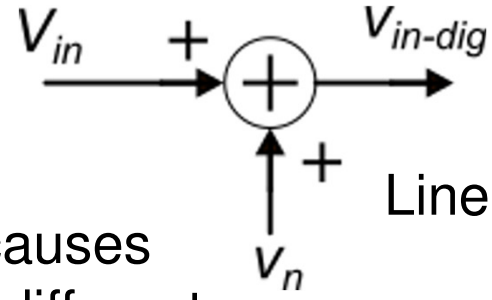
ADC linearized model

$$v_{in-dig} = V_{MIN} + \frac{V_{FS}}{2^n} D$$





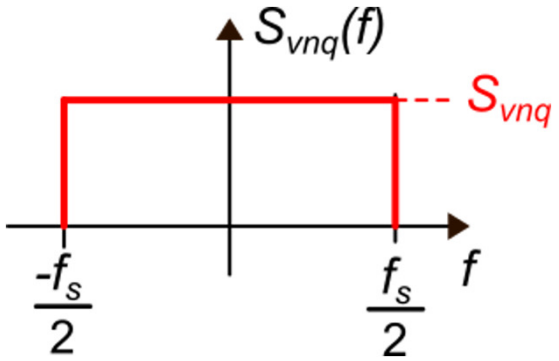
Linearized model

v_n includes **all** causes that make v_{in-dig} different from V_{in}

The error due to quantization can be represented by a component of v_n: the quantization noise:

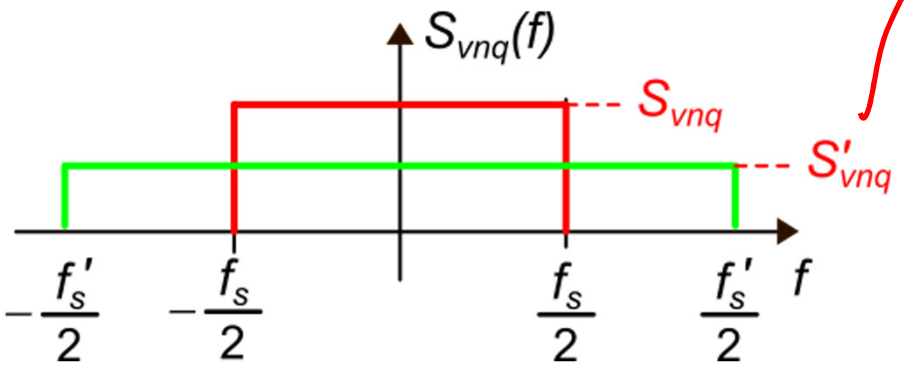
$$\left\langle v_{nq}^2 \right\rangle = \frac{\Delta^2}{12}$$

Uniform quantization noise PSD: properties



Total v_{nq} power: $\left\langle v_{nq}^2 \right\rangle = \frac{\Delta^2}{12}$ $\quad S_{vnq} = \frac{\Delta^2}{12}\frac{1}{f_s}$

Increasing the sampling frequency:

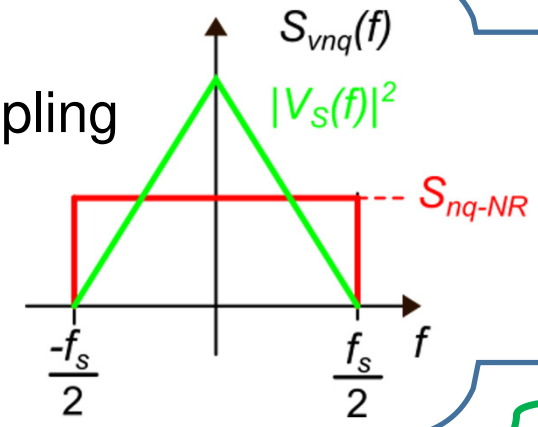


$$S'_{vnq} = \frac{\Delta^2}{12}\frac{1}{f_s'} = \frac{\Delta^2}{12}\frac{1}{f_s'}\frac{f_s}{f_s} = S_{vnq}\frac{f_s}{f_s'}$$

For the same ADC, increasing the sampling frequency proportionally reduces the PSD of the quantization noise

Oversampling ADCs

Nyquist rate sampling

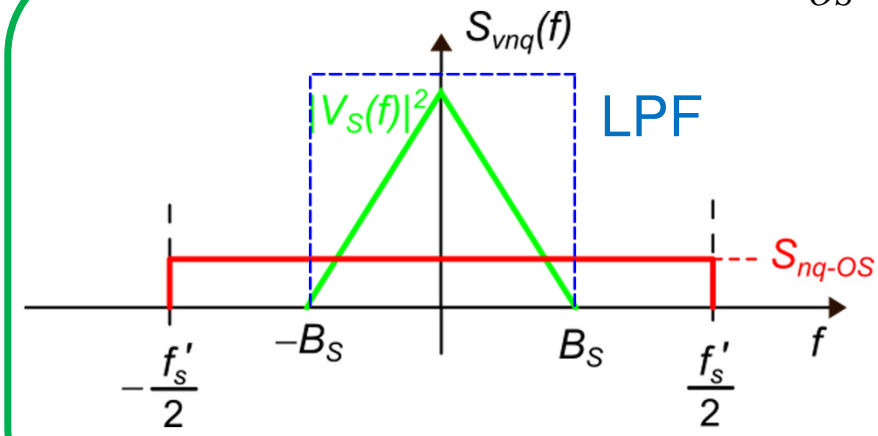


$$f_S = 2B_S = \text{"Nyquist rate"}$$

$$\left\langle v_{nq-NR}^2 \right\rangle = \frac{\Delta^2}{12} = f_S \cdot S_{nq-NR} = 2B_S \cdot S_{nq-NR}$$

$$r_{OS} = \frac{f_S'}{2B_S} > 1$$

r_{OS}=OSR
OverSampling Ratio



Oversampling case

$$f_S' = r_{OS} \cdot 2B_S \qquad S_{nq-OS} = S_{nq-NR}\frac{2B_S}{f_S'} = \frac{S_{nq-NR}}{r_{OS}}$$

$$\left\langle v_{nq-OS}^2 \right\rangle = 2B_S \cdot S_{nq-OS} = \frac{2B_S \cdot S_{nq-NR}}{r_{OS}} = \frac{1}{r_{OS}}\left\langle v_{nq-NR}^2 \right\rangle$$

Resolution increment in a pure oversampling ADC

Premise

Considering two ADCs with same V_{FS}

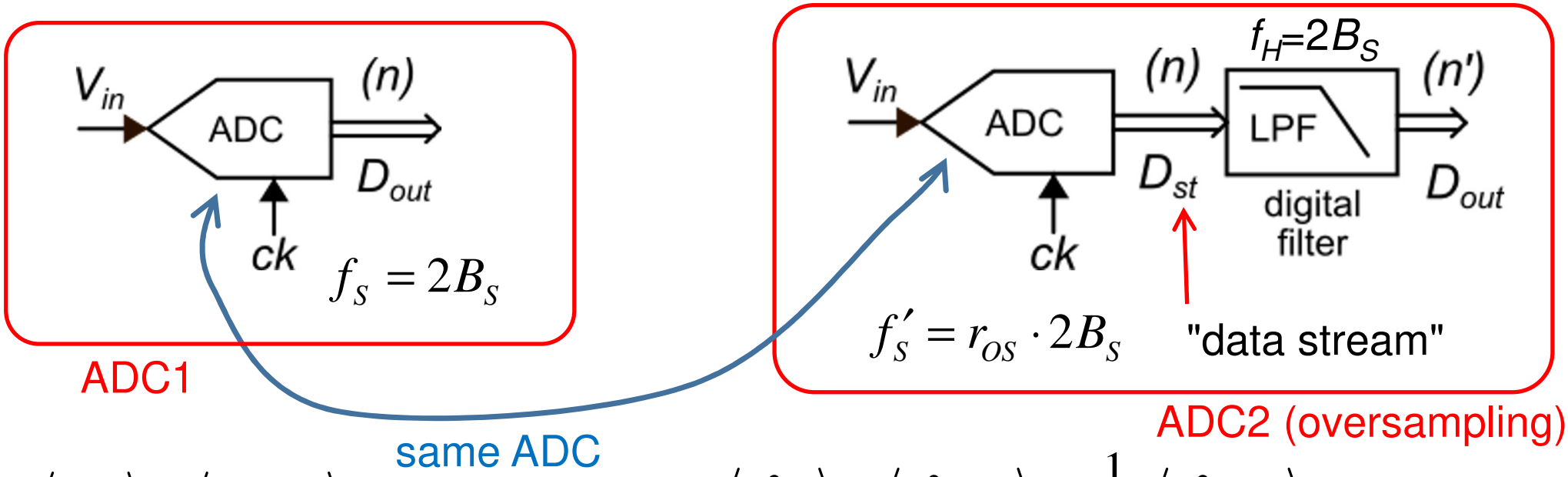
$$\begin{cases} \text{ADC}_1\text{: SQNR}_1,\ n_1 \\ \text{ADC}_2\text{: SQNR}_2,\ n_2 \end{cases}$$

$$SQNR = \frac{P_{MAX}}{\left\langle v_{nq}^2 \right\rangle} = \frac{3}{2} \cdot 2^{2n} \qquad P_{MAX} = \frac{V_{FS}^2}{8} \qquad \Rightarrow P_{MAX1} = P_{MAX1}$$

$$\frac{SQNR_2}{SQNR_1} = 2^{2(n_2 - n_1)} = \frac{P_{MAX2}}{\left\langle v_{nq2}^2 \right\rangle} \frac{\left\langle v_{nq1}^2 \right\rangle}{P_{MAX1}} = \frac{\left\langle v_{nq1}^2 \right\rangle}{\left\langle v_{nq2}^2 \right\rangle}$$

$$n_2 - n_1 = \frac{1}{2} \log_2 \left(\frac{\left\langle v_{n1}^2 \right\rangle}{\left\langle v_{n2}^2 \right\rangle} \right)$$

Resolution increment in a pure oversampling ADC



$$\left\langle v_{nq1}^2 \right\rangle = \left\langle v_{nq-NR}^2 \right\rangle \qquad \left\langle v_{nq2}^2 \right\rangle = \left\langle v_{nq-OS}^2 \right\rangle = \frac{1}{r_{OS}} \left\langle v_{nq-NR}^2 \right\rangle$$

$$n_2 - n_1 = \frac{1}{2}\log_2\left(\frac{\left\langle v_{n1}^2 \right\rangle}{\left\langle v_{n2}^2 \right\rangle}\right) = \frac{1}{2}\log_2\left(\frac{\left\langle v_{nq-NR}^2 \right\rangle}{\left\langle v_{nq-OS}^2 \right\rangle}\right) = \frac{1}{2}\log_2\left(r_{OS}\right)$$

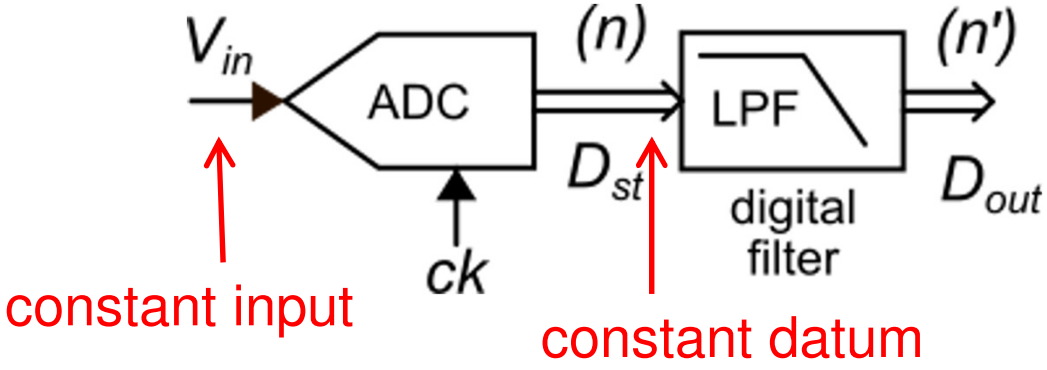
Resolution improvement

Pure oversampling ADCs: limits

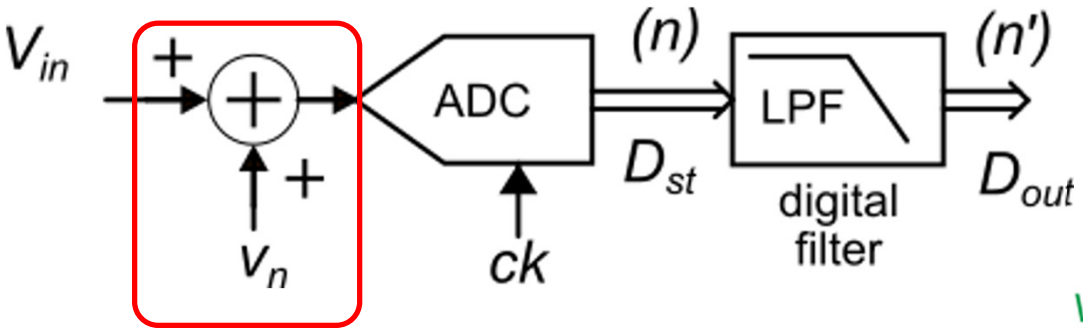
A minor limit:

The oversampling approach is based on the assumption that the quantization noise respects the uniform PSD model

If the input signal is a dc, the quantization noise superimposed on the data stream will be constant and then will be unaffected by the LPF. A similar problem occurs with signals that are slowly-varying and/or have a small magnitude.

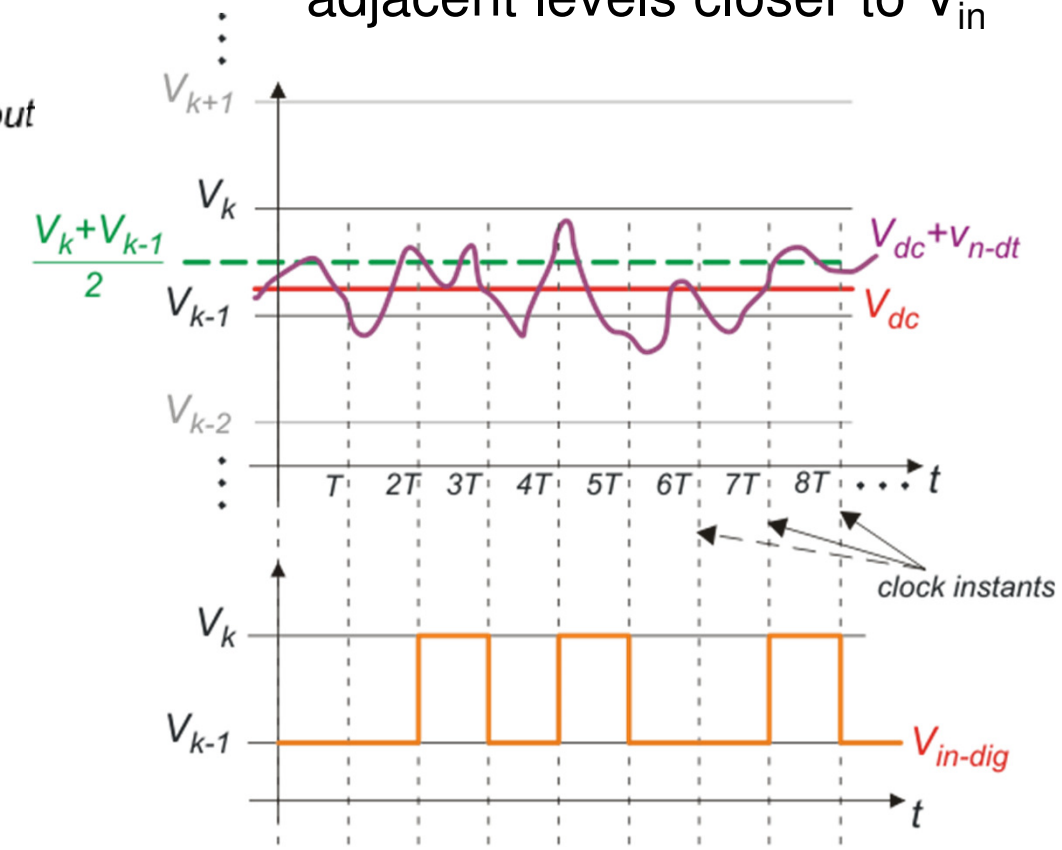


Signal dithering



Dithering

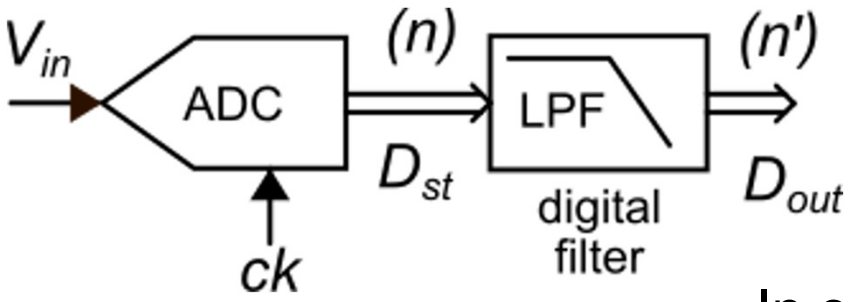
Noise makes the ADC switch across the two adjacent levels closer to V_{in}



Dithering consists in adding noise to the signal.

The added noise must have spectral components out of the signal band so that it is rejected by the LPF

The real limitation of the pure oversampling approach



$$n_{OS} - n_{NR} = \frac{1}{2}\log_2\left(r_{OS}\right)$$

In order to obtain a resolution increment of a single bit, the sampling frequency must be incremented by a factor of 4

Example:

To obtain 16 bits of resolution from a 12 bit ADC:

$$n_{OS} - n_{NR} = 4 \quad \text{(bits)}$$

$$r_{OS} = \frac{f_S}{2B_S} = 4^4 = 256$$

The pure oversampling approach is highly inefficient !

The Delta-Sigma (Δ–Σ) ADC

The Delta-Sigma converter combines two principles:

- Oversampling: $f_s >> 2B_s$
- Noise shaping

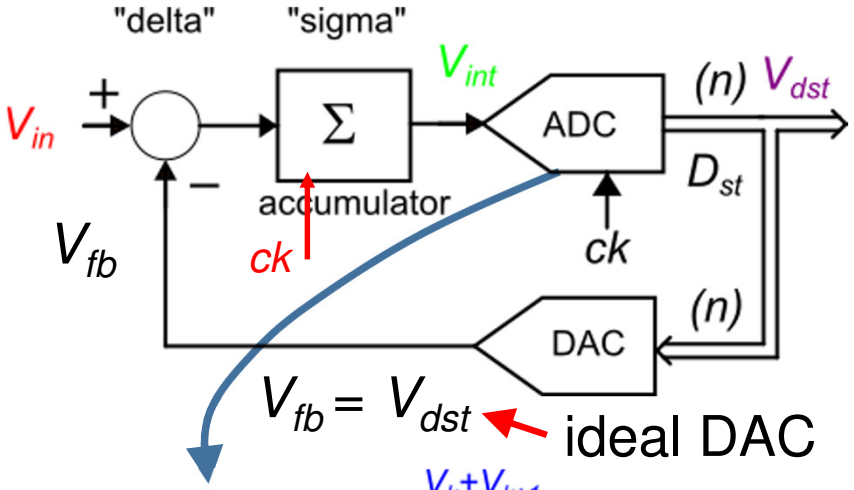
It was introduced in 1960

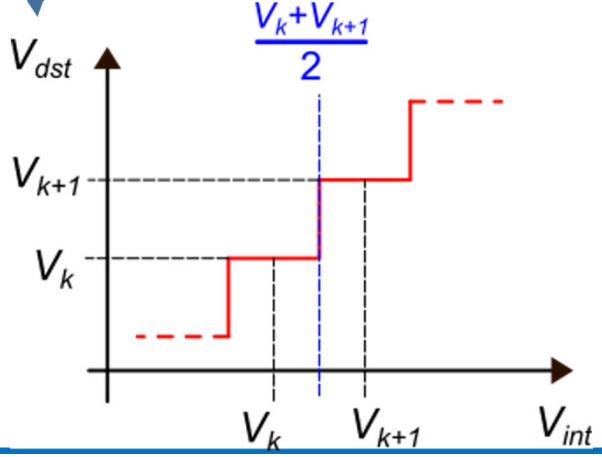
The term "Sigma-Delta (Σ–Δ)" ADC is simply a synonym.

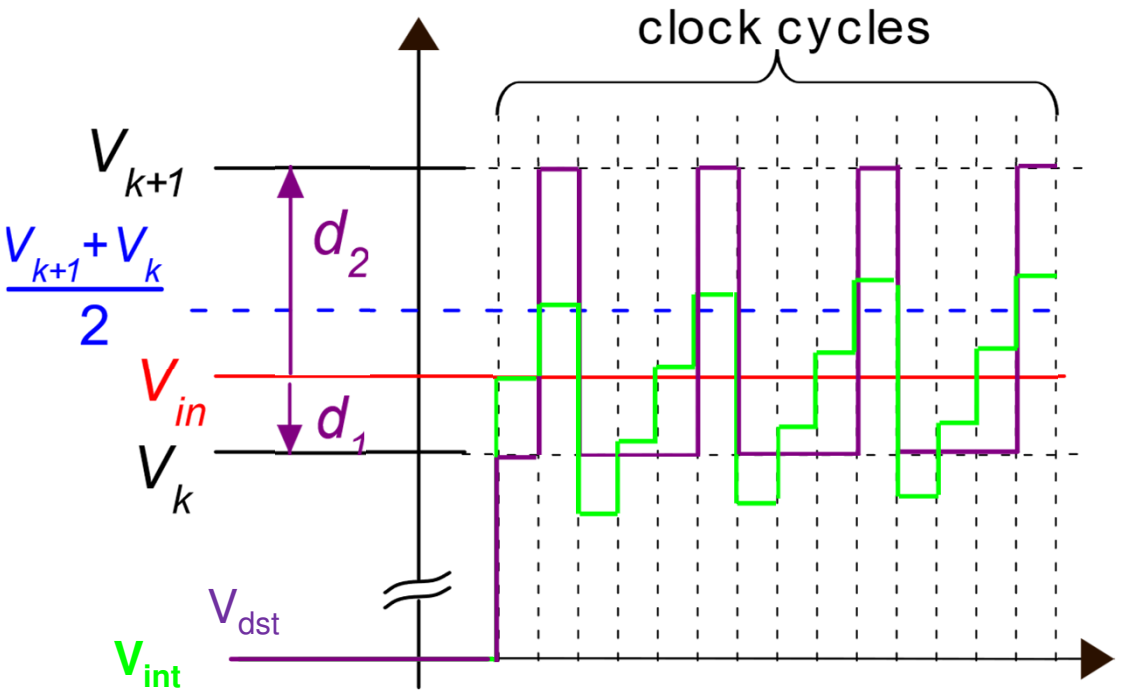
Delta-Sigma principle

Response to a DC voltage

The Delta-Sigma modulator (1st order)



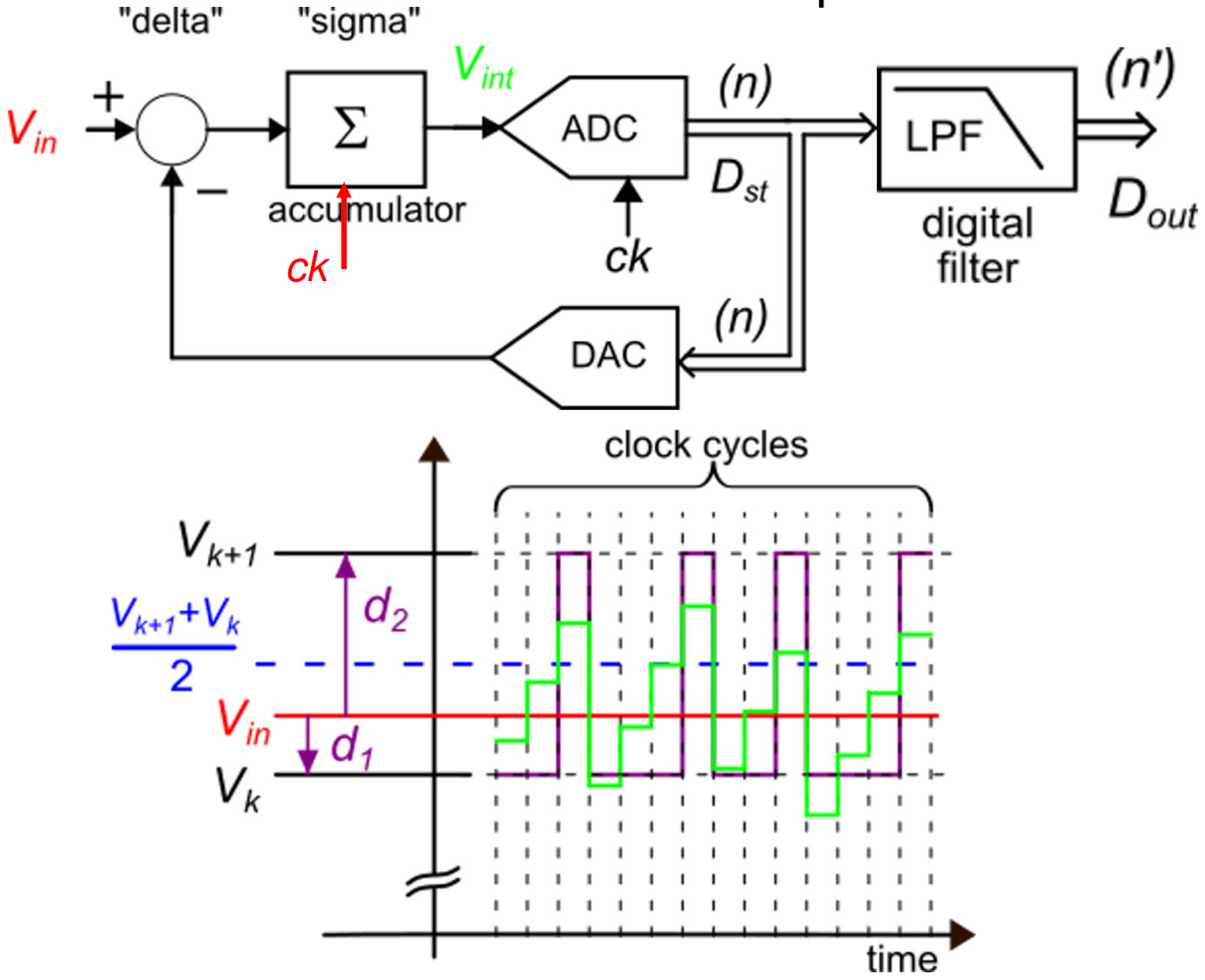




we imagine to start with $V_{int}=0$

Delta-Sigma principle

Response to a DC voltage



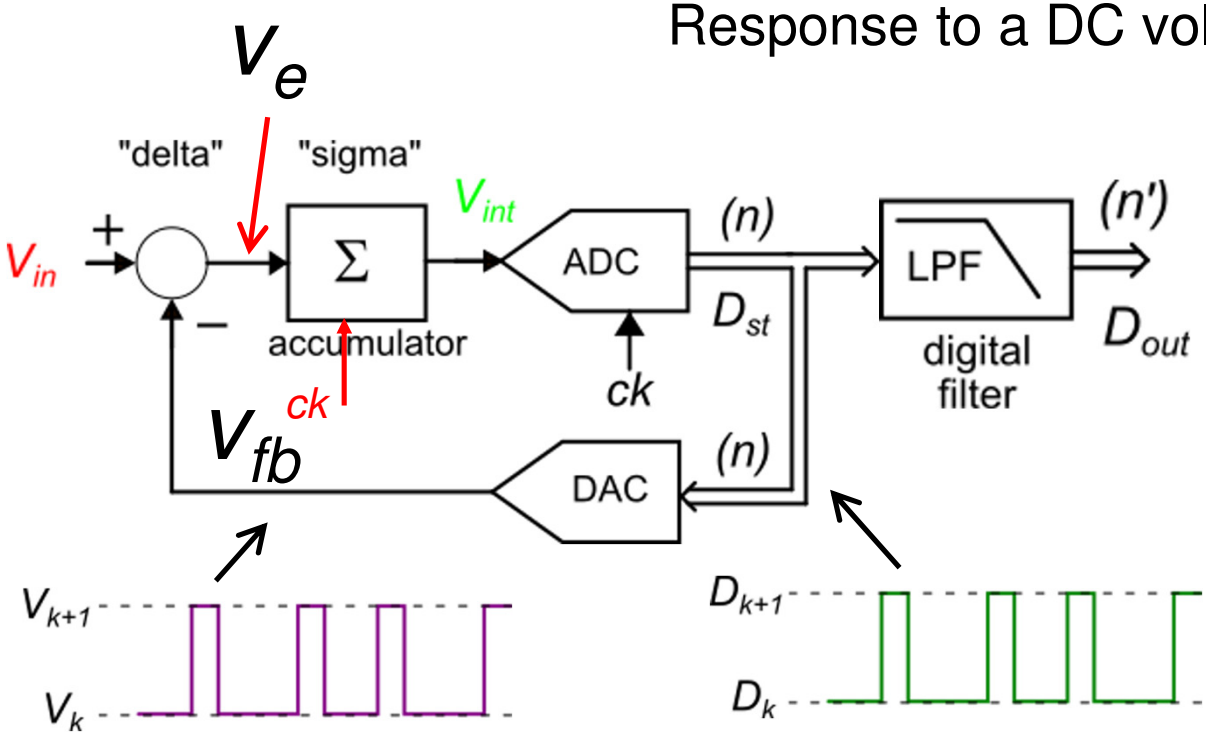
The digital filter averages the data stream that, in the example, contains only V_k and V_{k+1} levels.

The average will be a value between the two levels and will be closer to V_{in} than both V_k and V_{k+1}

In this example, value V_k appears more frequently than V_{k+1}. Then the average will be closer to V_k, as actually V_{in} is.

Delta-Sigma principle

Response to a DC voltage



The average of V_e, performed over a very long time, must be zero, otherwise the output of the accumulator would diverge.

$$\langle V_e \rangle = \langle V_{in} - V_{fb} \rangle = 0$$

$$\langle V_{fb} \rangle = \langle V_{in} \rangle$$

If the LPF filter has a bandwidth small enough, it can extract the average of the data stream D_k with arbitrary accuracy. If the DAC is ideal (no distortion), then the average of D_k gives V_{in} with an arbitrary resolution.

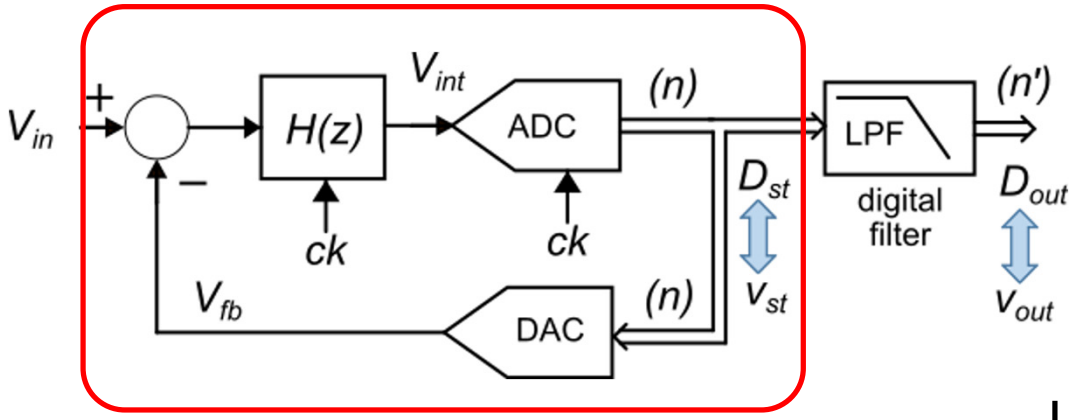
Delta-Sigma principle

What we have seen so far suggests that the delta-sigma modulator can produce a data stream that, once properly filtered, can yield V_{in} with a higher resolution than the original ADC.

Differently from the pure oversampling ADC, the delta-sigma is capable of producing the alternation of two adjacent codes ($V_{k,}$ V_{k+1}) even with a dc signal without dithering. In the case of an input dc signal, the constant error v_n is modulated (this is the origin of the name) and can be filtered out.

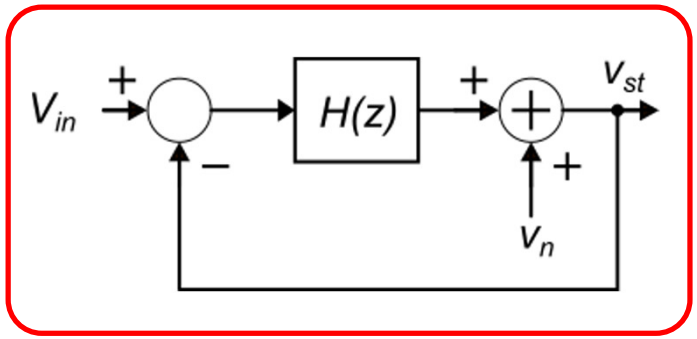
As in the oversampling approach, it is necessary to filter the output data stream, reducing the bandwidth to the minimum required by the signal spectrum. We will show that high resolution increments can be obtained with moderate oversampling ratios.

Analysis of a first order delta-sigma modulator



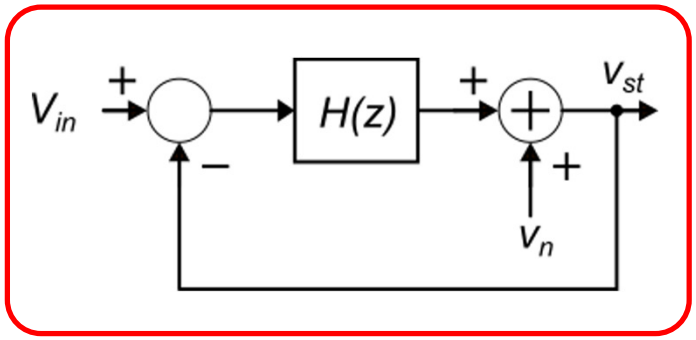
Δ–Σ modulator

H(*z*) is a discrete time transfer function, properly represented with its *z*-transform.



Linearized model of the modulator. The DAC is considered ideal; thus, it simply translates the voltage representation of D_{st} (v_{st}) in an exactly corresponding analog voltage (v_{fb}=v_{st})

Analysis of a first order delta-sigma modulator



$$v_{st} = (v_{in} - v_{st})\,H(z) + v_n$$

$$v_{st}\,[1 + H(z)] = v_{in} H(z) + v_n$$

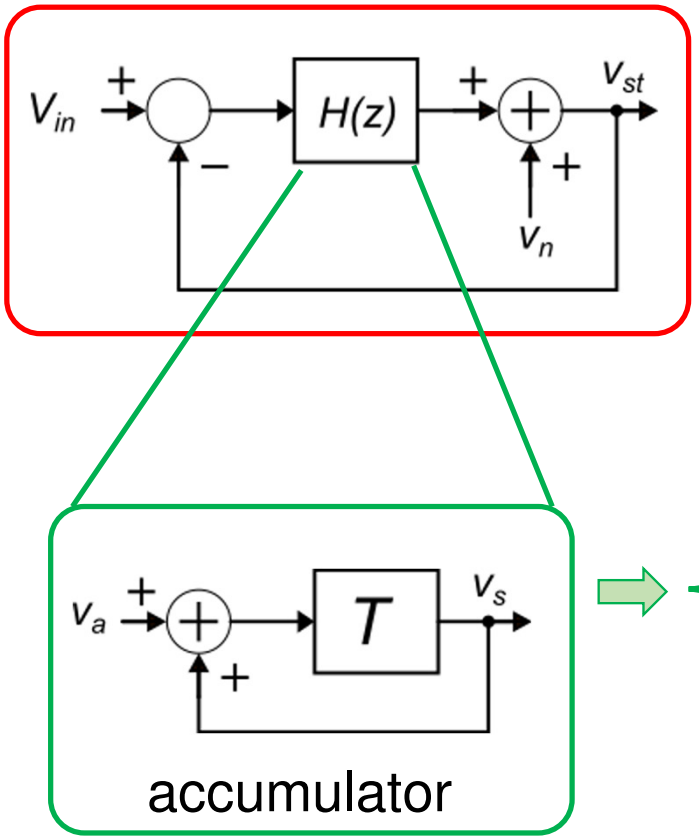
$$v_{st} = v_{in}\,\frac{H(z)}{1+H(z)} + v_n\,\frac{1}{1+H(z)}$$

$$v_{st} = v_{in} \cdot STF(z) + v_n \cdot NTF(z)$$

$$STF(z) = \text{Signal Transfer Function} = \frac{H(z)}{1+H(z)}$$

$$NTF(z) = \text{Noise Transfer Function} = \frac{1}{1+H(z)}$$

Analysis of a first order delta-sigma modulator



$$v_{st} = v_{in} \cdot STF(z) + v_n \cdot NTF(z)$$

$$STF(z) = \frac{H(z)}{1+H(z)} \qquad NTF(z) = \frac{1}{1+H(z)}$$

$$v_s(nT) = v_a(nT-T) + v_s(nT-T)$$

$$v_s(z) = v_a(z)z^{-1} + v_s(z)z^{-1}$$

$$v_s(z) = v_a(z)\frac{z^{-1}}{1-z^{-1}}$$

$$H(z) = \frac{z^{-1}}{1-z^{-1}}$$

Analysis of a first order delta-sigma modulator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} = \frac{1}{z - 1}$$ (forward Euler integrator)

$$STF(z) = \frac{H(z)}{1 + H(z)} = \frac{\frac{z^{-1}}{1 - z^{-1}}}{1 + \frac{z^{-1}}{1 - z^{-1}}} = \frac{\frac{z^{-1}}{1 - z^{-1}}}{\frac{1}{1 - z^{-1}}} = z^{-1}$$

A simple delay of one clock cycle

$$NTF(z) = \frac{1}{1 + H(z)} = \frac{1}{1 + \frac{z^{-1}}{1 - z^{-1}}} = \frac{1}{\frac{1}{1 - z^{-1}}} = 1 - z^{-1}$$

This is the equivalent of the derivative in the DT domain

NTF in the frequency domain

$$STF(z) = z^{-1}$$

$$NTF(z) = 1 - z^{-1} \qquad z \Leftarrow e^{j\omega T} \qquad \text{where: } T = \frac{1}{f_s}$$

$$NTF(j\omega) = 1 - e^{-j\omega T} = e^{-\frac{j\omega T}{2}} \left(e^{\frac{j\omega T}{2}} - e^{-\frac{j\omega T}{2}} \right)$$

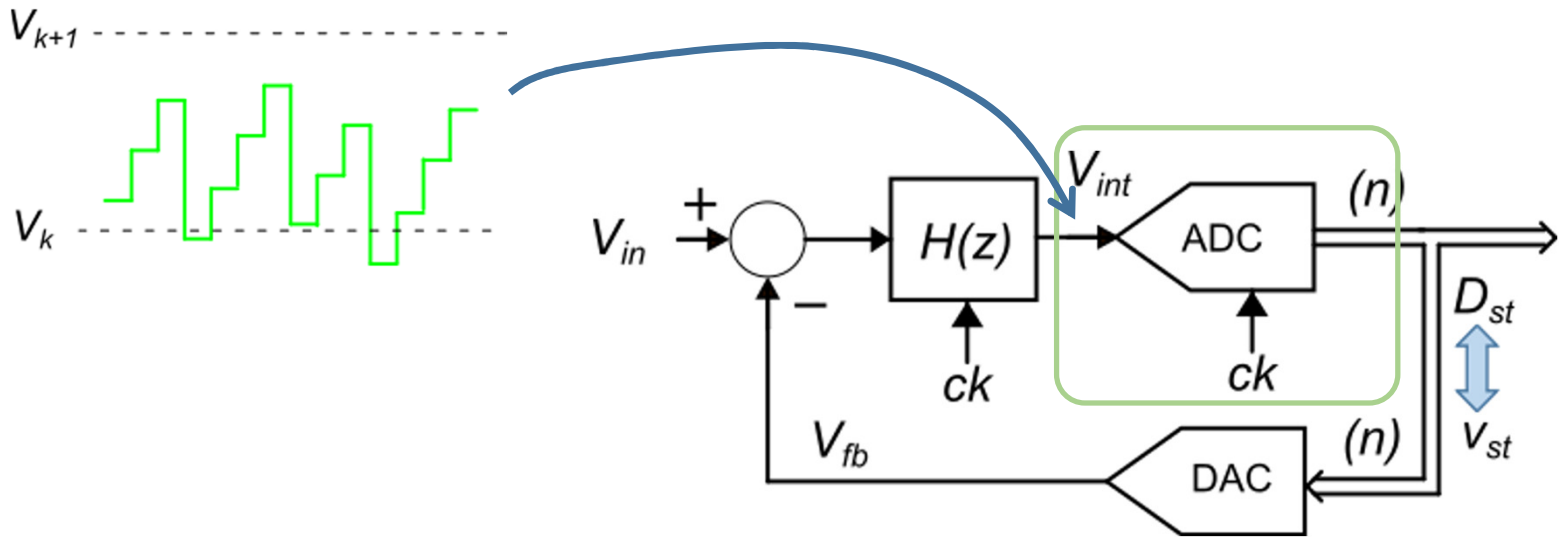
$$NTF(j\omega) = e^{-\frac{j\omega T}{2}} \cdot 2j \sin\left(\frac{\omega T}{2}\right) \qquad \omega = 2\pi f$$

$$NTF(j\omega) = e^{-j\pi fT} \cdot 2j \sin(\pi fT)$$

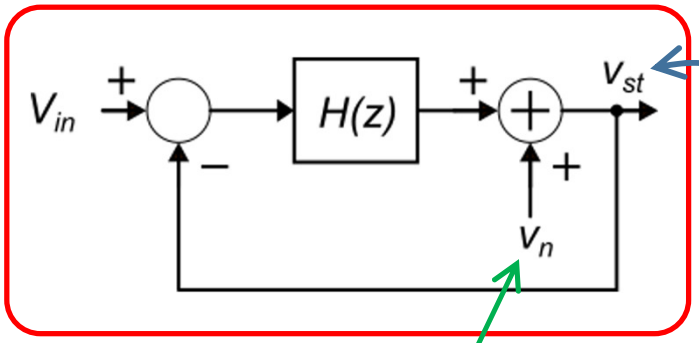
Output spectral density of the quantization noise

The uniform PSD model of the quantization noise is acceptable because the modulator continuously changes the input of the original ADC, sweeping across the whole range [-Δ/2, +Δ/2] of the quantization noise.

For more accurate analysis of second order effects, the limits of the uniform PSD model should be taken into account.

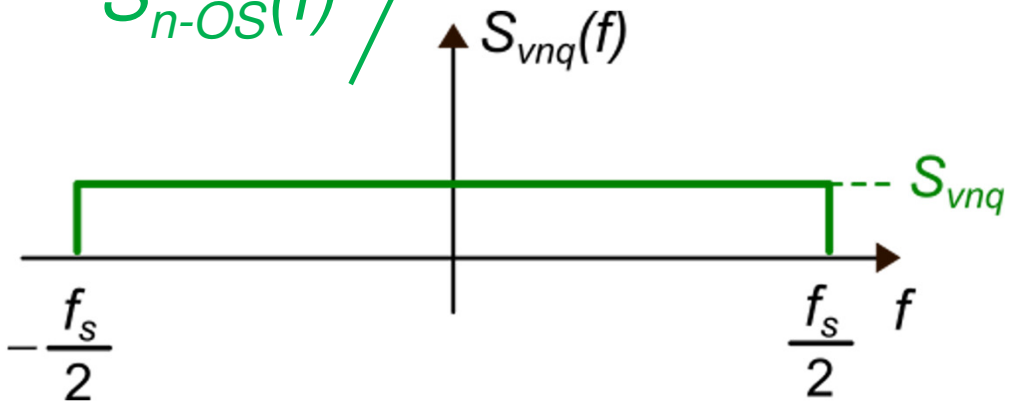


Quantization noise PSD at the output of the Δ–Σ modulator



$$NTF(j\omega) = e^{-j\pi fT} \cdot 2j\sin(\pi fT)$$

$$S_{n-DS}(f) = S_{n-OS}\left|NTF(f)\right|^2$$

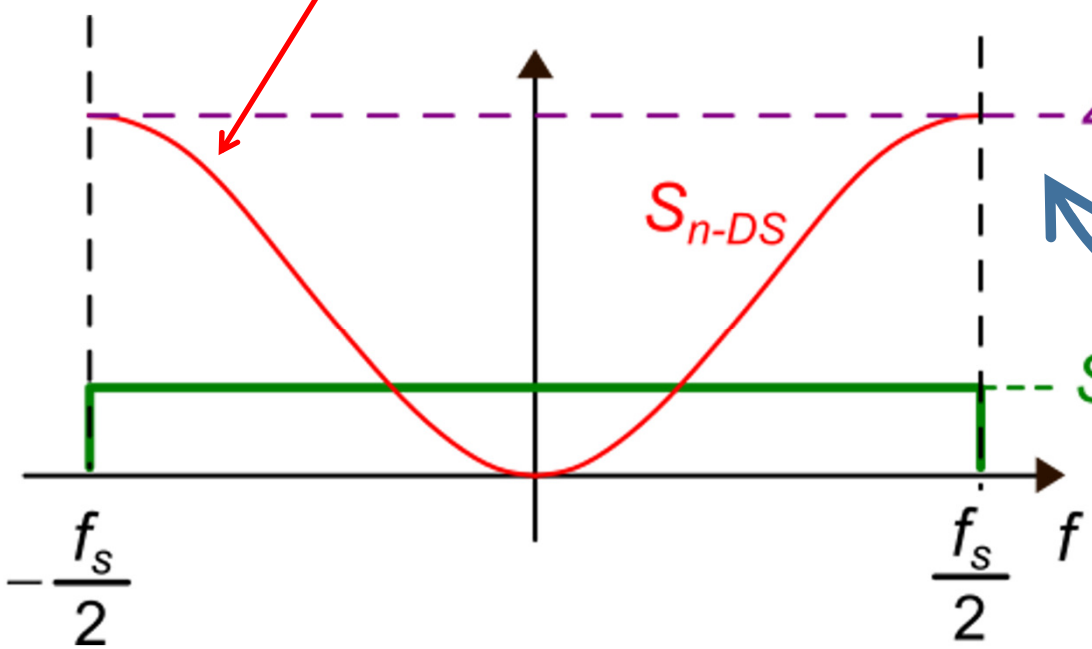


Recall: $T = \frac{1}{f_S}$

$$S_{n-DS}(f) = S_{n-OS} \cdot 4\sin^2\left(\pi\frac{f}{f_S}\right)$$

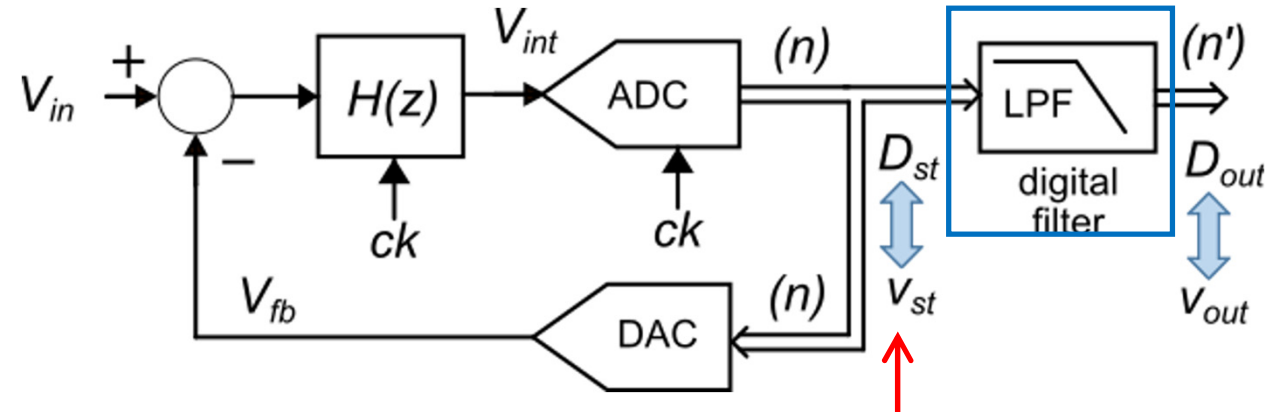
Quantization noise PSD at the output of the Δ–Σ modulator

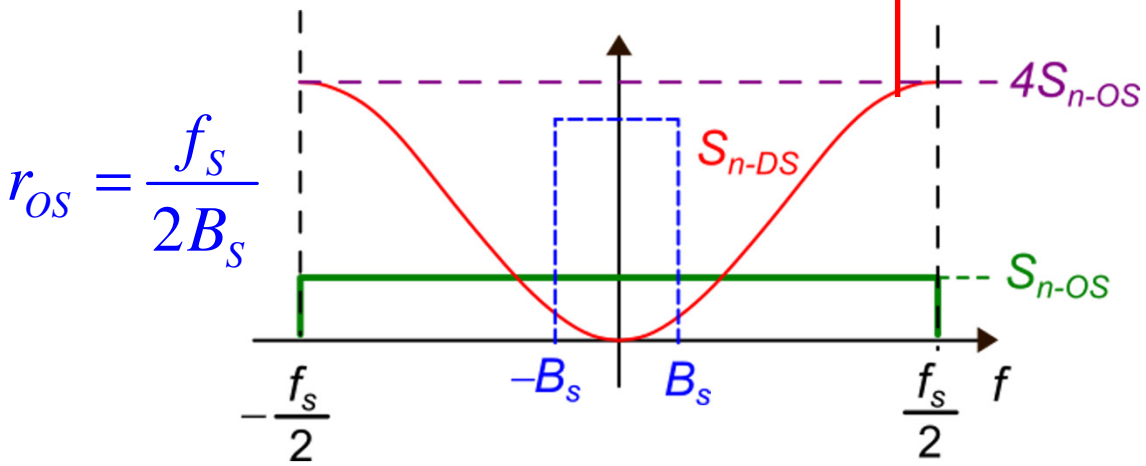
$$S_{n-DS}(f) = S_{n-OS} \cdot 4\sin^2\left(\pi \frac{f}{f_S}\right)$$



for $f=f_S/2$, the argument of $\sin^2$ is $\pi/2$

Output noise power in the Delta-Sigma ADC





$$r_{OS} = \frac{f_S}{2B_S}$$

$$S_{n-DS}(f) = S_{n-OS} \cdot 4\sin^2\left(\pi \frac{f}{f_S}\right)$$

$$\left\langle v_{n-out}^2 \right\rangle = \int_{-B_S}^{B_S} S_{n-DS}(f)\,df$$

$$\left\langle v_{n-out}^2 \right\rangle = S_{n-OS} \int_{-B_S}^{B_S} 4\sin^2\left(\pi \frac{f}{f_S}\right) df$$

$$\sin\left(\pi \frac{f}{f_S}\right) \cong \pi \frac{f}{f_S} \qquad f << f_S$$

$$\left\langle v_{n-out}^2 \right\rangle \cong S_{n-OS} \int_{-B_S}^{B_S} 4\left(\pi \frac{f}{f_S}\right)^2 df$$

Output noise power in the Delta-Sigma ADC

$$\left\langle v_{n-out}^2 \right\rangle \cong S_{n-OS} \int_{-B_S}^{B_S} 4\left(\pi \frac{f}{f_S}\right)^2 df = S_{n-OS} 4\pi^2 \frac{1}{f_S^2} \int_{-B_S}^{B_S} f^2 df = S_{n-OS} \frac{4\pi^2}{f_S^2} \left[\frac{f^3}{3}\right]_{-B_S}^{B_S}$$

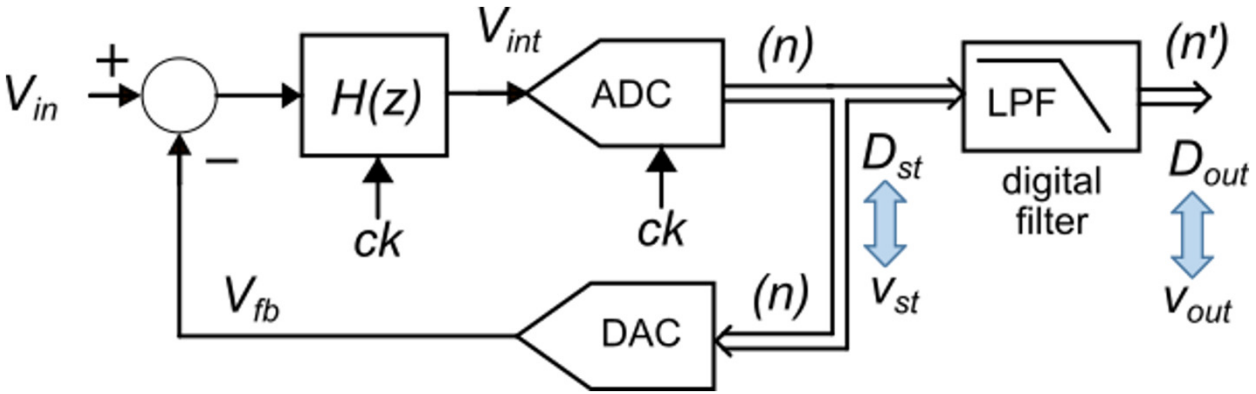
$$\left\langle v_{n-out}^2 \right\rangle \cong S_{n-OS} 4\pi^2 \frac{1}{f_S^2} \frac{2}{3} B_S^3 \qquad S_{n-OS} = \frac{S_{n-NR}}{r_{OS}} \qquad \left(r_{OS} = \frac{f_S}{2B_S} \right)$$

$$\left\langle v_{n-out}^2 \right\rangle \cong \frac{S_{n-NR}}{r_{OS}} 4\pi^2 \frac{1}{f_S^2} \frac{2}{3} B_S^3 \qquad 8B_S^3 = 2B_S \cdot (2B_S)^2$$

$$\left\langle v_{n-out}^2 \right\rangle \cong \frac{S_{n-NR} \cdot 2B_S}{r_{OS}} \frac{\pi^2}{3} \left(\frac{2B_S}{f_S}\right)^2 \frac{1}{r_{OS}^2} \qquad \left\langle v_{nq-NR}^2 \right\rangle$$

$$\left\langle v_{n-out}^2 \right\rangle \cong \left\langle v_{nq-NR}^2 \right\rangle \frac{\pi^2}{3} \frac{1}{r_{OS}^3}$$

Resolution increment in the first-order Δ–Σ ADC



$$n_2 - n_1 = \frac{1}{2}\log_2\left(\frac{\langle v_{n1}^2\rangle}{\langle v_{n2}^2\rangle}\right)$$

$$\left(\frac{\langle v_{n1}^2\rangle}{\langle v_{n2}^2\rangle}\right) = \frac{\langle v_{nq-NR}^2\rangle}{\langle v_{nq-NR}^2\rangle \frac{\pi^2}{3}\frac{1}{r_{OS}^3}} = r_{OS}^3\frac{3}{\pi^2}$$

$$n' - n = \frac{1}{2}\log_2\left(r_{OS}^3\frac{3}{\pi^2}\right)$$

$$n' - n = \frac{3}{2}\log_2(r_{OS}) - 0.86$$

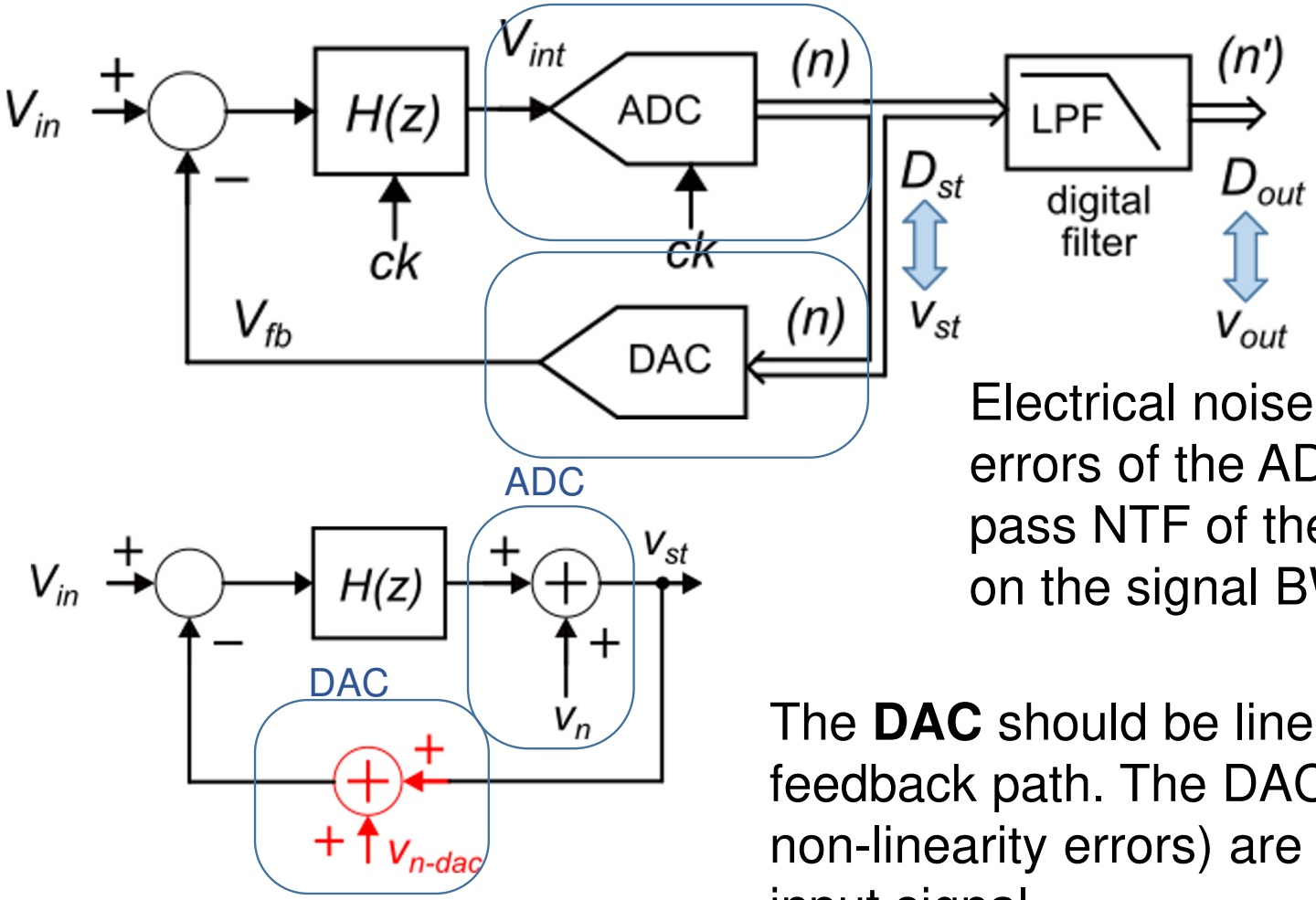
$$\frac{1}{2}\log_2\left(\frac{3}{\pi^2}\right)$$

Resolution increment in the first order Δ–Σ ADC

$$n' - n = \frac{3}{2}\log_2\left(r_{OS}\right) - 0.86$$

Every increment of r_{OS} by a factor of 2 produces a resolution gain of 1.5 bits.
This gain was only 1/2 bit in the pure oversampling ADC

ADC and DAC non idealities in Δ–Σ ADC



Electrical noise, offset and non-linearity errors of the ADC are shaped by the high pass NTF of the modulator, then the effect on the signal BW is negligible.

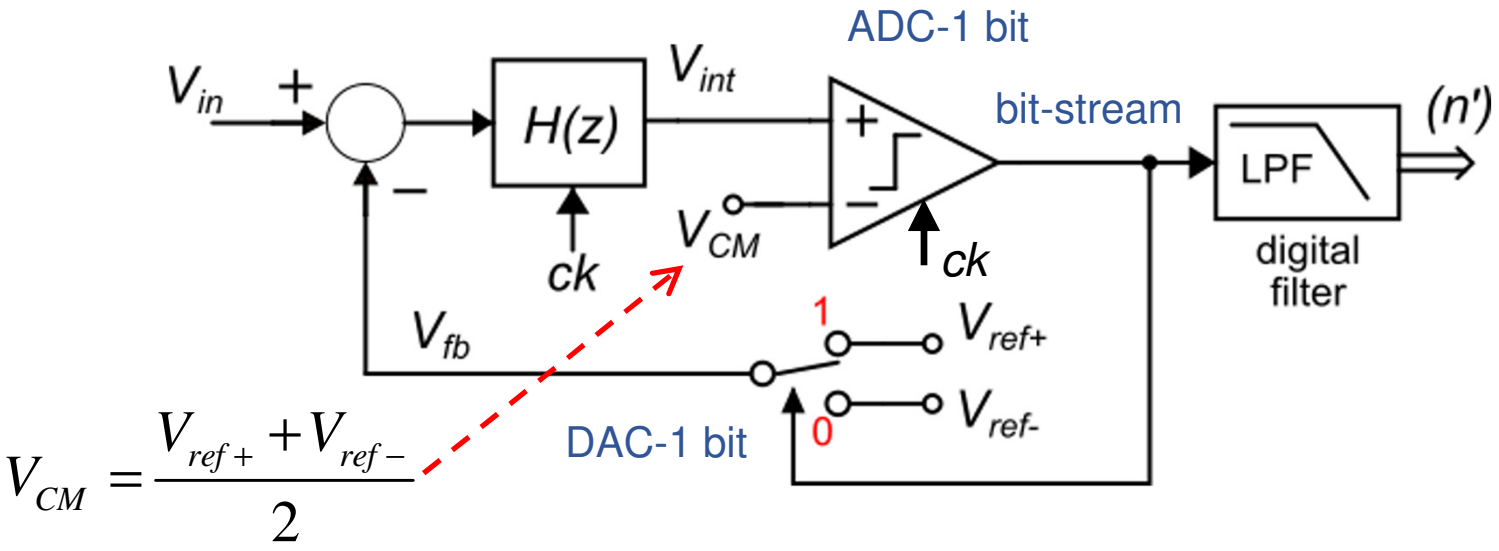
The **DAC** should be linear because it is in the feedback path. The DAC noise (that includes also non-linearity errors) are simply summed-up to the input signal.

Single-bit Δ–Σ ADC

As we have seen, the DAC linearity is a main issue of the Δ–Σ approach

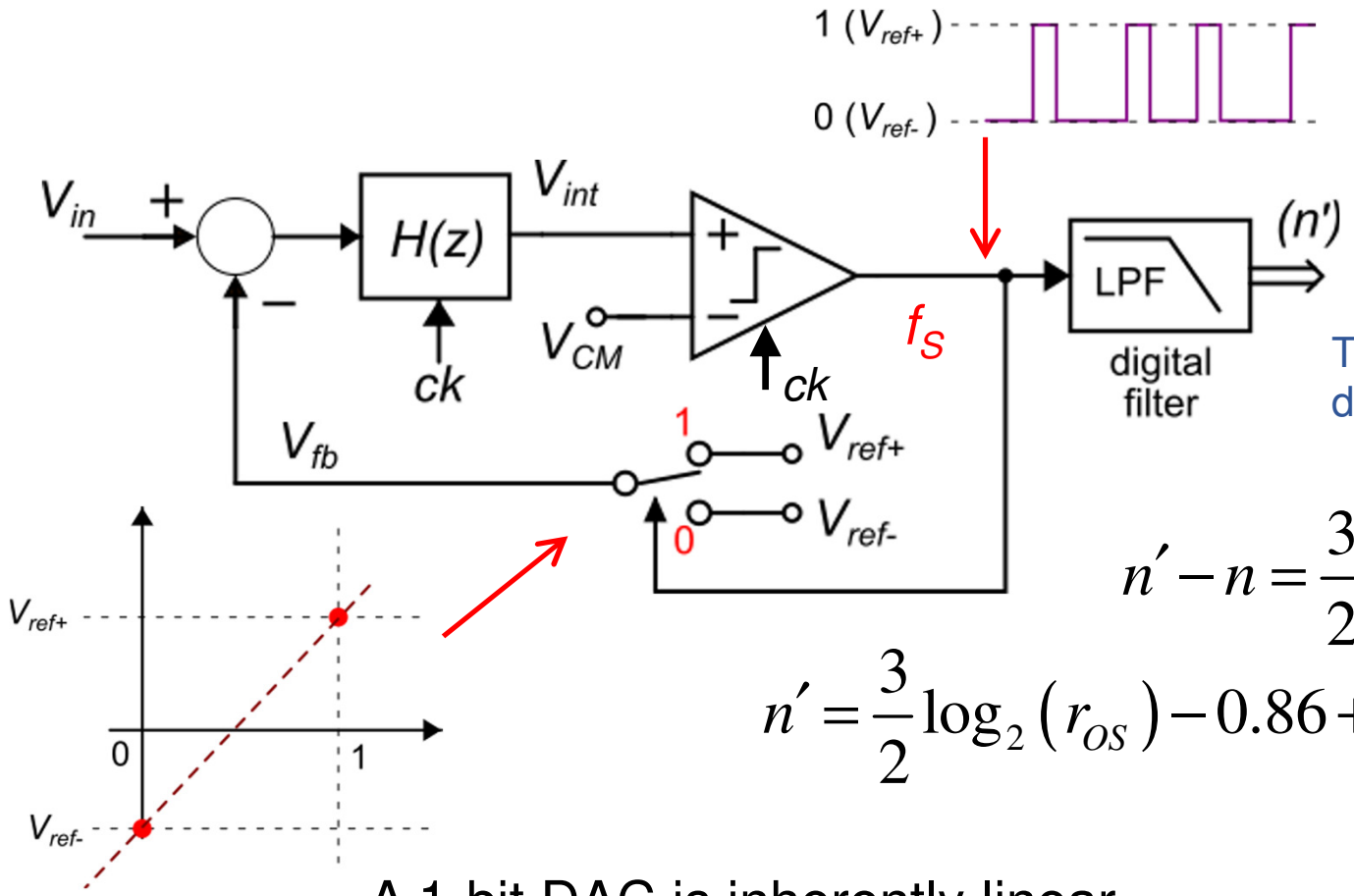
A very elegant and widely used solution is the single bit Δ–Σ ADC

In the single bit D-S ADC the internal Nyquist-rate ADC is a single bit quantizer, i.e., a comparator



Single-bit Δ–Σ ADC

[Tutorial Analog-Devices Delta-Sigma]



$$n' - n = \frac{3}{2}\log_2(r_{OS}) - 0.86$$

$$n' = \frac{3}{2}\log_2(r_{OS}) - 0.86 + 1$$

A 1-bit DAC is inherently linear

Example of DS ADC with 1-bit quantizer

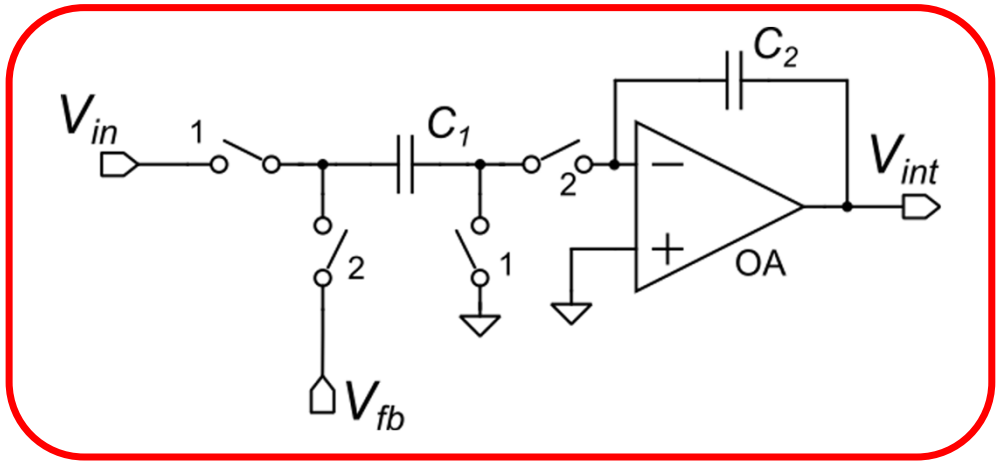
$$n' = \frac{3}{2}\log_2\left(r_{os}\right) - 0.86 + 1$$

r_{OS}=OSR=128

$$n' = \frac{3}{2} \times 7 - 0.86 + 1 = 10.8 \text{ bits}$$

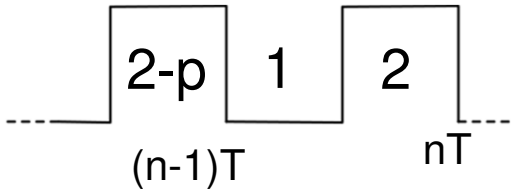
H(z) implementation (Single ended)

Classical, "parasitic insensitive" Switched Capacitor Integrator

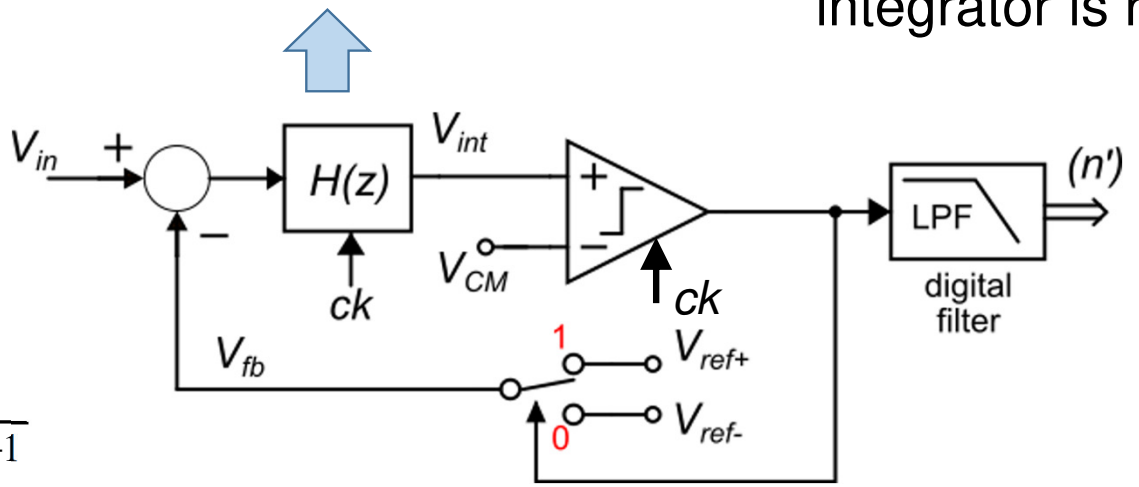


Note: electrical noise and distortion of the DT integrator are not shaped by the NTF: careful design of the integrator is required.

$$V_{\text{int}}^{(2)} = V_{\text{int}}^{(1)} + \frac{C_1}{C_2}\left(V_{in}^{(1)} - V_{fb}^{(2-p)}\right)$$



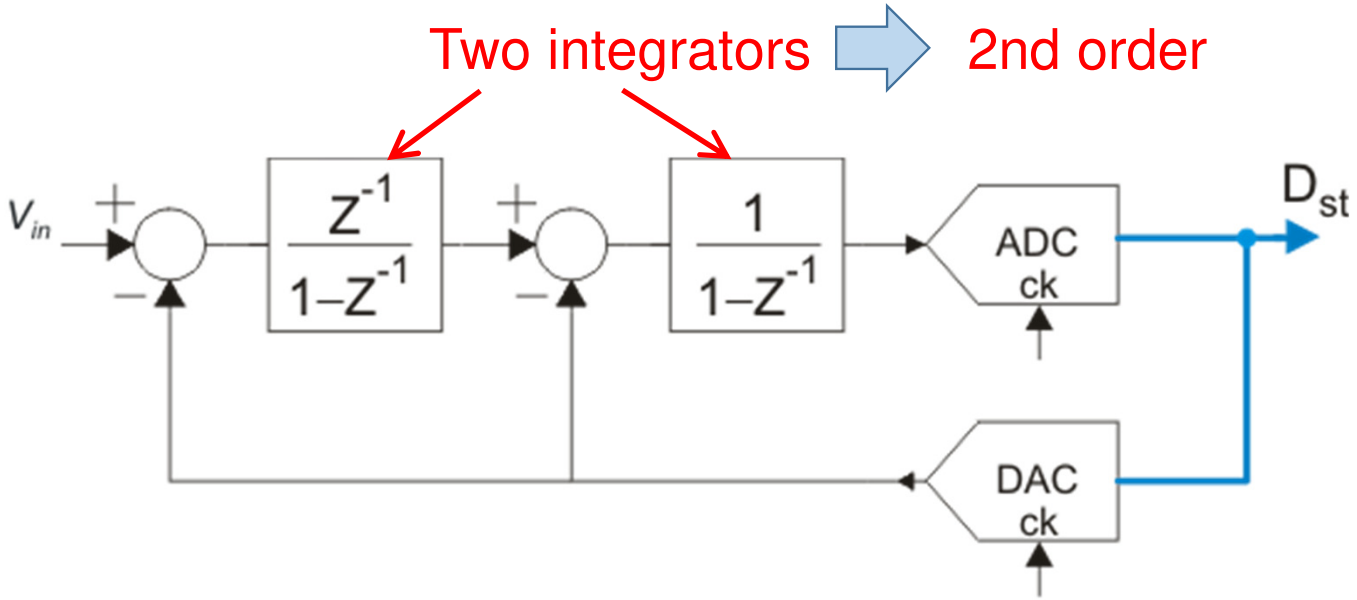
$$H(z) = \frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}$$



Higher order Δ–Σ ADCs

$$n' - n \approx \frac{5}{2}\log_2(r_{OS})$$

Example: second-order ADC



Advantage: 2.5 bits are gained doubling the OSR (instead of 1.5 bits).
Same final resolution with a much smaller OSR
The 2nd order D-S ADC is a very popular converter for sensor interfaces.