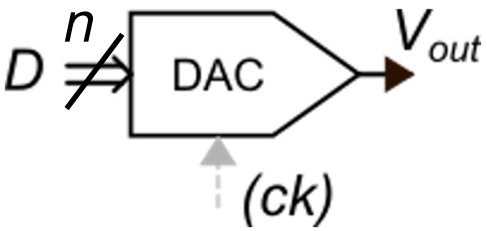
Digital to Analog Converters



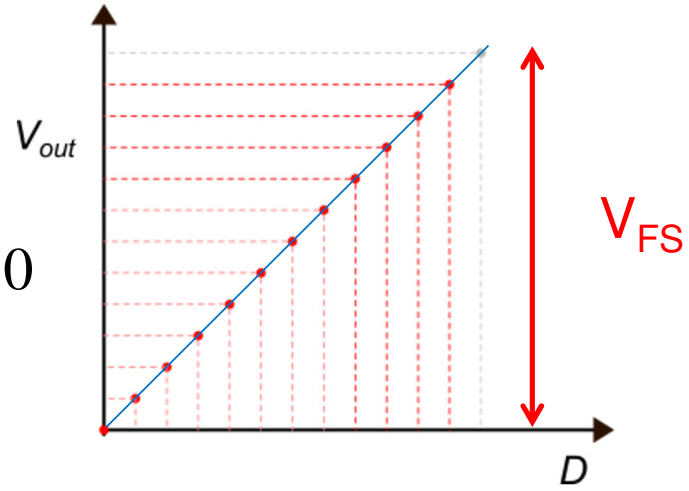
n= resolution

Input: digital code
Output: analog signal
A **clock** can be present for synchronization reasons or to avoid glitches during data update

Ideal function: $V_{out} = V_{MIN} + \frac{V_{FS}}{2^n} D$

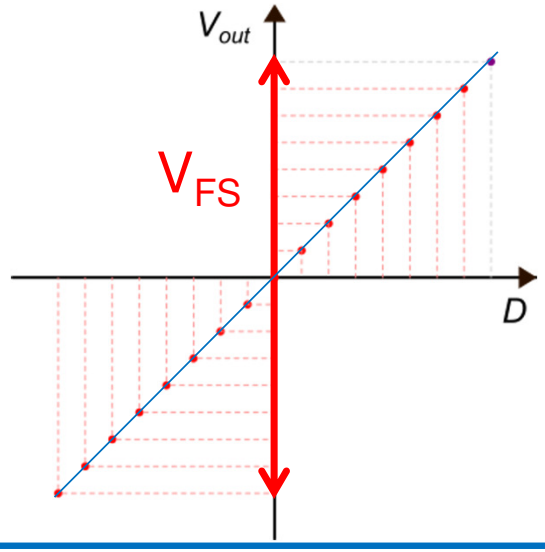
n= nominal resolution (in number of bits)

unipolar output range



$V_{MIN} = 0$

bipolar output range



D unsigned:

$$V_{MIN} = \frac{V_{FS}}{2}$$

D signed
e.g. two's complement:

$V_{MIN} = 0$

DAC applications

- Digital to analog signal reconstruction: e.g. audio and video signals, actuator control (e.g. control of motors, solenoids, piezoactuators
- Direct Digital Synthesis (DDS) of waveforms for telecommunications, sensor excitation, etc.
- Trimming of analog blocks (e.g. offset nulling)
- Feedback components in ADCs

DAC performance parameters

DAC errors

Quantization error

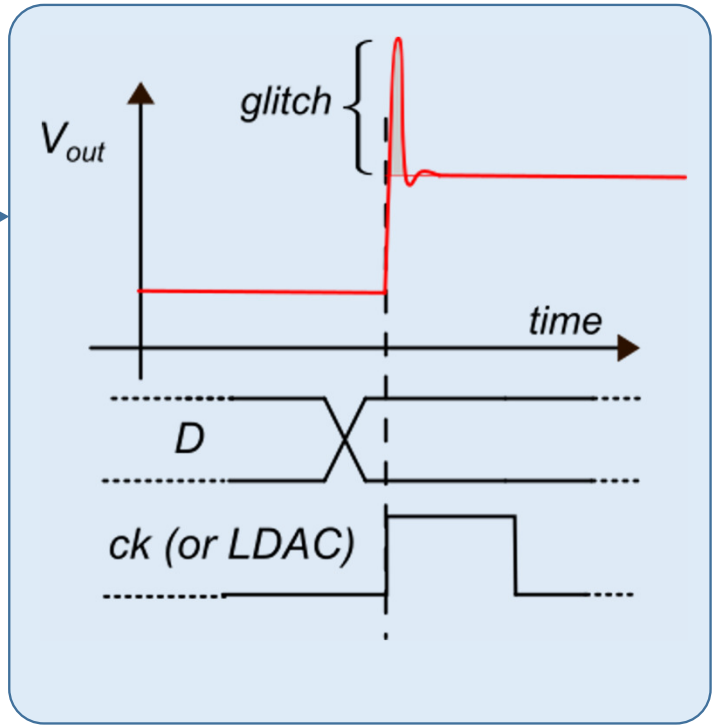
Offset
Gain
Non-linearity { INL, DNL }

Noise

Energy of the glitches $(\mathrm{nV} \cdot \mathrm{s})$

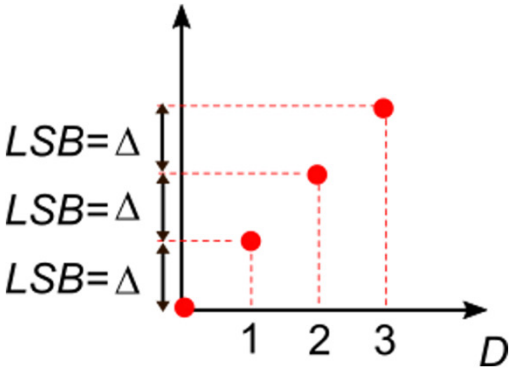
DAC speed: settling time, sample per seconds (sps),

Power consumption



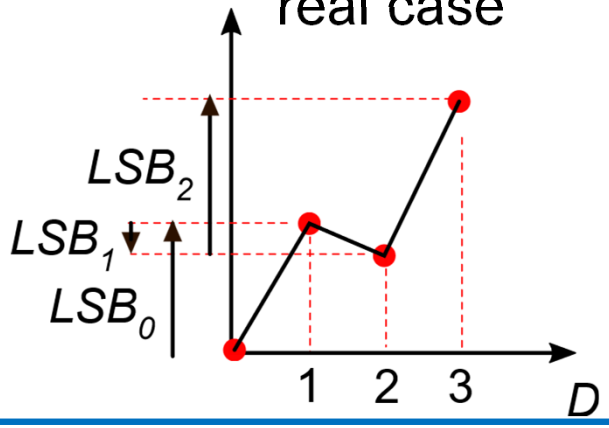
INL, DNL

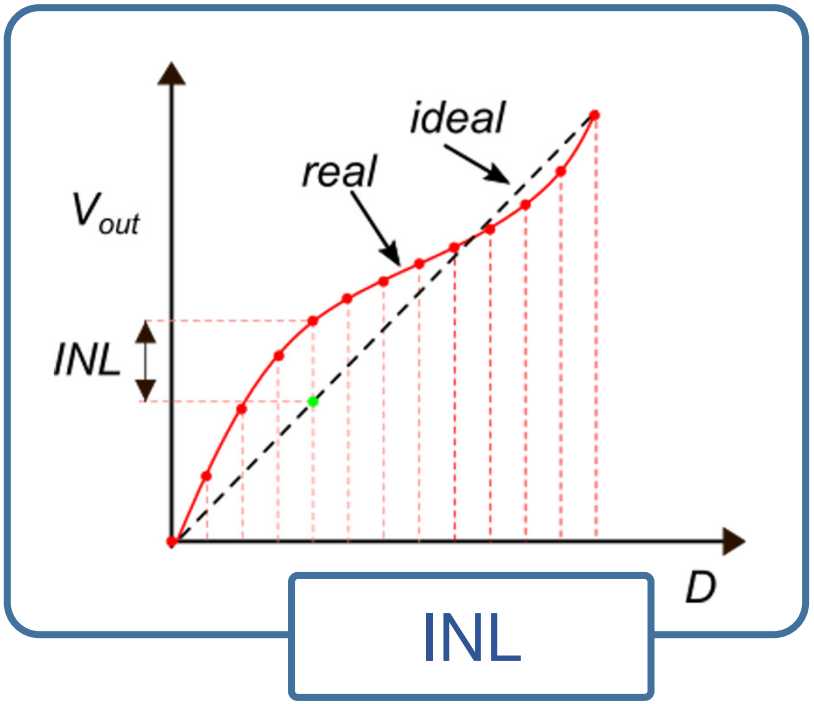
Ideal case
(absence of non-linearity errors)



$$LSB \equiv \Delta = \frac{V_{FS}}{2^n}$$

real case





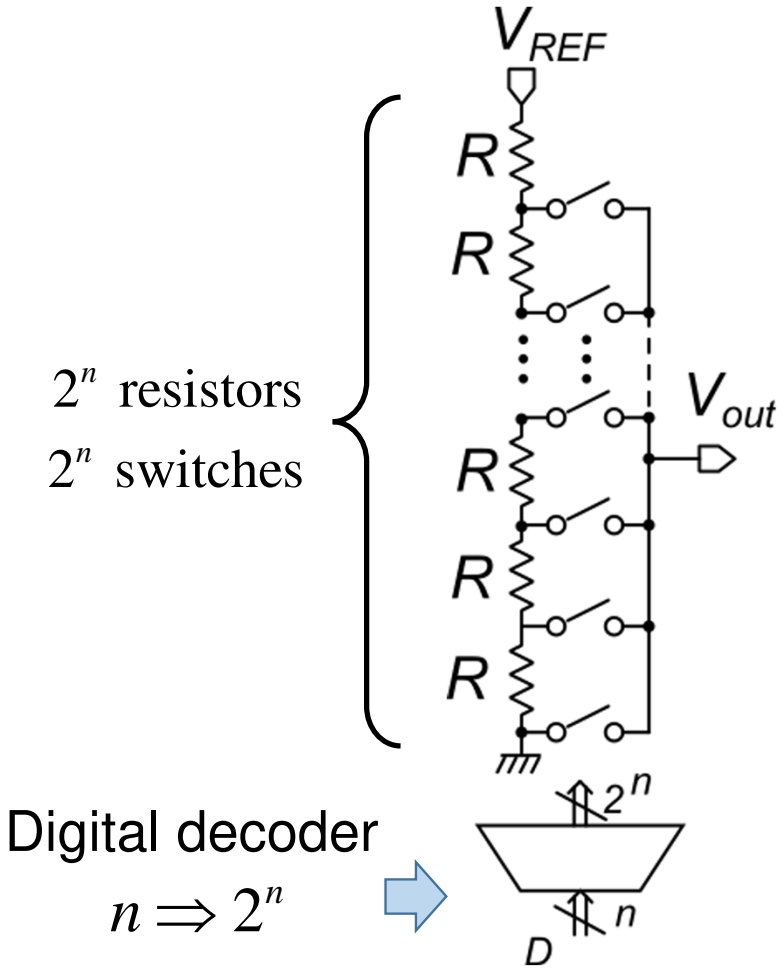
$$DNL_k = \frac{LSB_k - LSB}{LSB} \qquad (Unit = LSB)$$

$|DNL|>$ 1 LSB: probable non-monotonicity

DAC Architectures

	Pros	Cons
R-2-R ladder	Reduced number of resistors Resistors of similar value	Potentially non-monotonic Suffer from the on-resistance of the switches
Resistor String	Guaranteed monotonic Low power consumption	Number of resistors increases exponentially with resolution
Current Steering	Very fast. No need for resistors. Can be designed to be always monotonic	Current output. Flicker Noise
Switched Capacitors	Optimal power vs speed trade-off	The output may be not available in the whole clock cycle. Large glitches

DAC resistor string

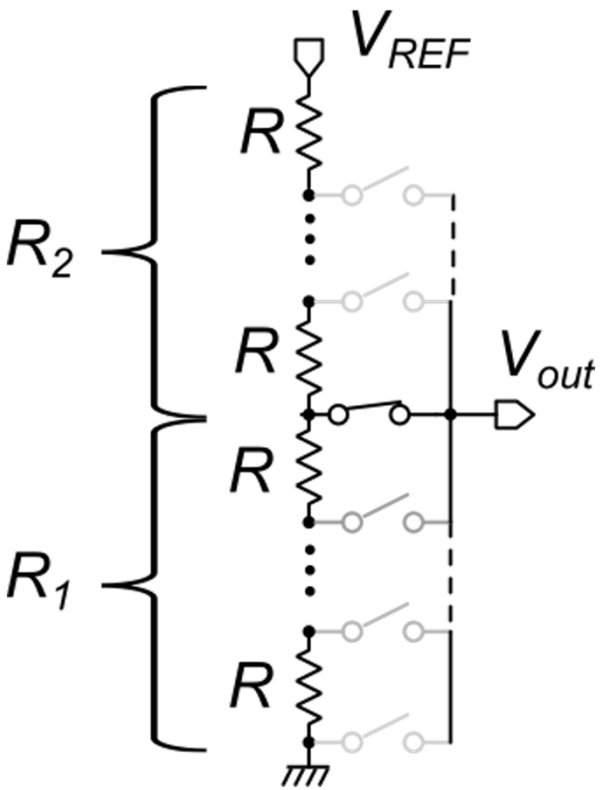


For any value of code D, only one switch at a time is on, selecting one of the 2^n voltage levels produced by the resistive divider

If code D turns on a certain switch, code D+1 turns on the switch placed in position up, then the output voltage can only grow

Monotonicity is guaranteed

INL in a resistor string: a simple estimate



$$V_{out} = V_{ref}\frac{R_1}{R_1+R_2}$$

We consider a code that, in the ideal case, select the mid voltage: $\Rightarrow V_{out-id} = \frac{V_{REF}}{2}$

Ideally $R_1 = R_2$

In a real case: $R_1 = \overline{R} + \frac{\Delta R}{2}, \quad R_2 = \overline{R} - \frac{\Delta R}{2}$

$$V_{out} = V_{ref}\frac{R_1}{R_1+R_2} = V_{ref}\frac{\overline{R}+\frac{\Delta R}{2}}{2\overline{R}} = \frac{V_{ref}}{2}\left(1+\frac{\Delta R}{2\overline{R}}\right)$$

$$\begin{cases} V_{INL} = \frac{V_{ref}}{2}\frac{\Delta R}{2\overline{R}} \\ LSB = \frac{V_{REF}}{2^n} \end{cases}$$

$$\frac{V_{INL}}{LSB} = \frac{2^n}{V_{ref}}\frac{V_{ref}}{2}\frac{\Delta R}{2\overline{R}} = 2^{n-2}\frac{\Delta R}{\overline{R}}$$

INL and resistor matching

$$\frac{V_{INL}}{LSB} = 2^{n-2}\frac{\Delta R}{\overline{R}}$$

In an n-bit DAC, to have an |*INL*|<1 LSB, the relative matching errors should satisfy:

$$2^{n-2}\frac{\Delta R}{\overline{R}} < 1 \quad \Rightarrow \quad \frac{\Delta R}{\overline{R}} < \frac{1}{2^{n-2}}$$

Example: 12 bit DAC:

$$\frac{\Delta R}{\overline{R}} < \frac{1}{2^{10}} \cong 10^{-3}$$

Feasible, with large area occupation

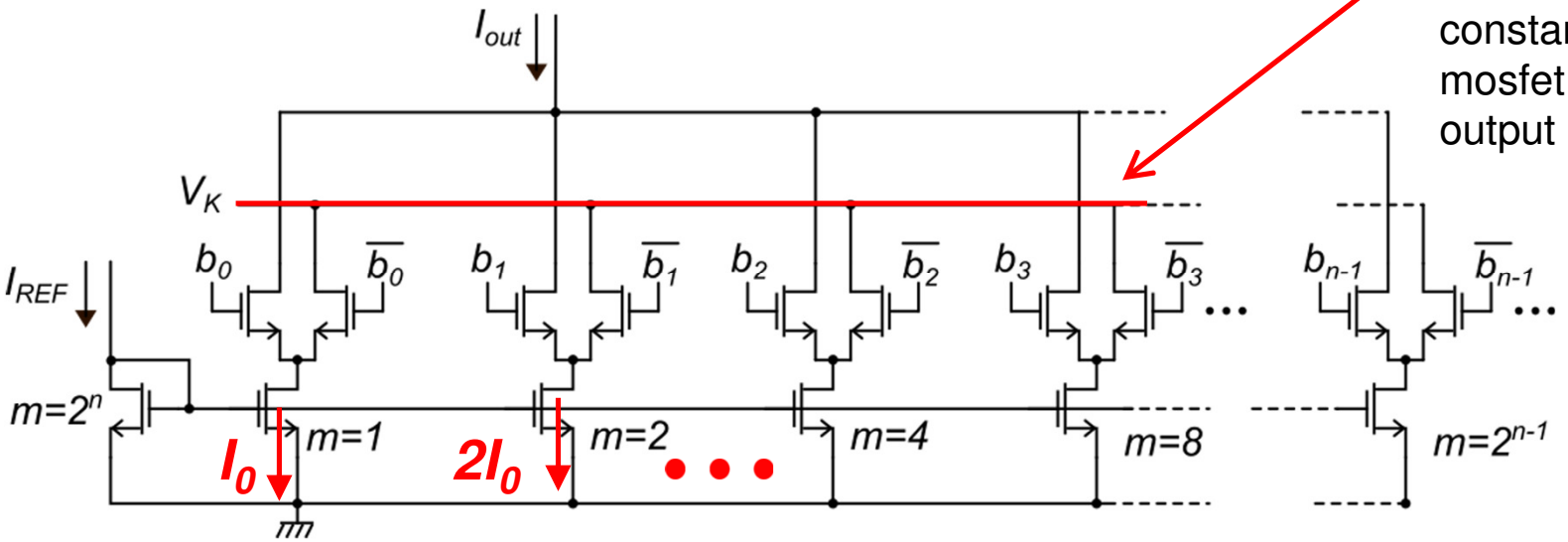
Example: 16 bit DAC:

$$\frac{\Delta R}{\overline{R}} < \frac{1}{2^{14}} \cong 6\times 10^{-5}$$

Unfeasible. Requires complicated post-production trimming or self-calibration procedures

Current Steering DAC

The current of mosfets that are not routed to the output (their bit is 0), is not interrupted but is routed to a constant voltage (V_k) to keep the mosfet ready to be connected to the output in a short time



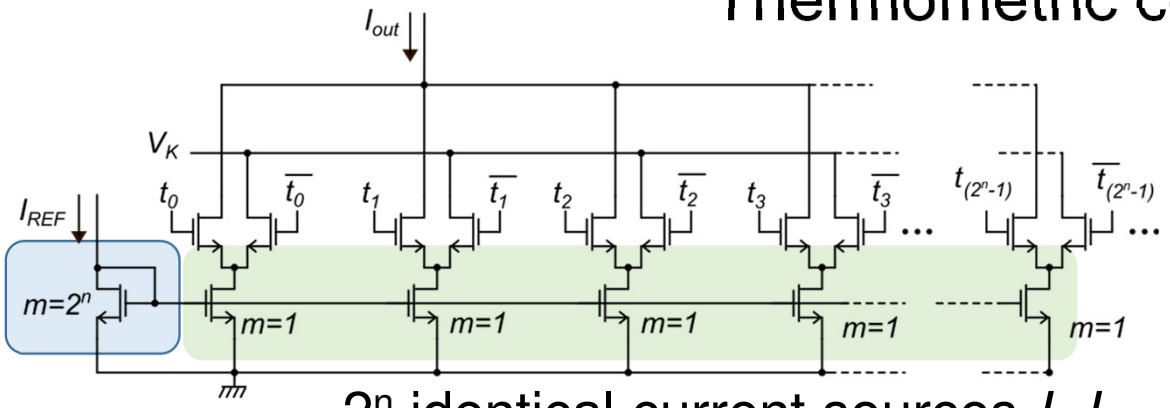
$$I_0 = \frac{I_{REF}}{2^n}$$

$$I_{out} = I_0 \sum b_k 2^k = \frac{I_{REF}}{2^n} \sum b_k 2^k = \frac{I_{REF}}{2^n} D \qquad D = \sum b_k 2^k$$

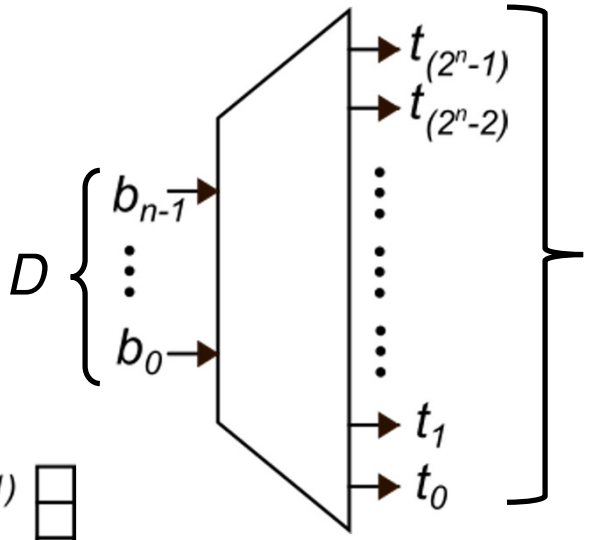
It can be made monotonic-guaranteed by driving the 2^n mosfets of the array with thermometric coding

It suffers from the same INL problem of the resistor string DAC

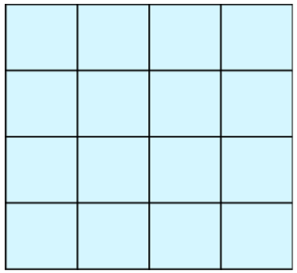
Thermometric coding



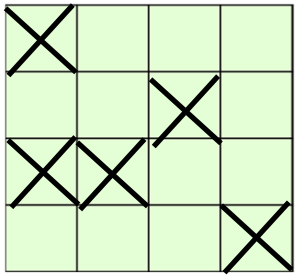
2^n identical current sources $I=I_0$



randomly placed into the matrix

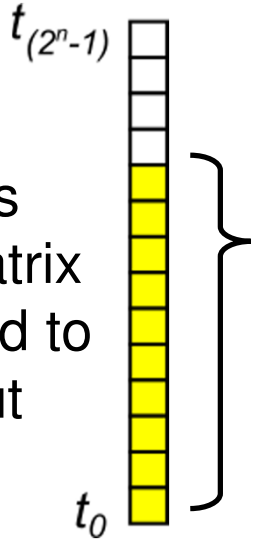


2^n devices (always in parallel)



2^n devices

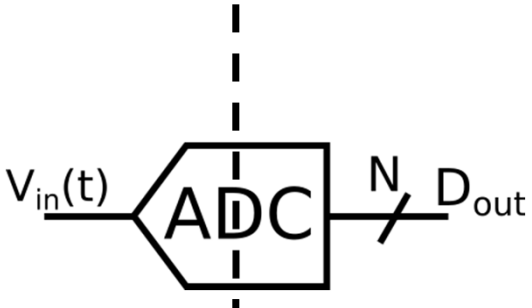
D devices of the matrix are routed to the output



The first *D* lines are set to 1

If D is incremented by one, one more device is routed to the output: Iout increases. Monotonicity is guaranteed

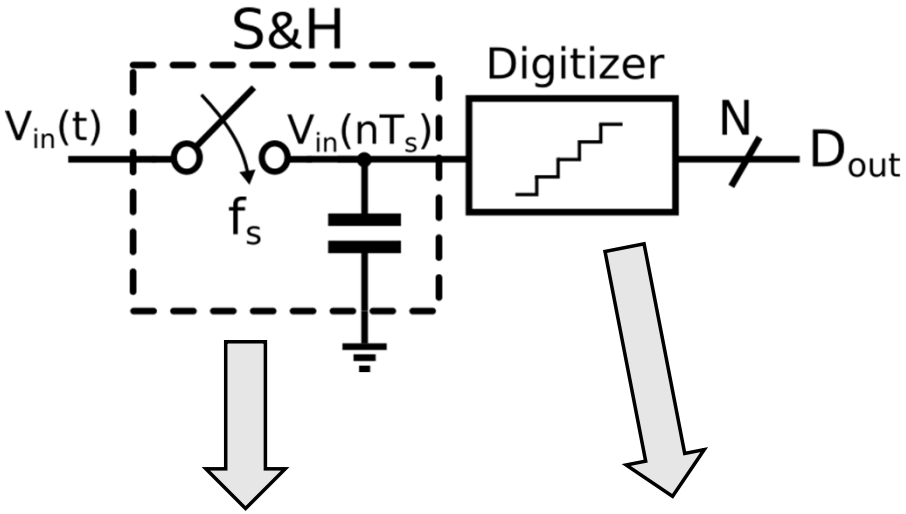
Analog to Digital Converters



Time-continuous
Infinite levels

Time-discrete
Finite number of levels

Analog-to-Digital converter



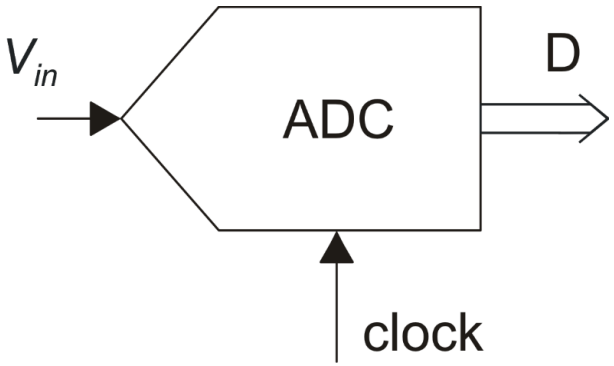
Sampling:
Nyquist-Shannon sampling theorem
Aliasing

Quantization:
Quantization noise

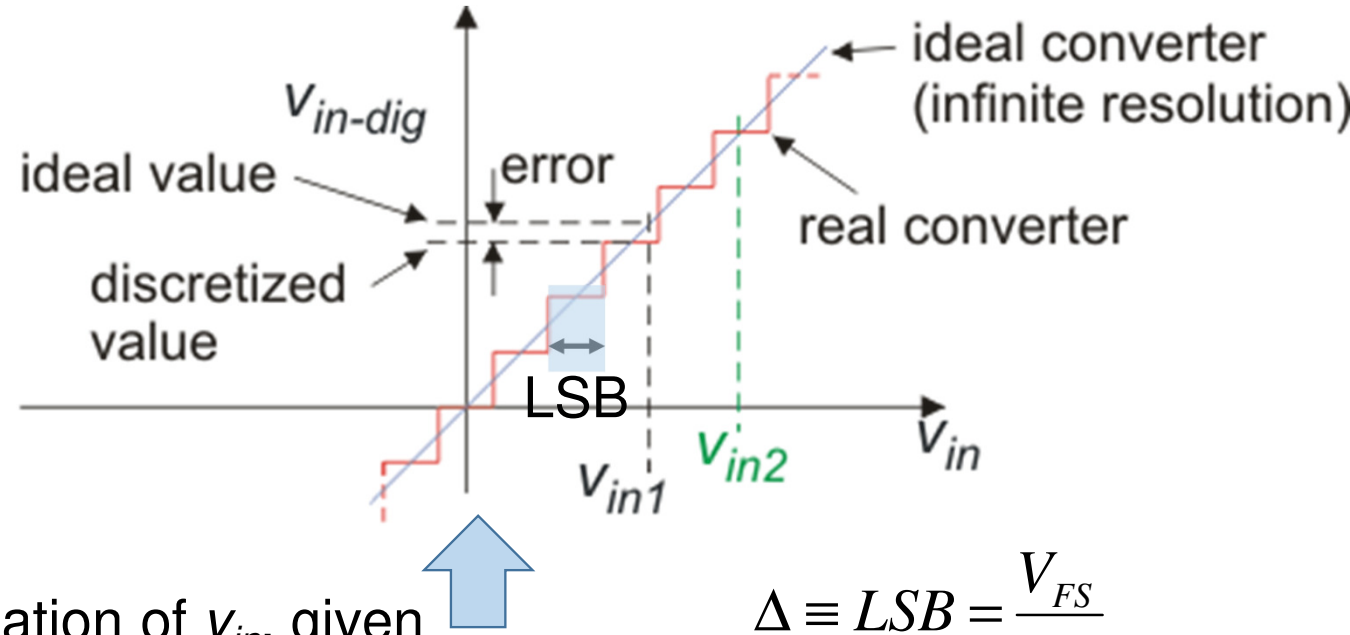
ADC applications

- Measurements and data acquisition
- Industrial (control systems, PLCs, …)
- Commercial electronics (mobile phones, video and audio devices, microcontrollers …)
- High-speed communications (data link, IF conversion…)

Analog to Digital Converters (ADCs)



The characteristic of an n-bit ADC with no offset, gain, and non-linearity errors (only quantization errors)



It is useful to refer to the equivalent voltage of D

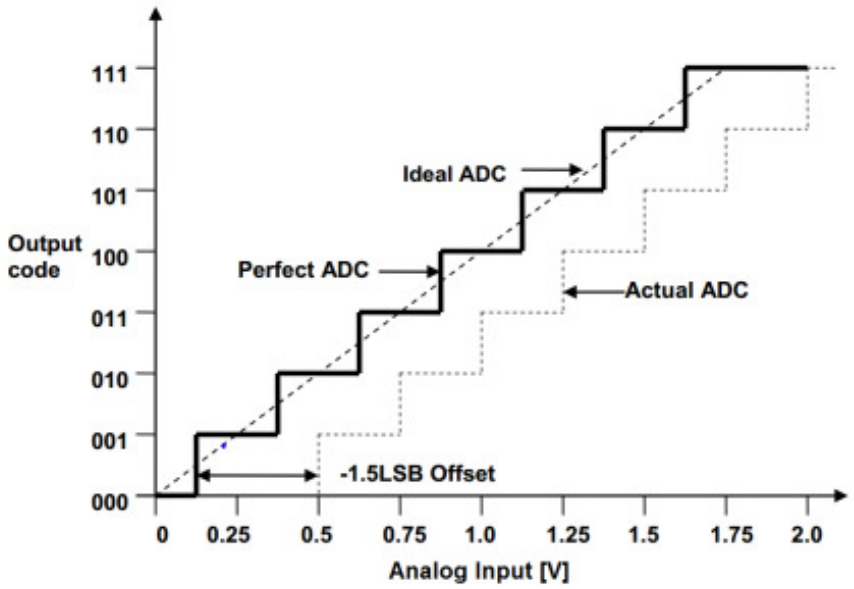
$$v_{in-dig} = V_{MIN} + \frac{V_{FS}}{2^n} D$$

$$\Delta \equiv LSB = \frac{V_{FS}}{2^n}$$

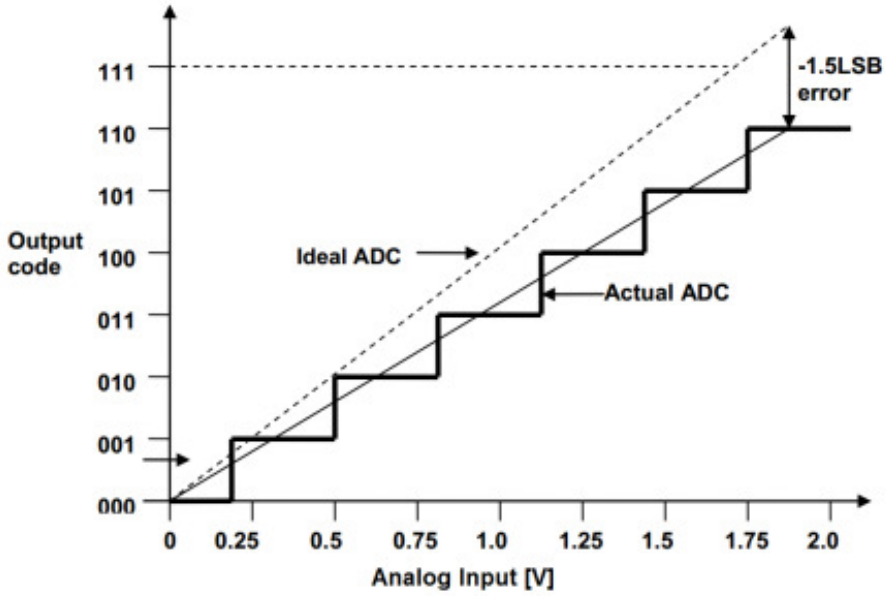
v_{in-dig} must be the best approximation of v_{in}, given the number of bit of D

ADCs – Static Parameters

- **Offset error:** difference between the actual ADC characteristic and the perfect ADC characteristic, evaluated at the zero transition



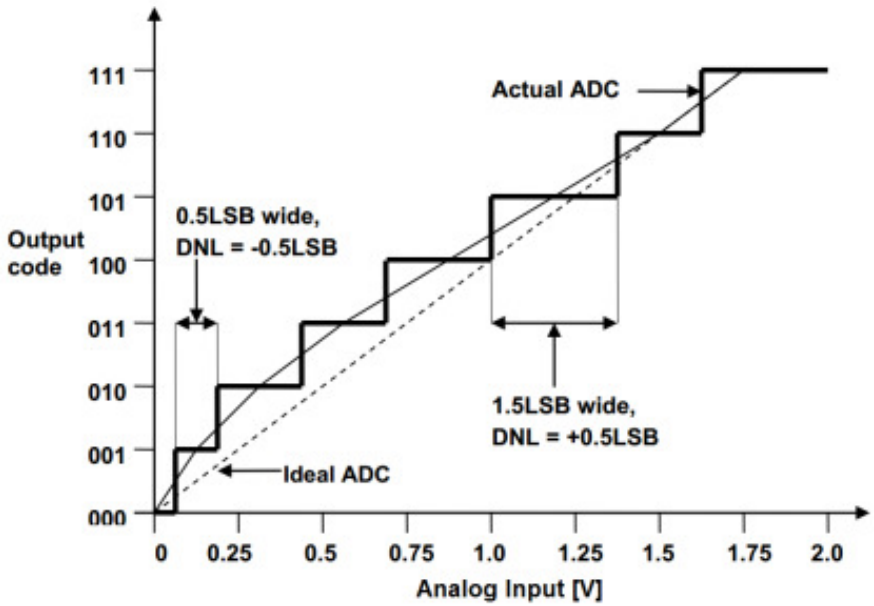
- **Gain error:** difference between the last step midpoint of the actual ADC and the last step midpoint of the ideal ADC, after the compensation of the offset error



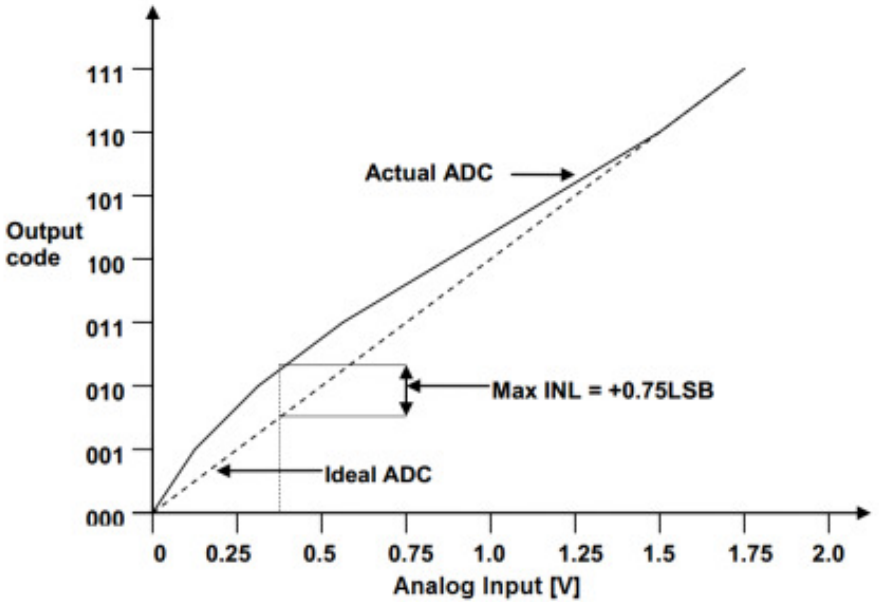
http://ww1.microchip.com/downloads/en/appnotes/atmel-8456-8-and-32-bit-avr-microcontrollers-avr127-understanding-adc-parameters_application-note.pdf

ADCs – Static Parameters

- **DNL error:** difference in the step width between the actual characteristic and the ideal one

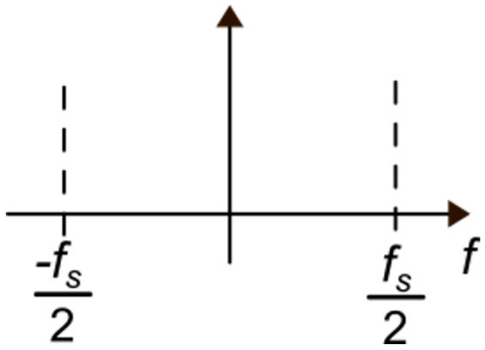


- **INL error:** vertical difference between the actual input-output characteristic and the ideal one, after the compensation of the offset and gain error

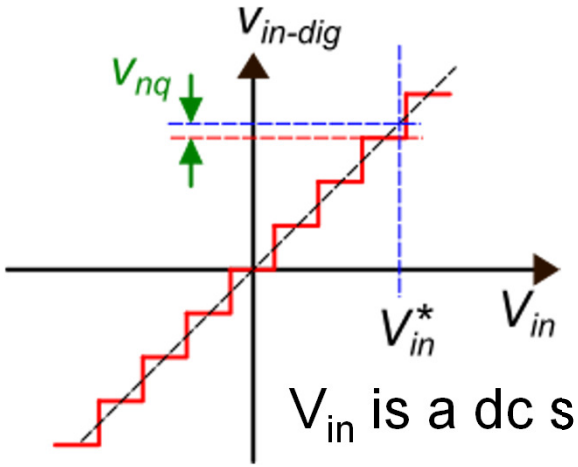


http://ww1.microchip.com/downloads/en/appnotes/atmel-8456-8-and-32-bit-avr-microcontrollers-avr127-understanding-adc-parameters_application-note.pdf

Quantization noise in the frequency domain

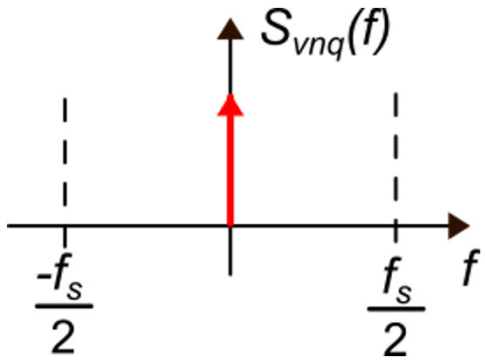


Since the ADC samples the input data, the output frequency domain is $[-f_s/2,+f_s/2]$

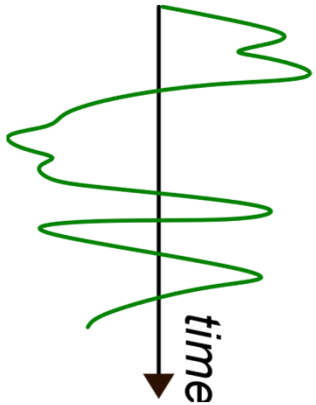


V_{in} is a dc signal

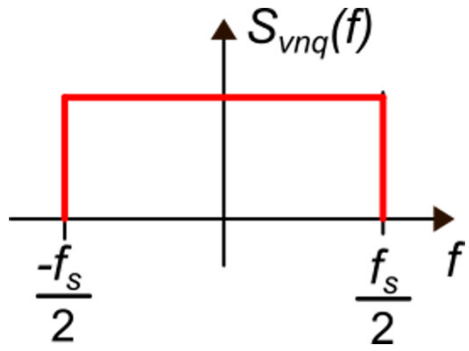
The v_{nq} spectrum is a Dirac delta



Two extreme cases

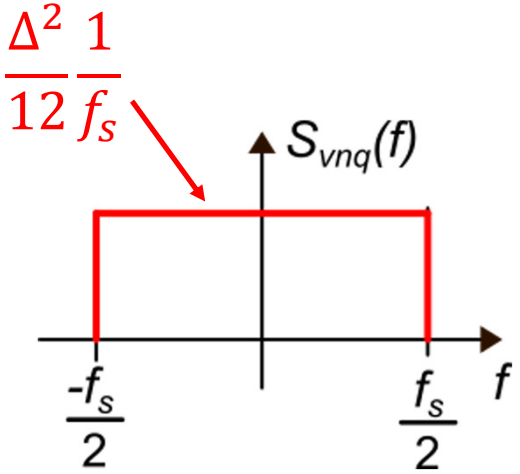


V_{in} is fast-varying signal of magnitude >> LSB



uniform distribution

The uniform power spectral density (PSD) model for the quantization noise



$$\Delta = \frac{V_{FS}}{2^N} = LSB$$

$$\left\langle v_{nq}^2 \right\rangle = \frac{\Delta^2}{12}$$

This model is very useful and simple **but should be applied with much care.**

In real cases, the quantization noise depends on the input signal, and so does its spectrum.

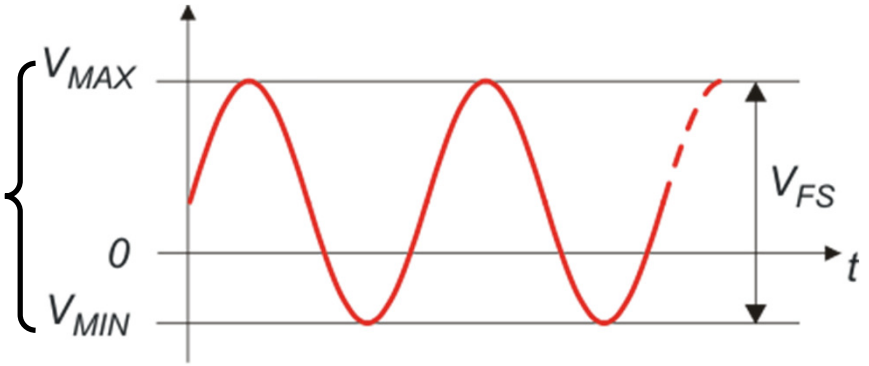
The uniform spectral density model is acceptable when the input signal has **magnitude** and/or **frequency** such that the output levels are changed in a **fast** and almost **random** way.

This happens when the average time spent by the signal on a single level is short (of the order of the sampling time).

Signal to Noise Ratio and resolution

$$SNR_{max} = \frac{P_{MAX}}{< v_n{}^2 >}$$

Input range of the ADC



$$P_{MAX} = \frac{V_{FS}^2}{8}$$

Considering only quantization noise: $\left\langle v_{nq}^2 \right\rangle = \frac{\Delta^2}{12}$

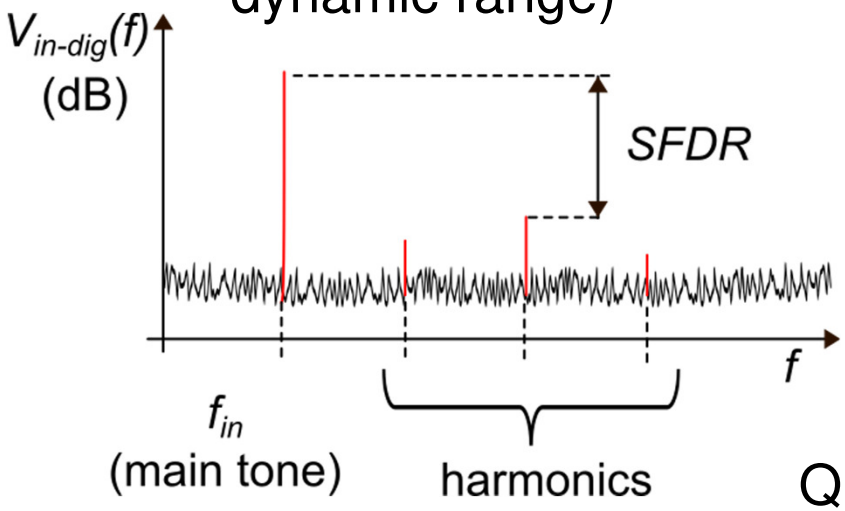
$$SNR = SQNR = \frac{V_{FS}^2}{8}\frac{12}{\Delta^2} = \frac{3}{2}\frac{V_{FS}^2}{\Delta^2}$$

$$\Delta = \frac{V_{FS}}{2^n} \qquad SQNR = \frac{V_{FS}^2}{2}\frac{3\cdot 2^{2n}}{V_{FS}^2} = \frac{3}{2}\cdot 2^{2n}$$

$$SQNR_{dB} = 10\log_{10}\left(SQNR\right) \cong 6.02n + 1.76$$

Effective Number Of Bits (ENOB)

Distortion and SFDR (spurious free dynamic range)



P_D=total power of the harmonics

$$SINAD = \frac{P_{MAX}}{\left\langle v_n^2 \right\rangle + P_D}$$

Also indicated with *SNDR*

Quantization and electrical noise

$$SQNR_{dB} = 10\log_{10}\left(SQNR\right) \cong 6.02n + 1.76$$

$$SINAD_{dB} \cong 6.02 \cdot ENOB + 1.76$$

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02}$$

Nyquist rate ADCs

N-bit ADC

- Direct conversion:
  - Flash converters

1 cycle of comparison
(fast but with low resolution)

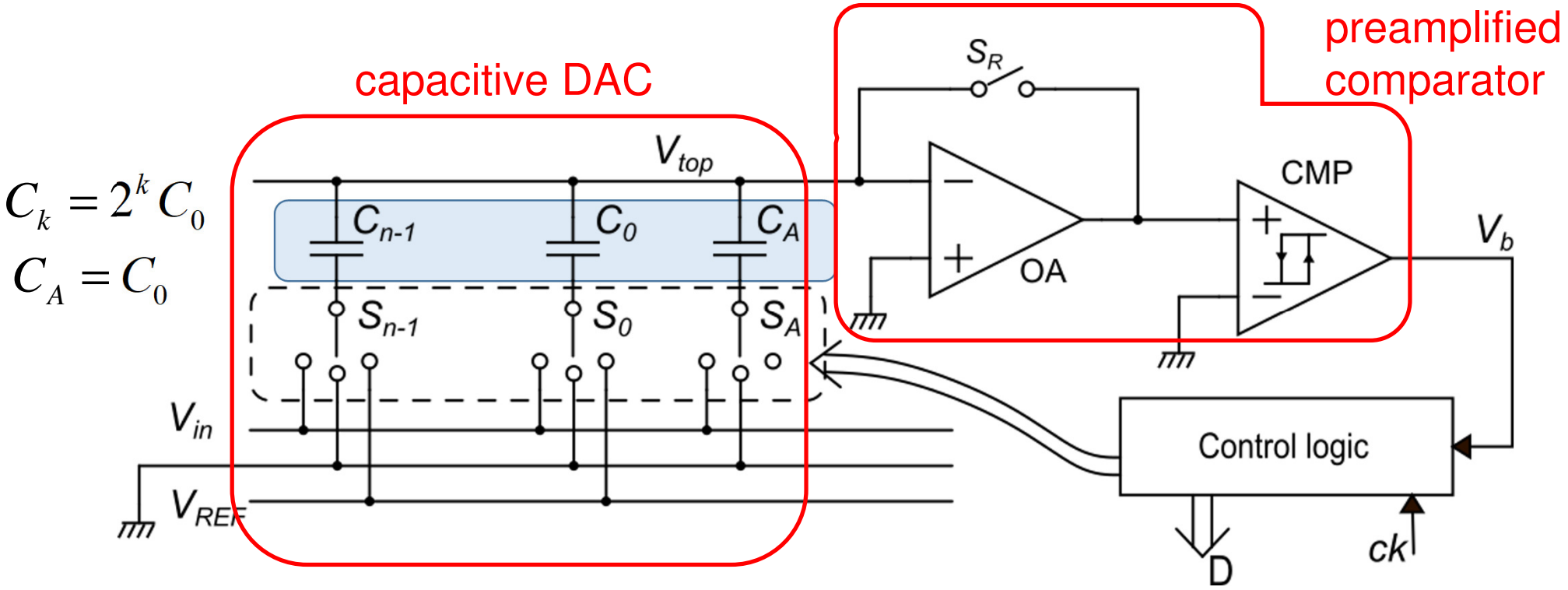
- Counting and Integrating ADCs:
  - Counting converters
  - Dual-slope

2^N cycles of comparison
(simple/accurate but slow)

- Binary-Search Algorithm based:
  - Successive approximation converters (SAR)
  - Pipelined converters

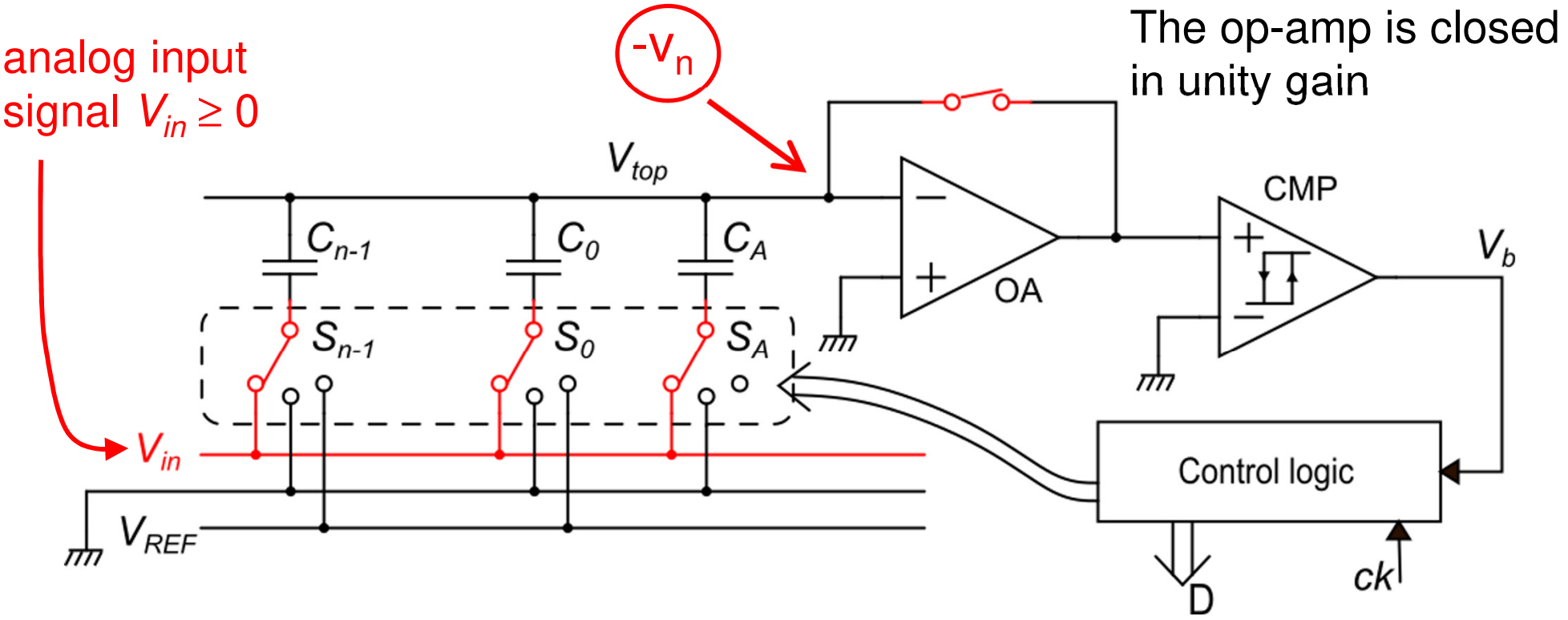
N cycles of comparison
(good trade-off speed/resolution)

A very common SAR ADC: the charge-redistribution ADC



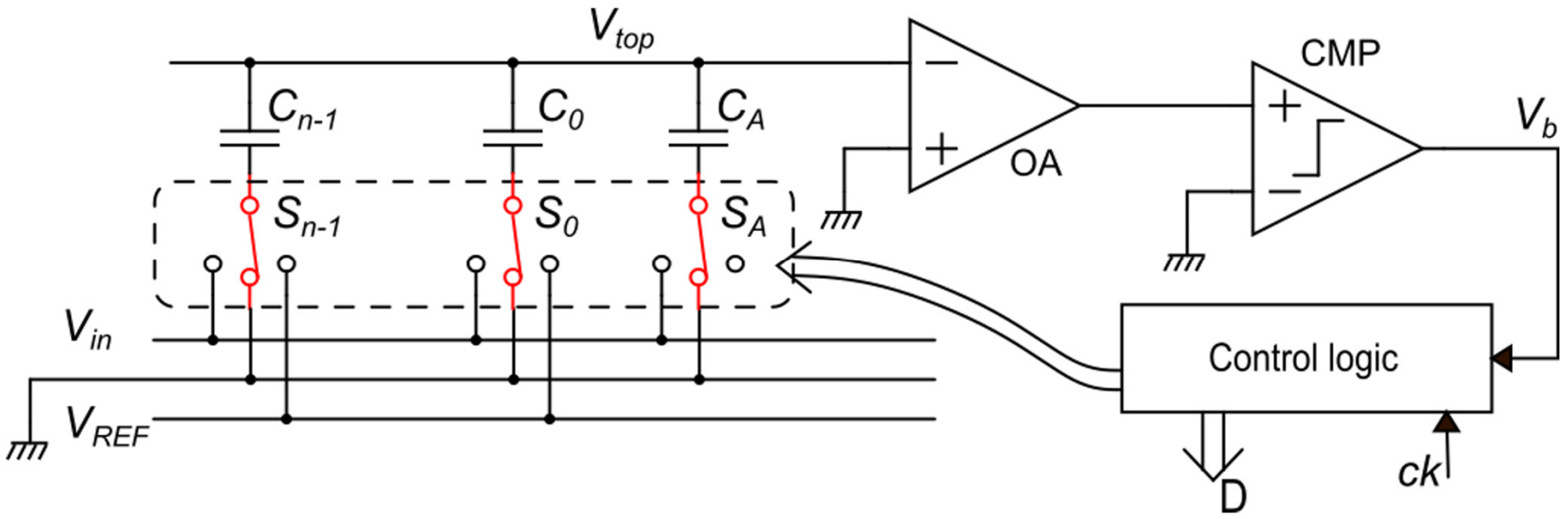
$$C_{tot} = C_A + \sum_{k=0}^{n-1} C_k = C_0 + C_0 \sum_{k=0}^{n-1} 2^k = C_0 + C_0\left(2^n - 1\right) = 2^n C_0$$

Reset phase



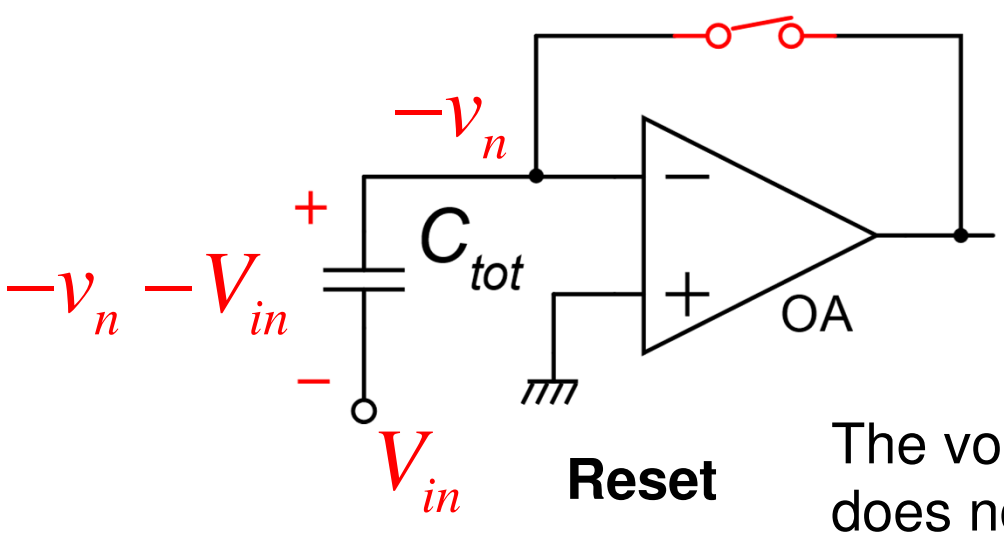
<u>All capacitors are in parallel,</u> with one terminal connected to the input voltage V_{in}.

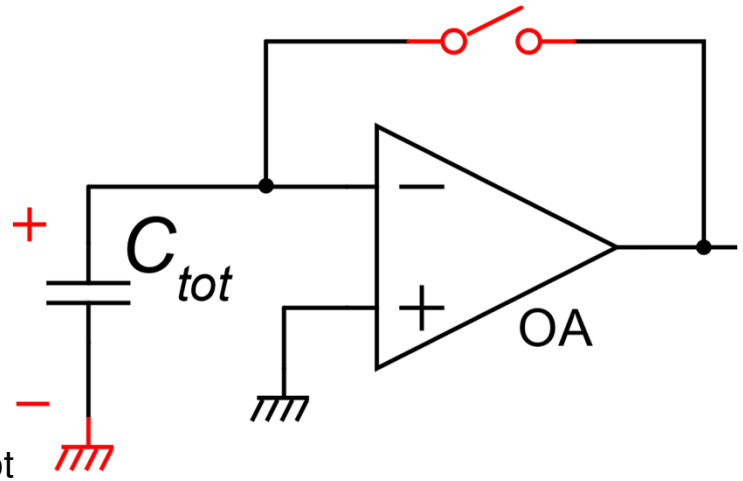
Sampling phase



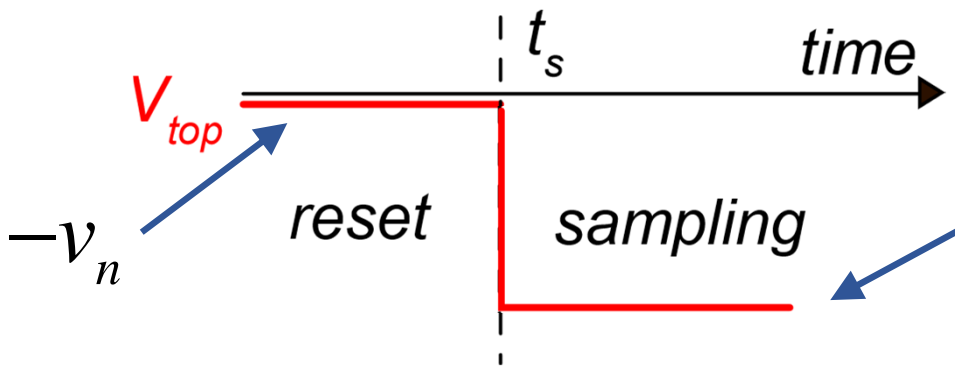
- The op-amp is placed in open loop configuration and the bottom plates of all capacitors are connected to gnd.
- The voltage of the top plates (V_{top}) is free to evolve (it is floating, no current comes from the OP to V_{top})

Top voltage in the sampling phase





The voltage on C_{tot} does not change

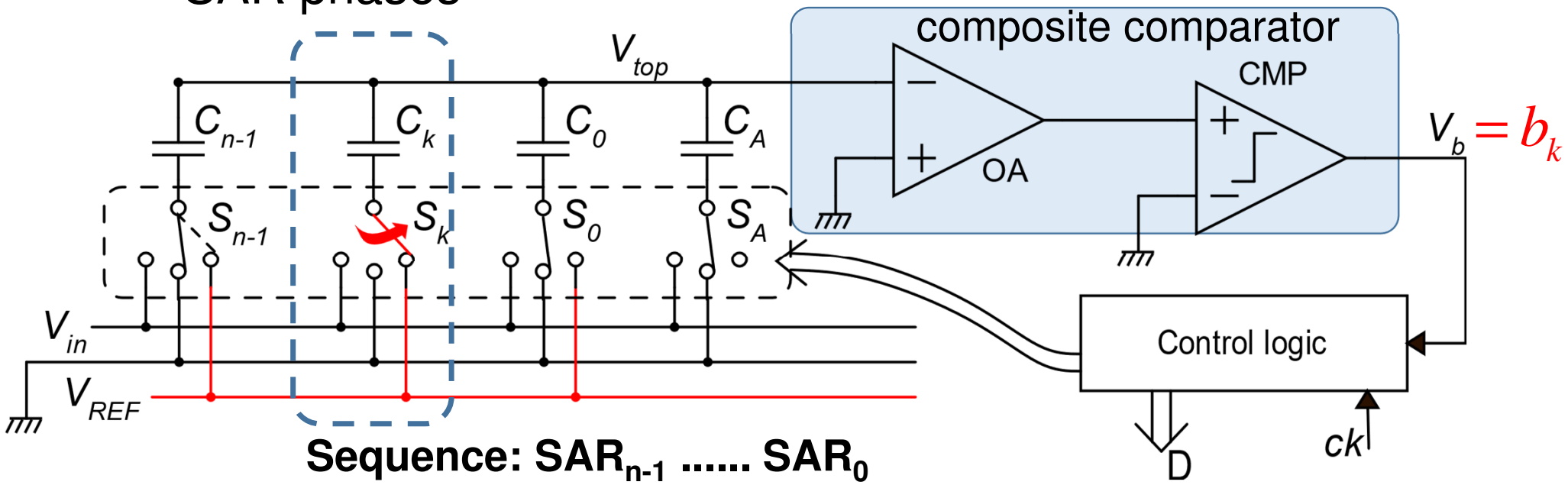


$$V_{top} = V_{Ctot}(t_s)$$

$$V_{top} = -V_{in}(t_s) - v_n(t_s)$$

$$(V_{in} \geq 0)$$

SAR phases

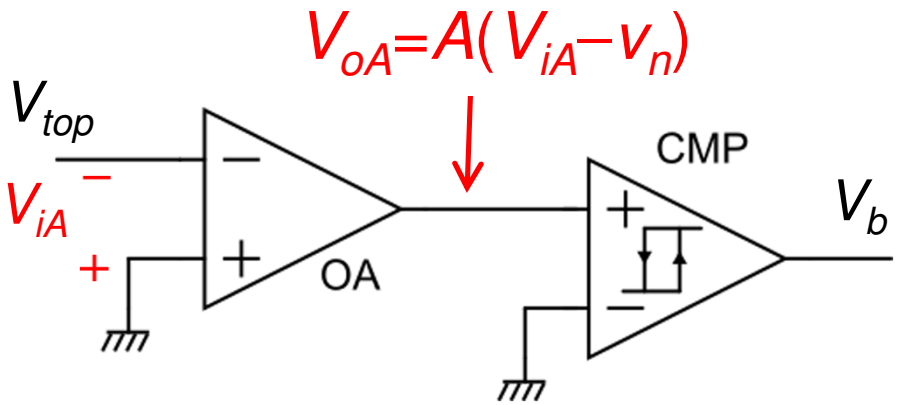


Sequence: SAR_{n-1} ..... SAR_0

Phase SAR_k

- Phase SAR_k begins by connecting the bottom plate of C_k to the reference voltage V_{REF} through switch S_k
- This causes a jump in voltage V_{top}.
- Bit k-th is the output of the composite comparator (V_b) at the end of phase SAR_k
- If b_k =0 S_k comes back to *gnd*, else it remains at V_{REF}

Composite comparator



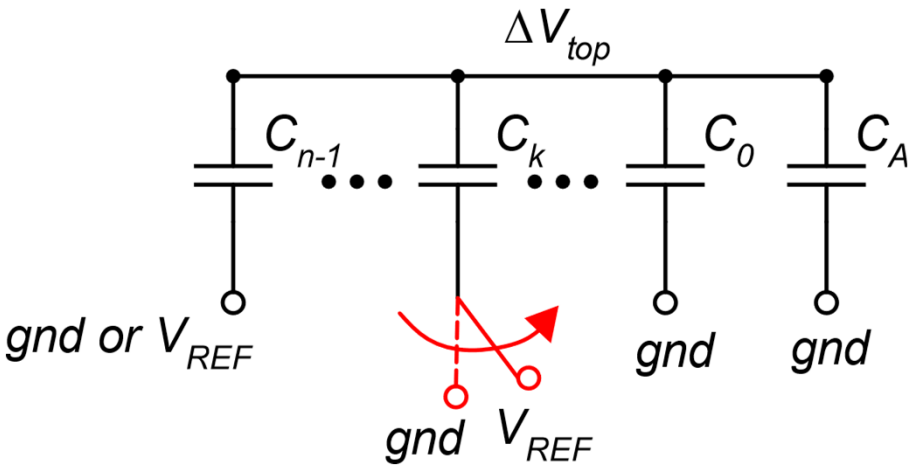
The gain of OA is so large that the offset and hysteresis of CMP has negligible impact on the composite comparator characteristics.

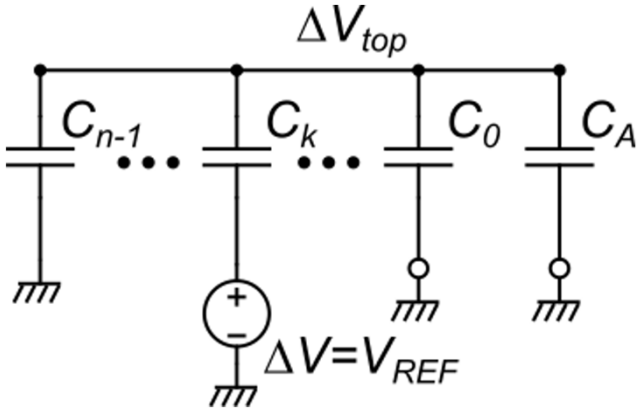
$$V_{iA} = -V_{top}$$

$$V_b = \begin{cases} 1 & \text{if} \quad V_{iA} > v_n \\ 0 & \text{if} \quad V_{iA} \le v_n \end{cases}$$

$$V_b = \begin{cases} 1 & \text{if} \quad -V_{top} > v_n \Leftrightarrow V_{top} < v_n \\ 0 & \text{if} \quad -V_{top} \le v_n \Leftrightarrow V_{top} \ge v_n \end{cases}$$

Phase $\mathbf{SAR_k}$: calculation of the V_{top} jump





ΔV_{top} at phase SAR_k

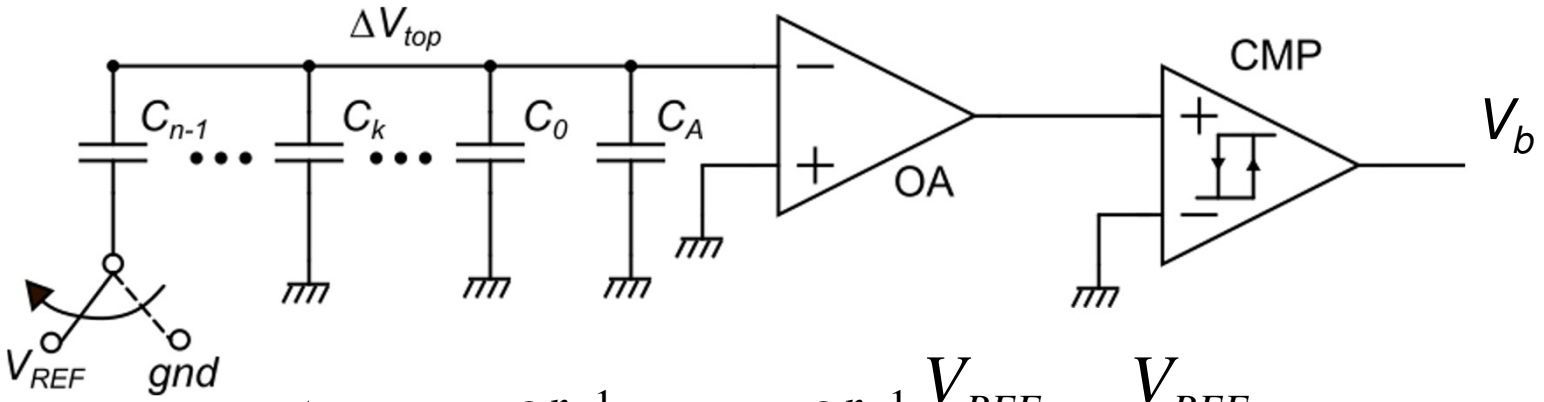
$$\Delta V_{top} = \Delta V_k = \Delta V \frac{C_k}{C_{tot}} = V_{REF} \frac{2^k C_0}{2^n C_0}$$

$$V_{LSB} = \frac{V_{REF}}{2^n} = \Delta$$

$$\Delta V_k = 2^k V_{LSB}$$

All-capacitor network: equivalent circuit for variations. Capacitors can be replaced by a resistors of value 1/C

Phase **SAR$_{n-1}$**



$$\Delta V_{n-1} = 2^{n-1} V_{LSB} = 2^{n-1} \frac{V_{REF}}{2^n} = \frac{V_{REF}}{2}$$

from sampling phase

$$V_{top} = \overbrace{-V_{in}(t_s) - v_n(t_s)} + \Delta V_{n-1} = -V_{in}(t_s) - v_n(t_s) + \frac{V_{REF}}{2}$$

Decision for bit b_{n-1} (taken at time t_{n-1} = end of phase SAR$_{n-1}$)

$$V_b = 1 \text{ if } V_{top}(t_{n-1}) < -v_n(t_{n-1}) \Rightarrow -V_{in}(t_s) - v_n(t_s) + \frac{V_{REF}}{2} < -v_n(t_{n-1})$$

Phase SAR_{n-1}

$$b_{n-1}=1 \text{ if: } -V_{in}(t_s)-v_n(t_s)+\frac{V_{REF}}{2}<-v_n(t_{n-1})$$

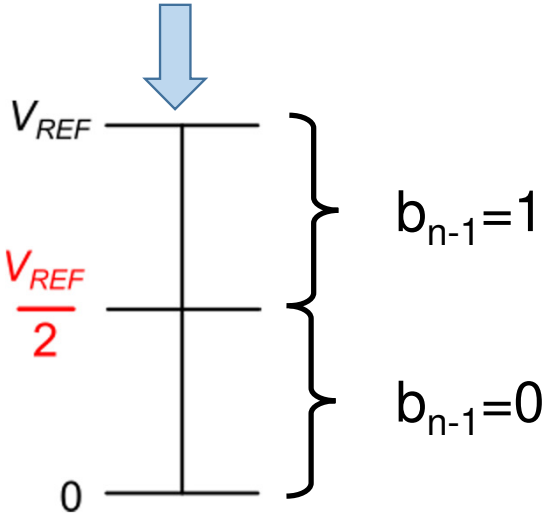
$$V_{in}(t_s)>\frac{V_{REF}}{2}-\underbrace{v_n(t_s)+v_n(t_{n-1})}$$

Subtraction of two noise samples taken at different times: constant and correlated components are rejected (CDS).

Neglecting noise / offset components, the condition becomes:

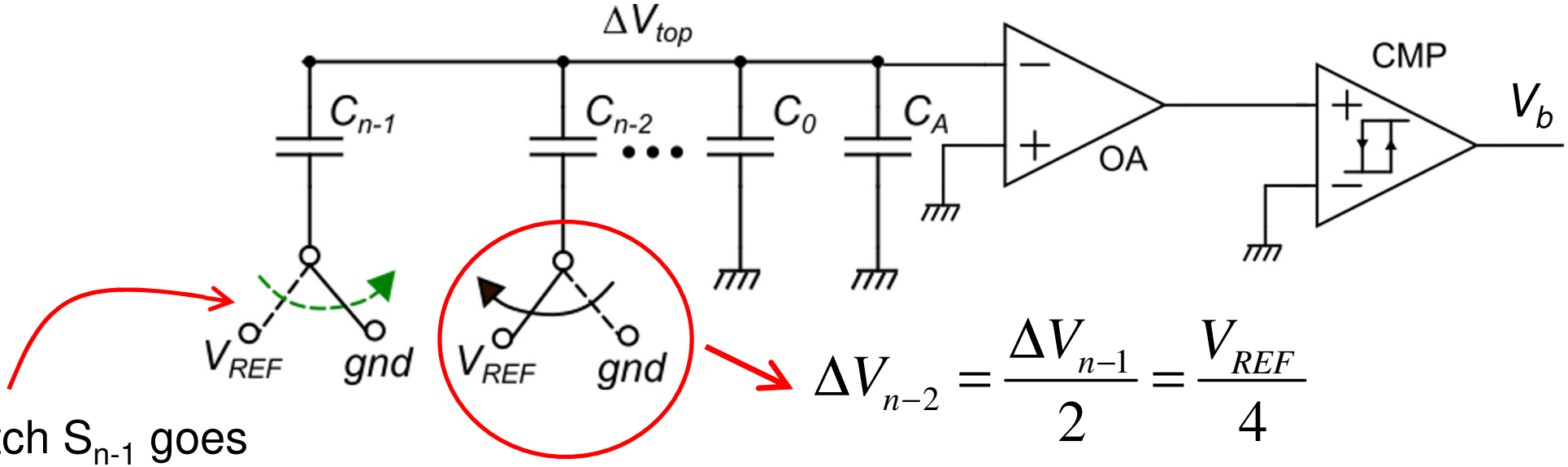
$$V_{in}(t_s)>\frac{V_{REF}}{2}$$

possible values of $V_{in}(t_s)$ and resulting value of b_{n-1}



This is in conformity with the successive approximation algorithm

Phase SAR_{n-2}



$$\Delta V_{n-2} = \frac{\Delta V_{n-1}}{2} = \frac{V_{REF}}{4}$$

Switch S_{n-1} goes back to *gnd* **if $b_{n-1}=0$** Otherwise, it remains to V_{REF}

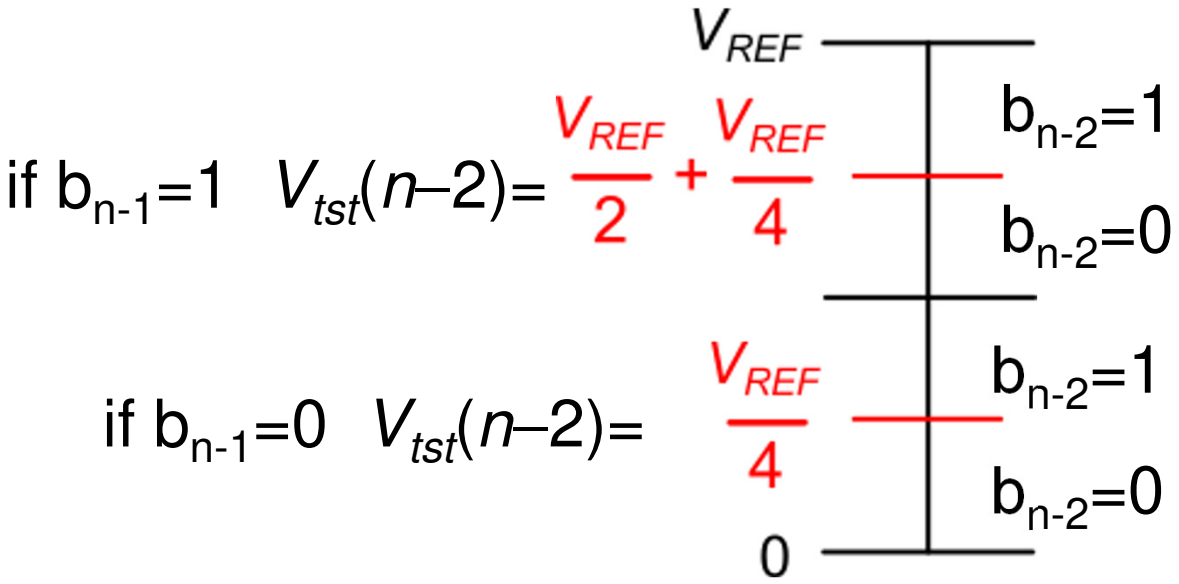
Decision : bit b_{n-2} =1 if:

$$V_{top} = -V_{in}(t_s) - v_n(t_s) + b_{n-1}\Delta V_{n-1} + \Delta V_{n-2} < -v_n(t_{n-2})$$

If S_{n-1} comes back to *gnd*, it subtracts ΔV_{n-1} from V_{top}

Decision for b_{n-2}

$$b_{n-2}=1 \text{ if: } V_{in}(t_s) > \underbrace{b_{n-1}\Delta V_{n-1}+\Delta V_{n-2}}_{V_{tst}(n-2)}$$



Generalization

At k-th step (phase SAR_k) , bit b_k is determined from the comparison of $V_{in}(t_s)$ with:

$$V_{tst}(k) = \underbrace{b_{n-1}\Delta V_{n-1} + b_{n-2}\Delta V_{n-2} + ... + b_{k+1}\Delta V_{k+1}} + \Delta V_k$$

Increments applied in previous phases and maintained only if the corresponding bits are 1

At any step the increment is halved

$$\Delta V_k = \frac{\Delta V_{k+1}}{2}$$

At the last phase, SAR_0, the LSB (b_0) is determined and the conversion is complete. The bits determined in the successive phases are stored inside a register of the control logic and can be retrieved at the end of conversion.

Examples of conversion cycle