Mitigation of Single Event Upsets in the Control Logic of a Charge Equalizer for Li-ion Batteries

F. Baronti, C. Bernardeschi, L. Cassano, A. Domenici, R. Roncella, R. Saletti

Dipartimento di ingegneria dell’informazione, Università di Pisa
Overview

- A Battery Management System has been designed and implemented.
- Charge equalization is controlled by a CPLD.
- Two *ad hoc* fault-tolerant designs have been produced to mitigate the effects of SEUs in the CPLD.
- The two designs have been simulated and evaluated wrt to the TMR approach.
Lithium-ion batteries are a promising solution for energy storage in many industrial applications, such as electric transportation and smart grids.

Li-ion batteries are very sensitive to overcharge, deep discharge and operation outside the specified temperature range.

A Battery Management System (BMS) is required to guarantee the safe and effective operation of the battery.

In particular, the BMS must keep a balanced *State of Charge* among the battery cells.
Programmable Logic Devices (PLD), such as CPLDs and FPGAs, are cost-effective building blocks for the control logic of a BMS.

However, they are subject to radiation-induced faults, called Single Event Upsets (SEU), which may alter their behavior.

Since a BMS is a safety-critical component, it is necessary to adopt appropriate fault-tolerance techniques to improve its reliability.

In this work, we analyze by simulation different fault-tolerant designs for the control logic of a charge equalizer.
Within a battery pack, a DC/DC converter moves charge from one cell to another to achieve charge equalization by *active balancing*.

The d[3..0] signals from the microcontroller encode the required switch configuration s[11..1], computed by the *logic driver*.
To avoid short circuits, only one DPST switch may be conducting at any time.

Thus, at most one of the s[11..1] signals may be asserted at any time.
Or else...

Zap!
The logic driver ensures that configurations leading to short circuits are not possible.

The logic driver is a safety critical component.
Simulated fault-tolerance techniques

CL: the non-hardened design.
CLF: the control logic followed by the Filter block, which blocks all commands with more than one closed switch.
CLF3UV: the control logic followed by the triplicated Filter and a unanimity voter (AND gate).
CL3MV: the classical TMR technique.
A logic cell

A simplified view of an Altera Max V logic cell.
## Implementation parameters

<table>
<thead>
<tr>
<th></th>
<th>LCs</th>
<th>FFs</th>
<th>LUTs</th>
<th>LUT-FF</th>
<th>LUTs + LUT-FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL</td>
<td>26</td>
<td>4</td>
<td>11</td>
<td>11</td>
<td>22</td>
</tr>
<tr>
<td>CLF</td>
<td>45</td>
<td>4</td>
<td>30</td>
<td>11</td>
<td>41</td>
</tr>
<tr>
<td>CL3MV</td>
<td>89</td>
<td>12</td>
<td>44</td>
<td>33</td>
<td>77</td>
</tr>
<tr>
<td>CLF3UV</td>
<td>94</td>
<td>4</td>
<td>79</td>
<td>11</td>
<td>90</td>
</tr>
</tbody>
</table>

LC: Overall number of required logic cells, divided in:

- LUTs: LCs using only LUTs;
- FFs: LCs using only flip-flops;
- LUT-FF: LCs using both LUTs and flip-flops.
Smallest Altera MAX V CPLDs

<table>
<thead>
<tr>
<th>Feature</th>
<th>5M40Z</th>
<th>5M80Z</th>
<th>5M160Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells (LCs)</td>
<td>40</td>
<td>80</td>
<td>160</td>
</tr>
<tr>
<td>Typical equivalent macrocells</td>
<td>32</td>
<td>64</td>
<td>128</td>
</tr>
<tr>
<td>Maximum user I/O pins*</td>
<td>54</td>
<td>54</td>
<td>54</td>
</tr>
<tr>
<td>Accommodates FT schemas</td>
<td>no</td>
<td>CLF</td>
<td>CLF3UV</td>
</tr>
</tbody>
</table>

* 64-Pin EQFP

The 5M40Z device is sufficient for the basic (non-FT) design, but the 5M80Z and 5M160Z are needed for the FT designs.

However, the three devices are all available in the 64-Pin EQFP package: FT designs do not require board-level redesign.
Simulation environment

Each CL implementation has been simulated with sequences of random test vectors $i$ clock cycles long, with $i$ from 1 to 10.

For each value of $i$, 10,000 simulation runs have been performed.

At each simulation run, a fault has been injected into a random location of the configuration memory.

*System failures $(F_i)$*: only affect BMS performance.
*Catastrophic failures $(CF_i)$*: cause physical damage.
System failure probability

Failure probability as a function of test vector sequence length $i$:

$$FP_i = F_i/10000$$

Triple modular redundancy achieves the best results.
Catastrophic failure probability

\[ \text{CFP}_i = \frac{\text{CF}_i}{10000} \]

**Triple filtering** achieves the best results.

**Single filtering** has an intermediate performance.
Summary of simulation results

<table>
<thead>
<tr>
<th></th>
<th>Ovhd</th>
<th>FP\textsubscript{10}</th>
<th>CFP\textsubscript{10}</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL</td>
<td>1.0</td>
<td>1.00</td>
<td>1.000</td>
</tr>
<tr>
<td>CLF</td>
<td>1.7</td>
<td>0.95</td>
<td>0.090</td>
</tr>
<tr>
<td>CL3MV</td>
<td>3.4</td>
<td>0.02</td>
<td>0.010</td>
</tr>
<tr>
<td>CLF3UV</td>
<td>3.6</td>
<td>0.96</td>
<td>0.005</td>
</tr>
</tbody>
</table>

Ovhd: Area overhead wrt bare non fault-tolerant design.

FP\textsubscript{10}: Failure probability with 10 clock cycles.

CFP\textsubscript{10}: Catastrophic failure probability with 10 clock cycles.

The CLF3UV design is more effective than the CL3MV, with a small increase of area overhead.
Conclusions

Two design-specific SEU mitigation techniques for a BMS have been designed and simulated.

The two designs have been assessed for effectiveness, taking TMR as a reference.

The TMR approach is most effective at reducing the probability of system failures, i.e., affecting only BMS performance.

The design-specific solution using the triplicated safety filter is most effective at reducing the probability of catastrophic failures, i.e., leading to physical damage due to short-circuits.

The implementation of these mitigation techniques can be achieved by a moderate increase of the used logic resources.

In particular, their implementations fit on the same package as the non-mitigated design, thus requiring no change to the original board layout.
Thank you

Danke schön