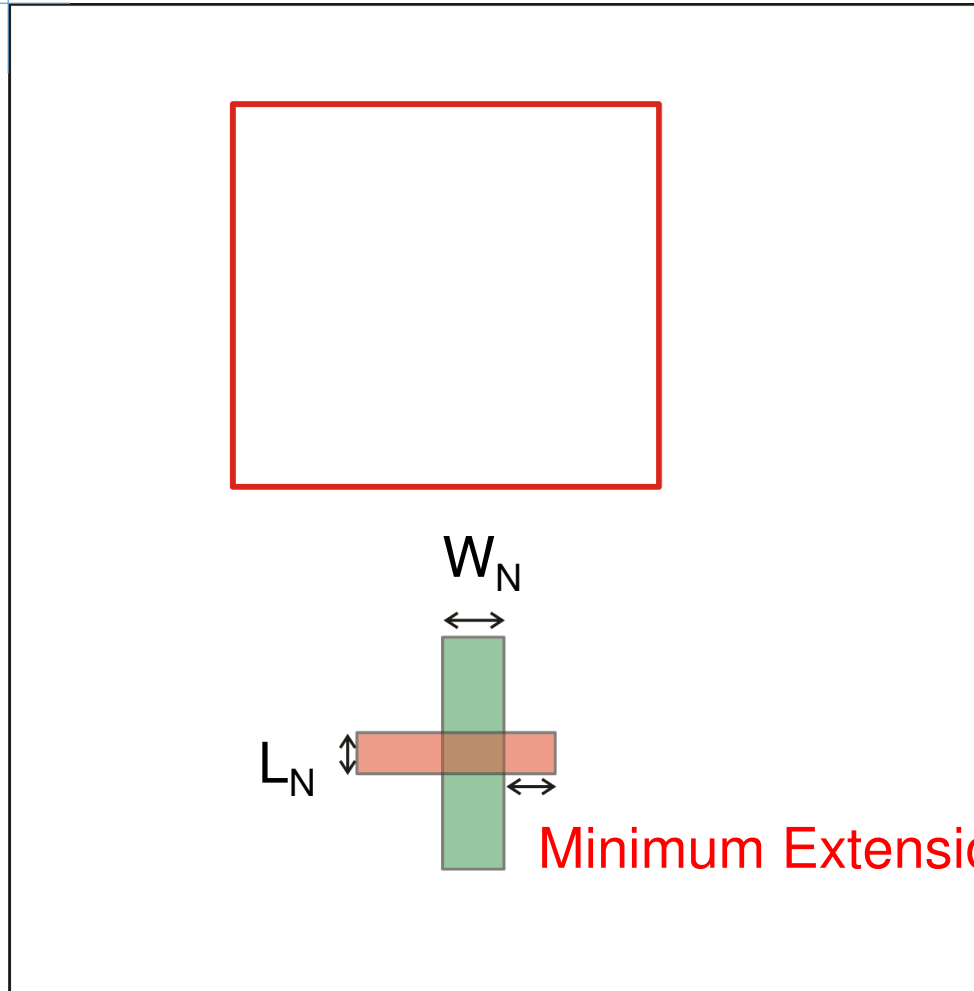
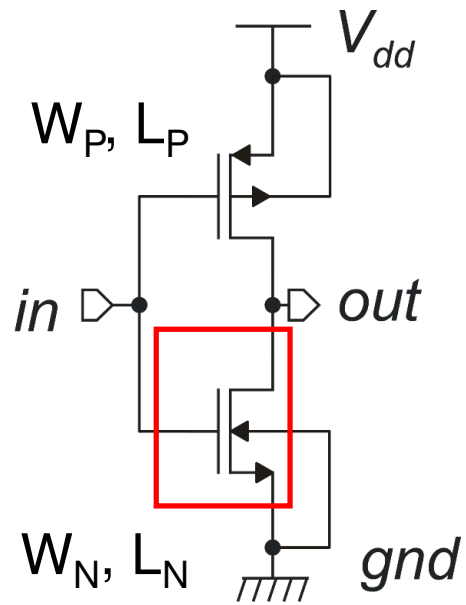
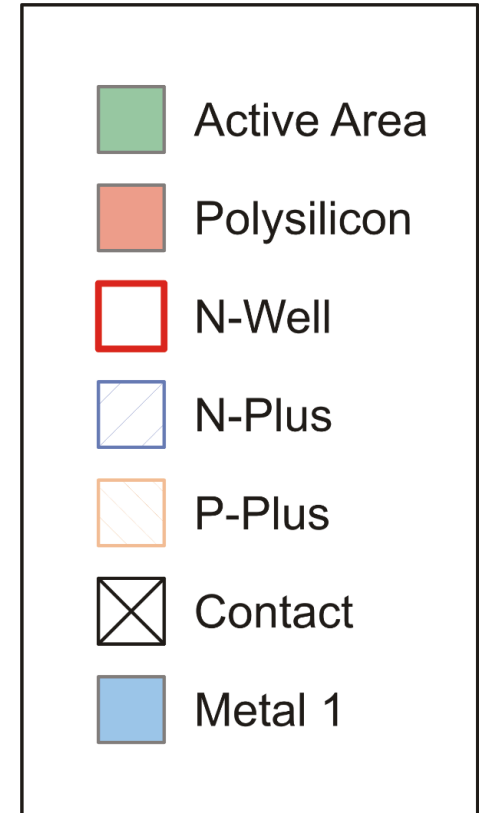


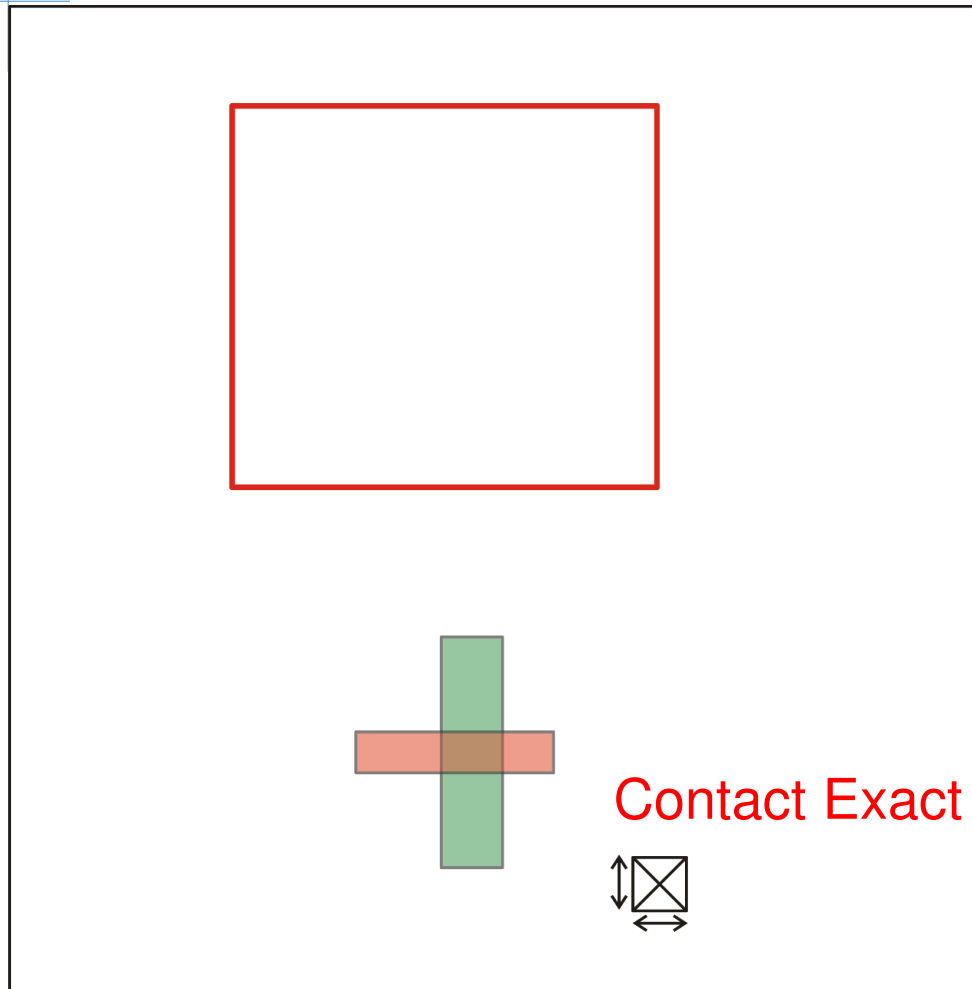
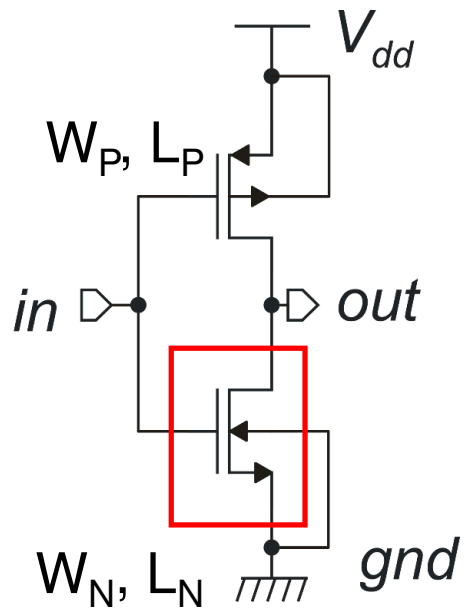
Example: CMOS Inverter



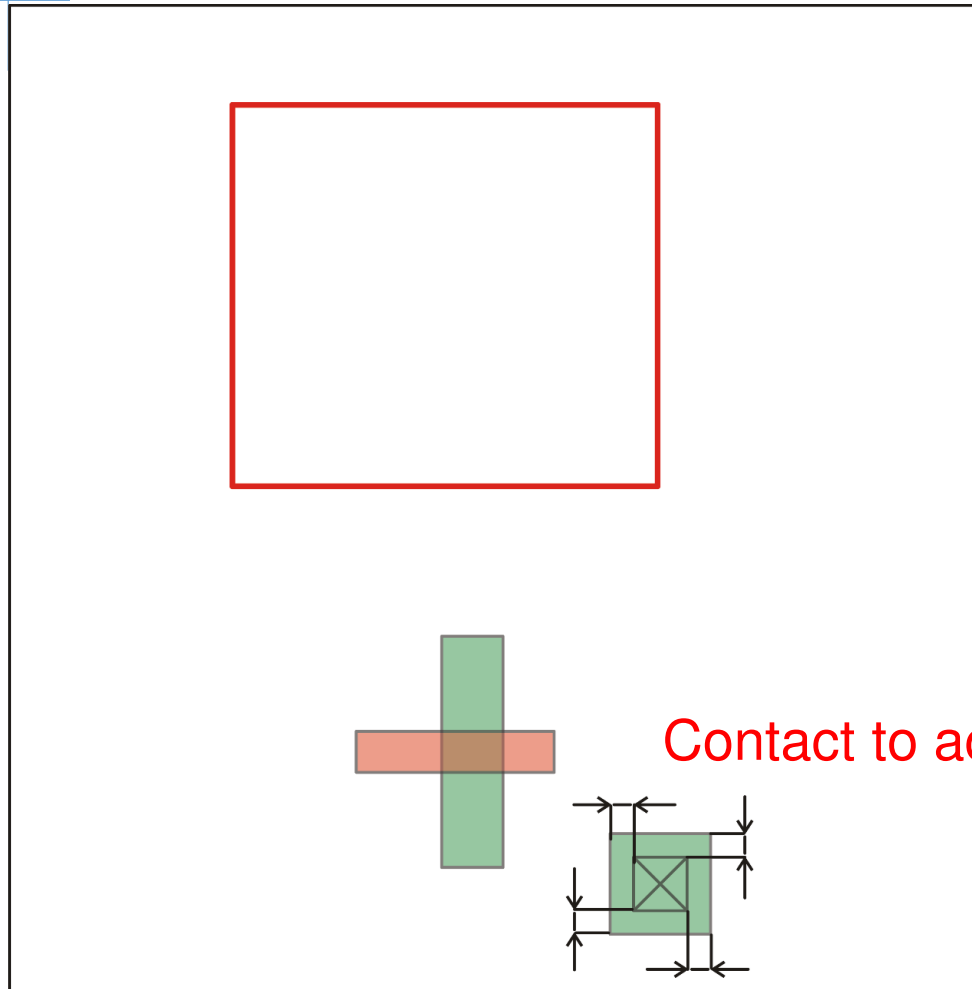
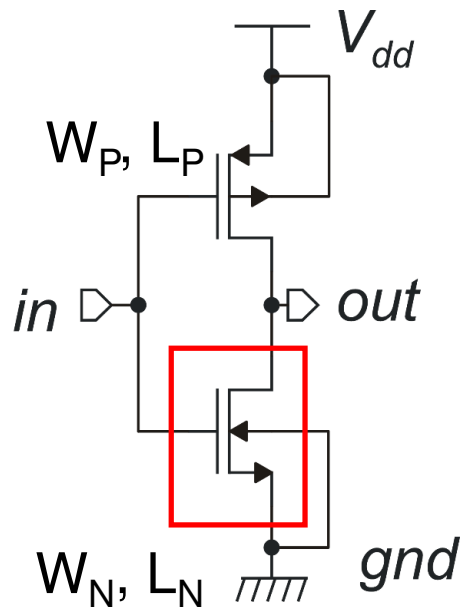
Layer Palette



Let's introduce a contact

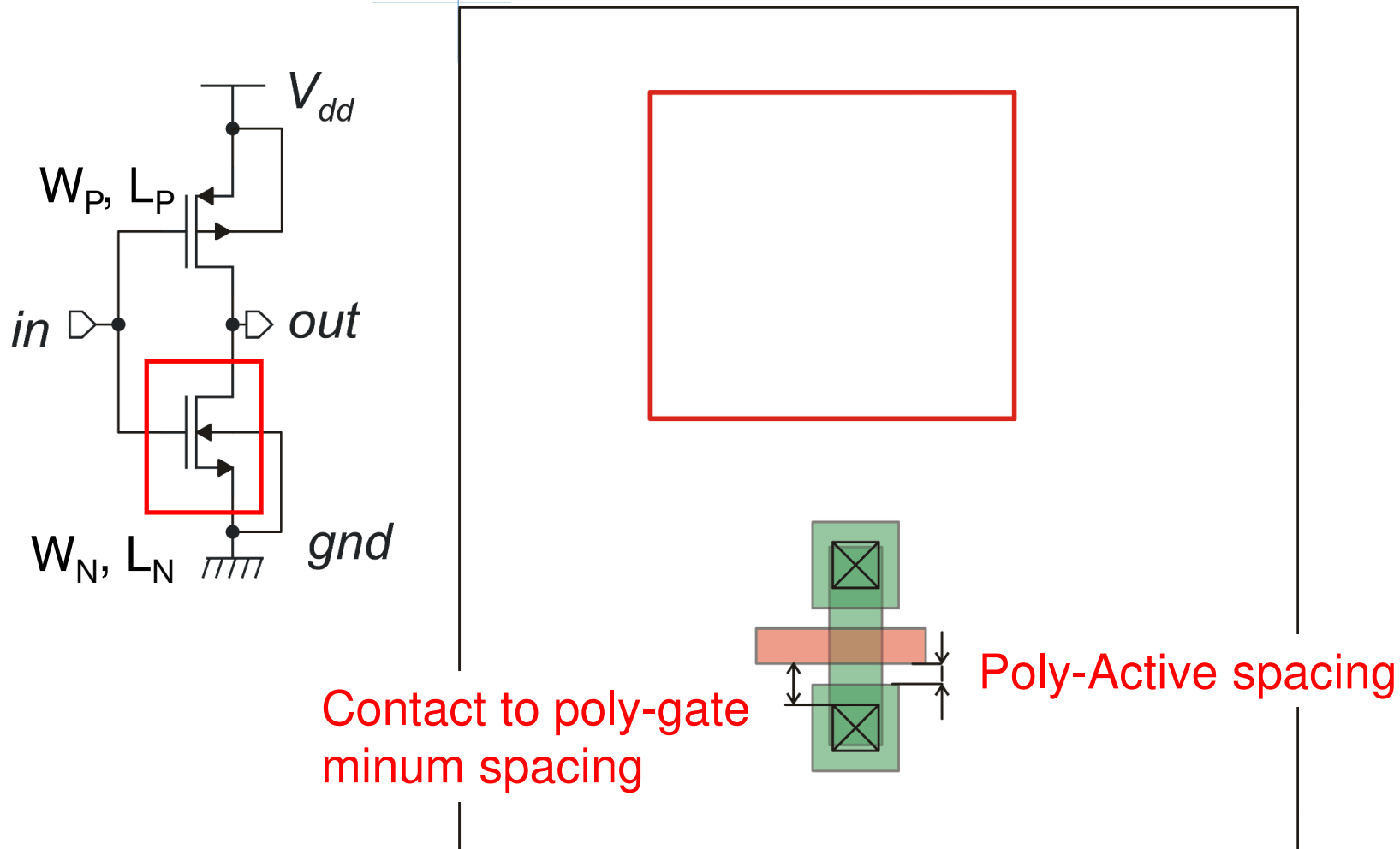


Then, we provide enough active surround to the contact

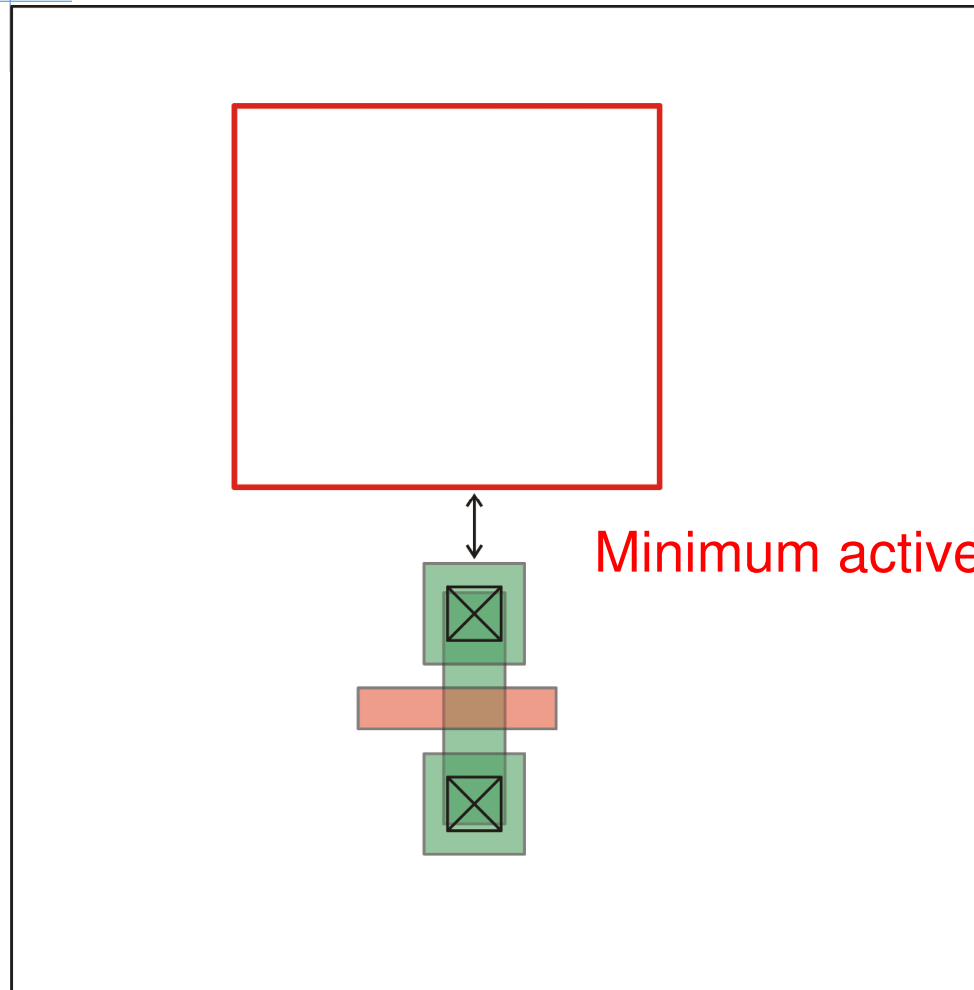
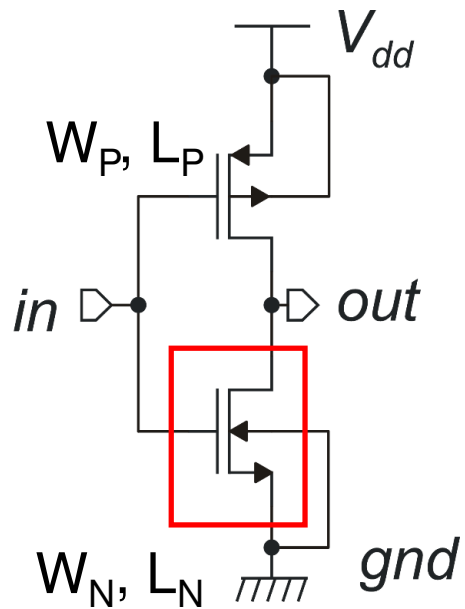


Contact to active margin

Then, we provide enough active surround to the contact

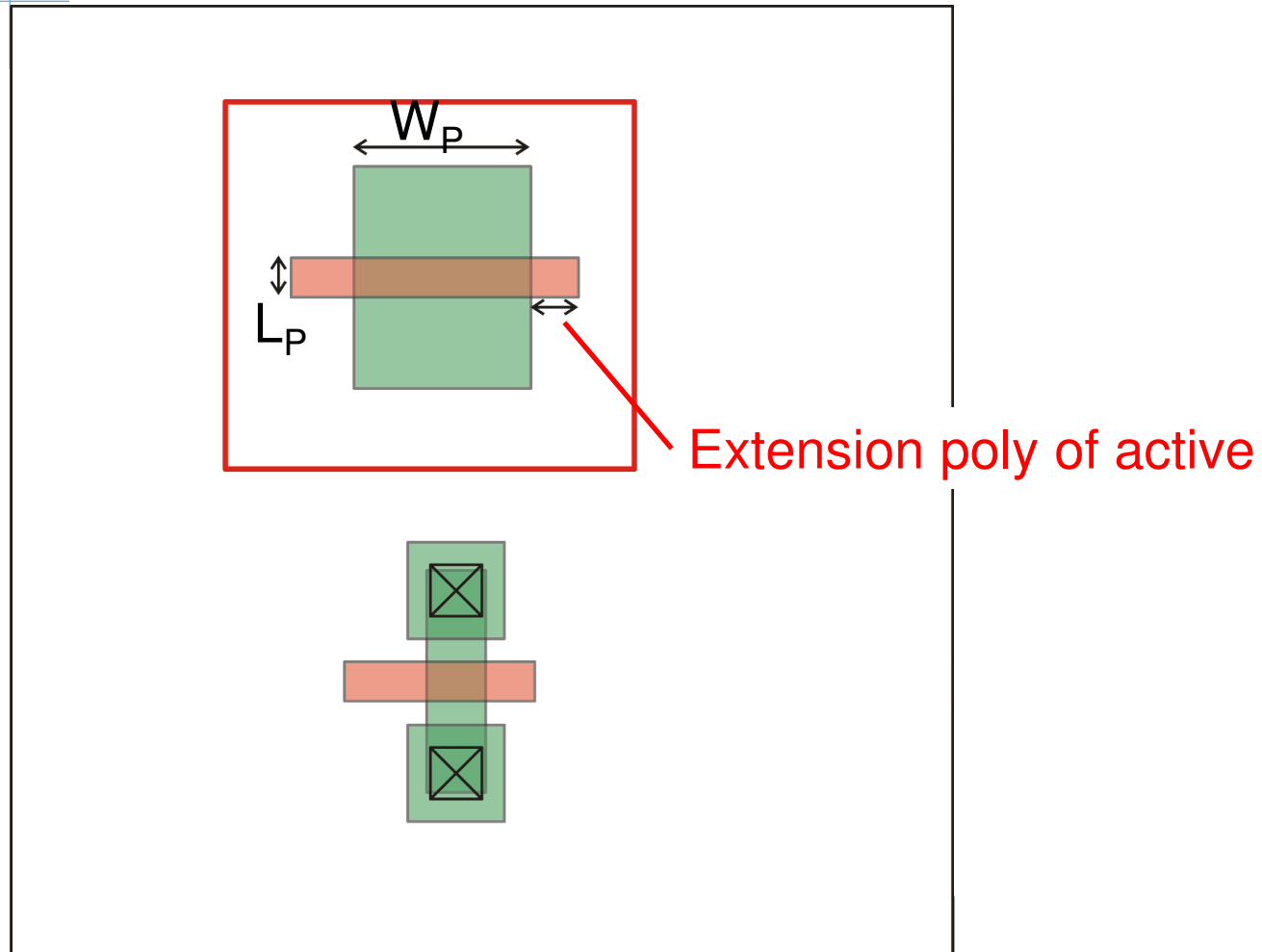
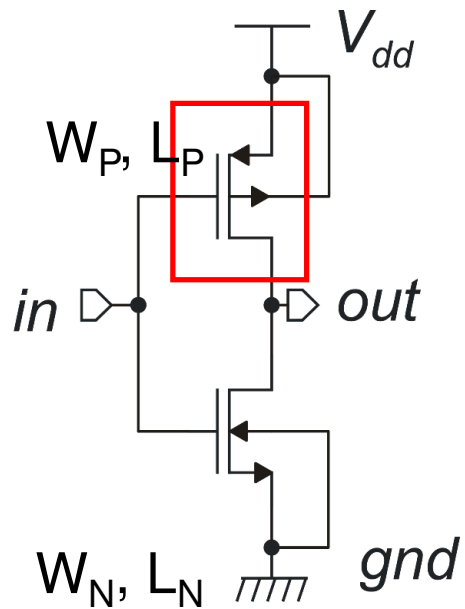


Place the n-MOS as close as possible to the n-well

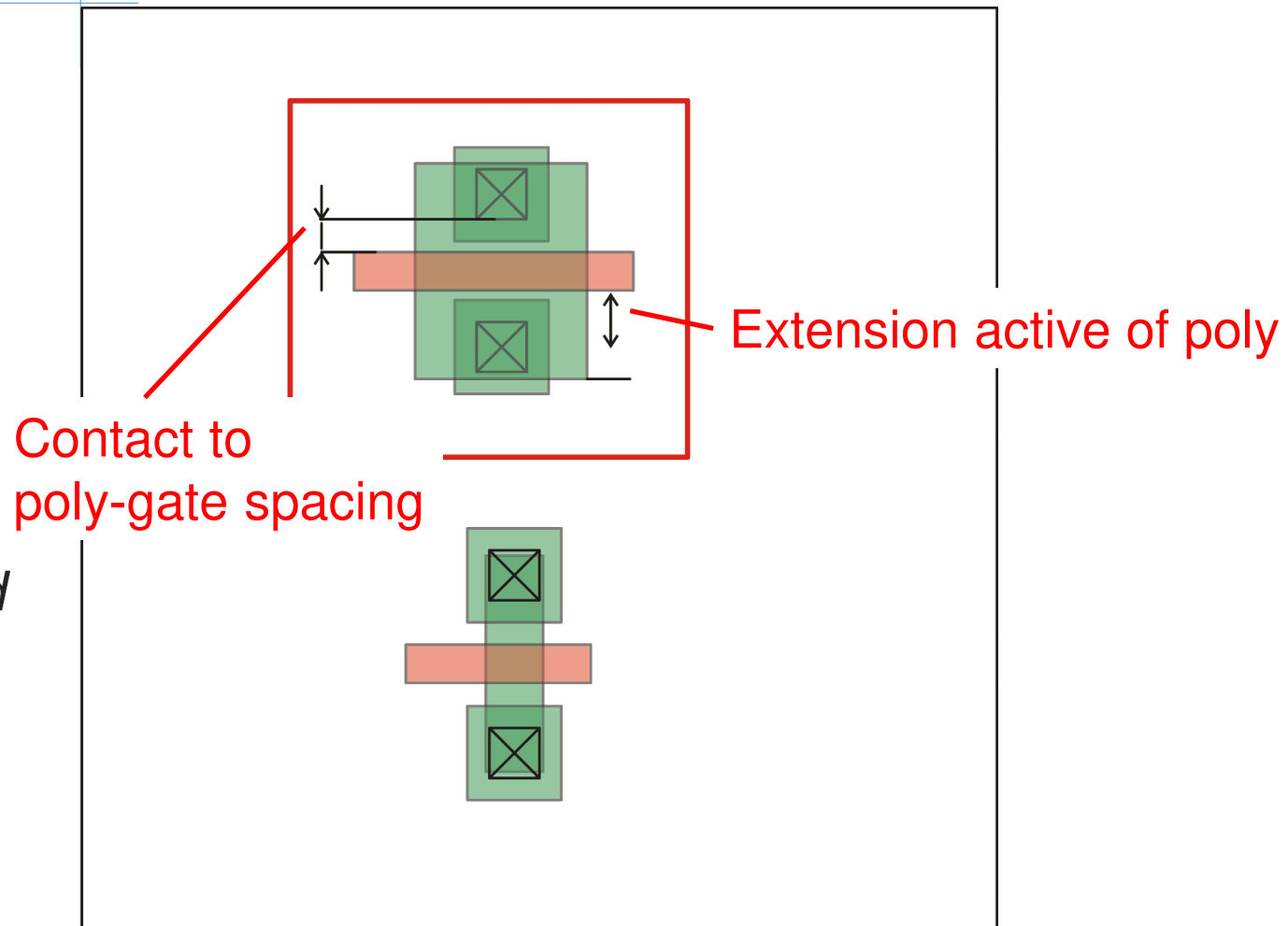
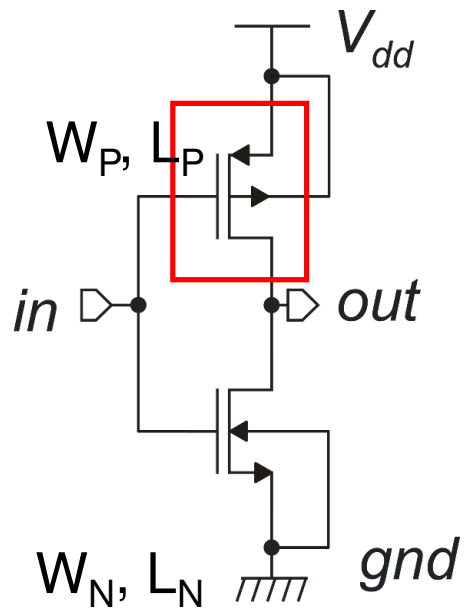


Minimum active to well spacing

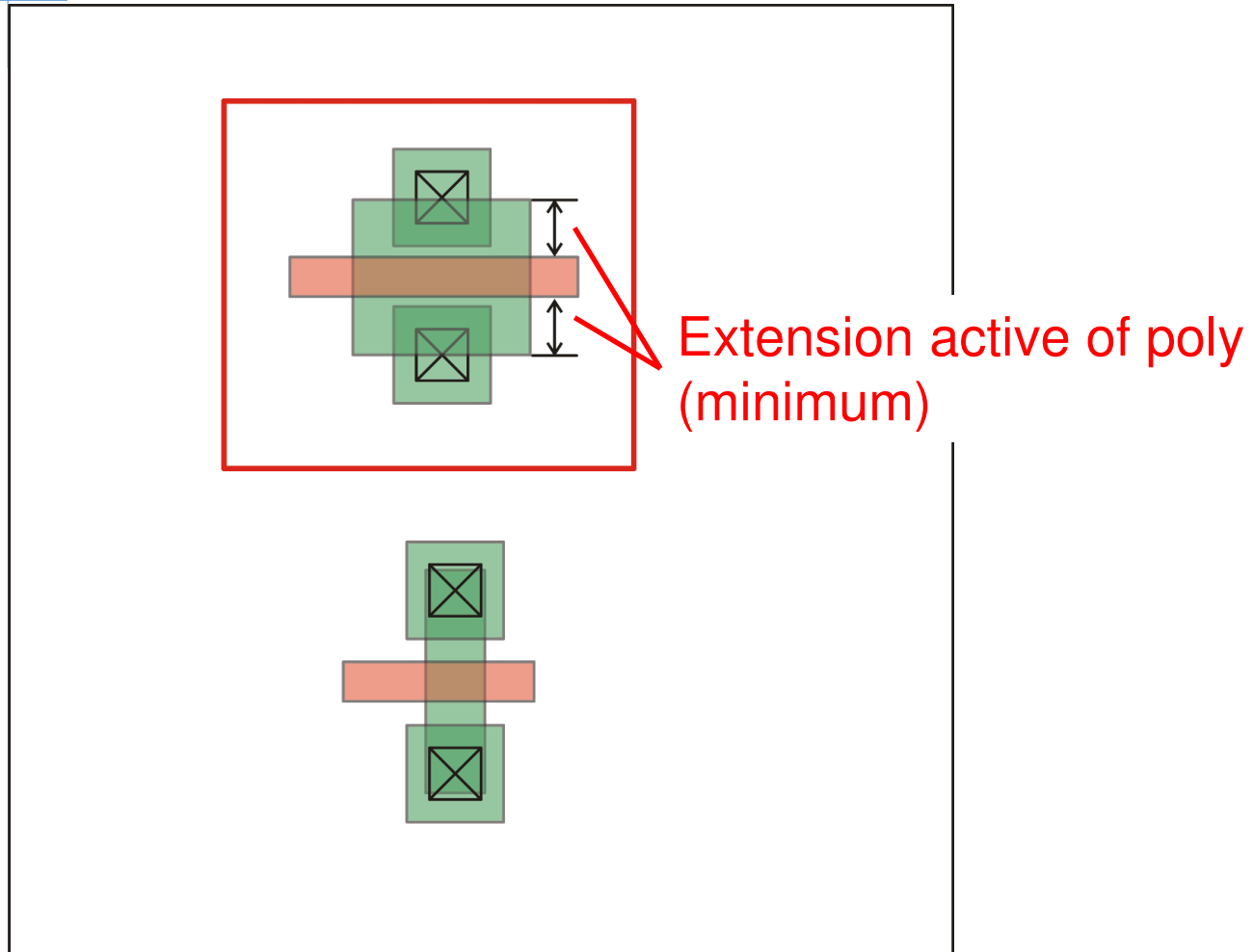
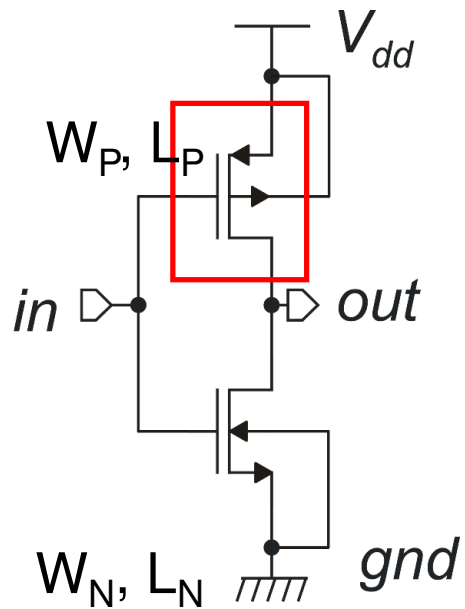
Now draw the p-MOS inside the n-well



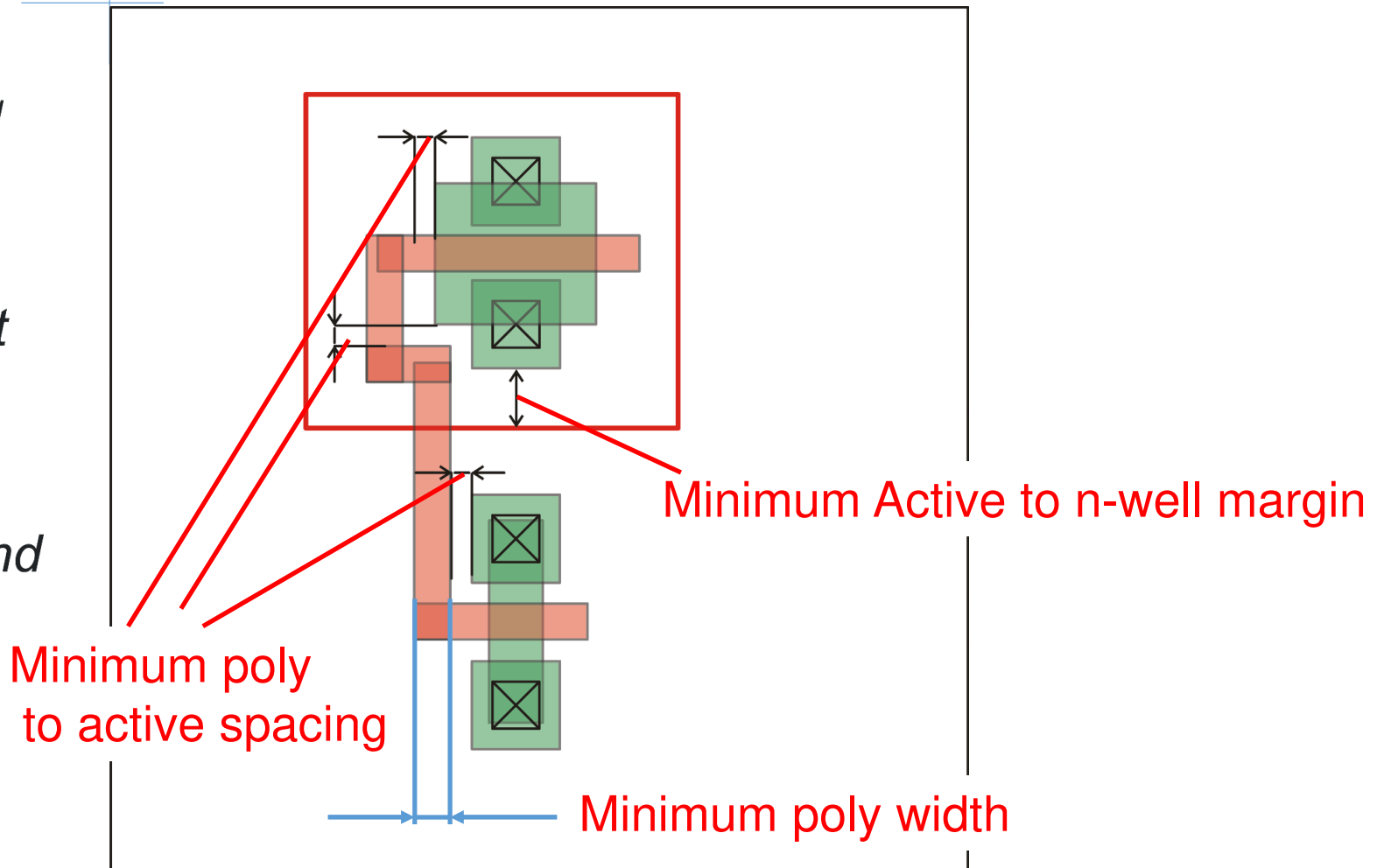
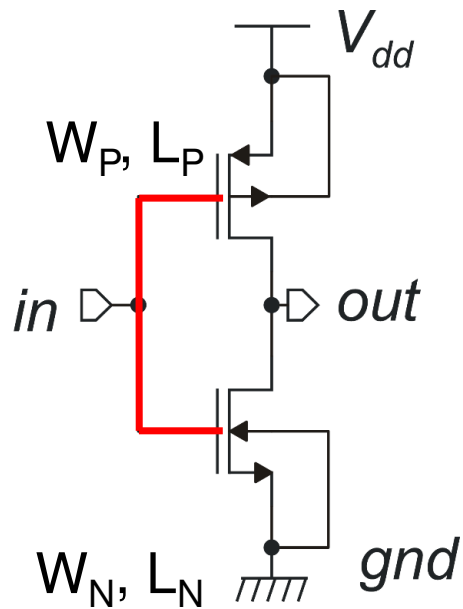
Place the source/drain contact of the



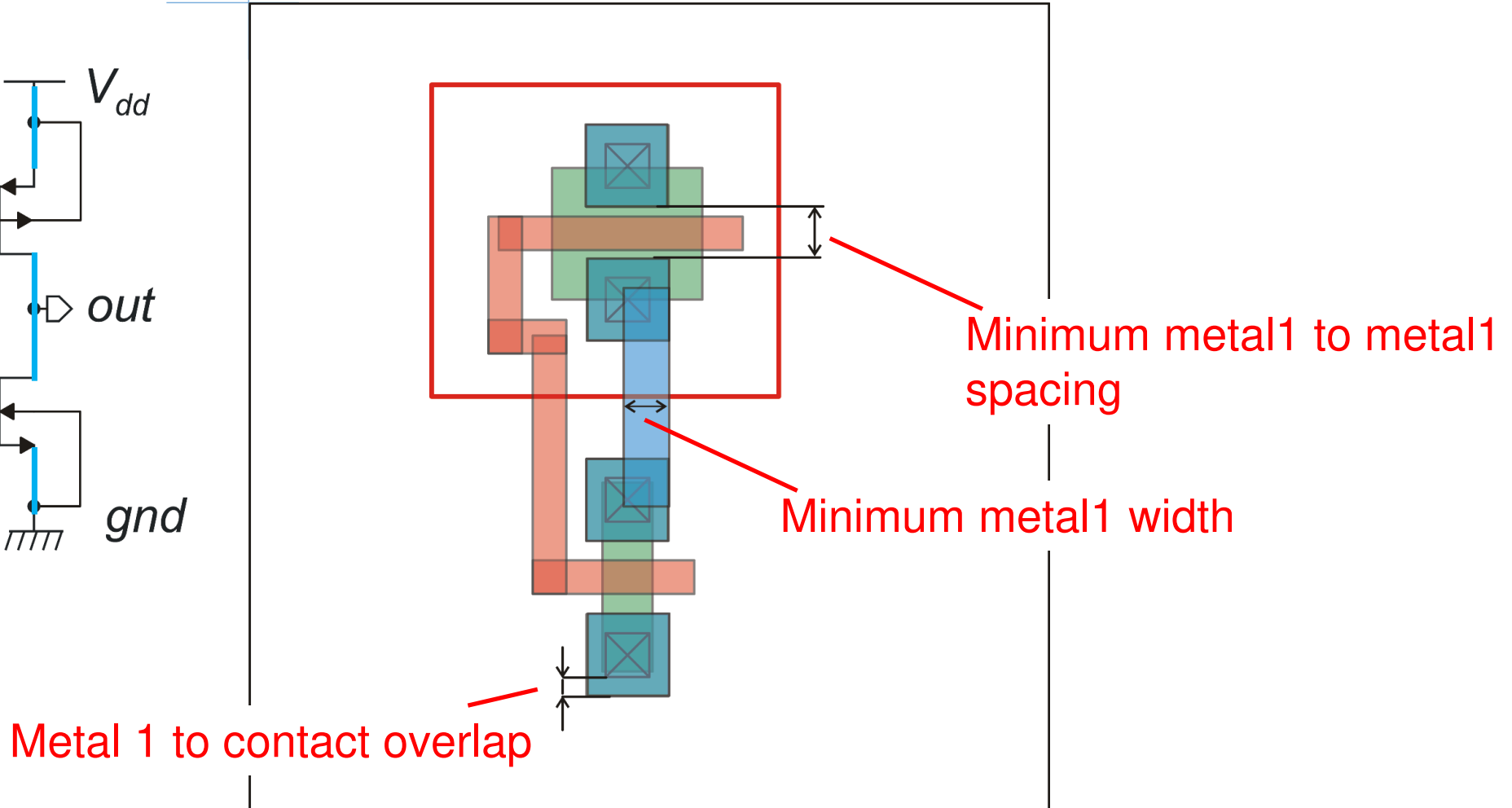
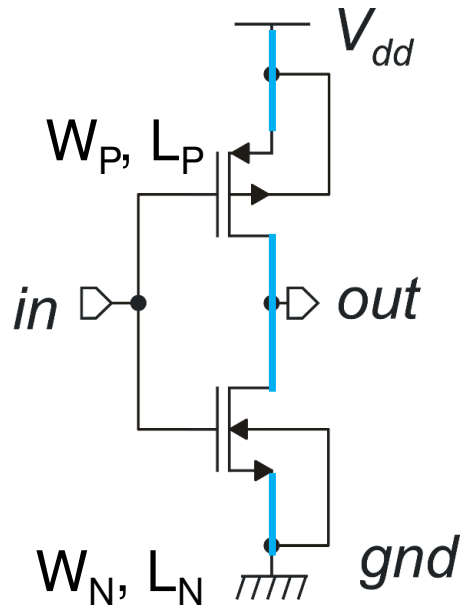
Reduce the active extension to the minimum



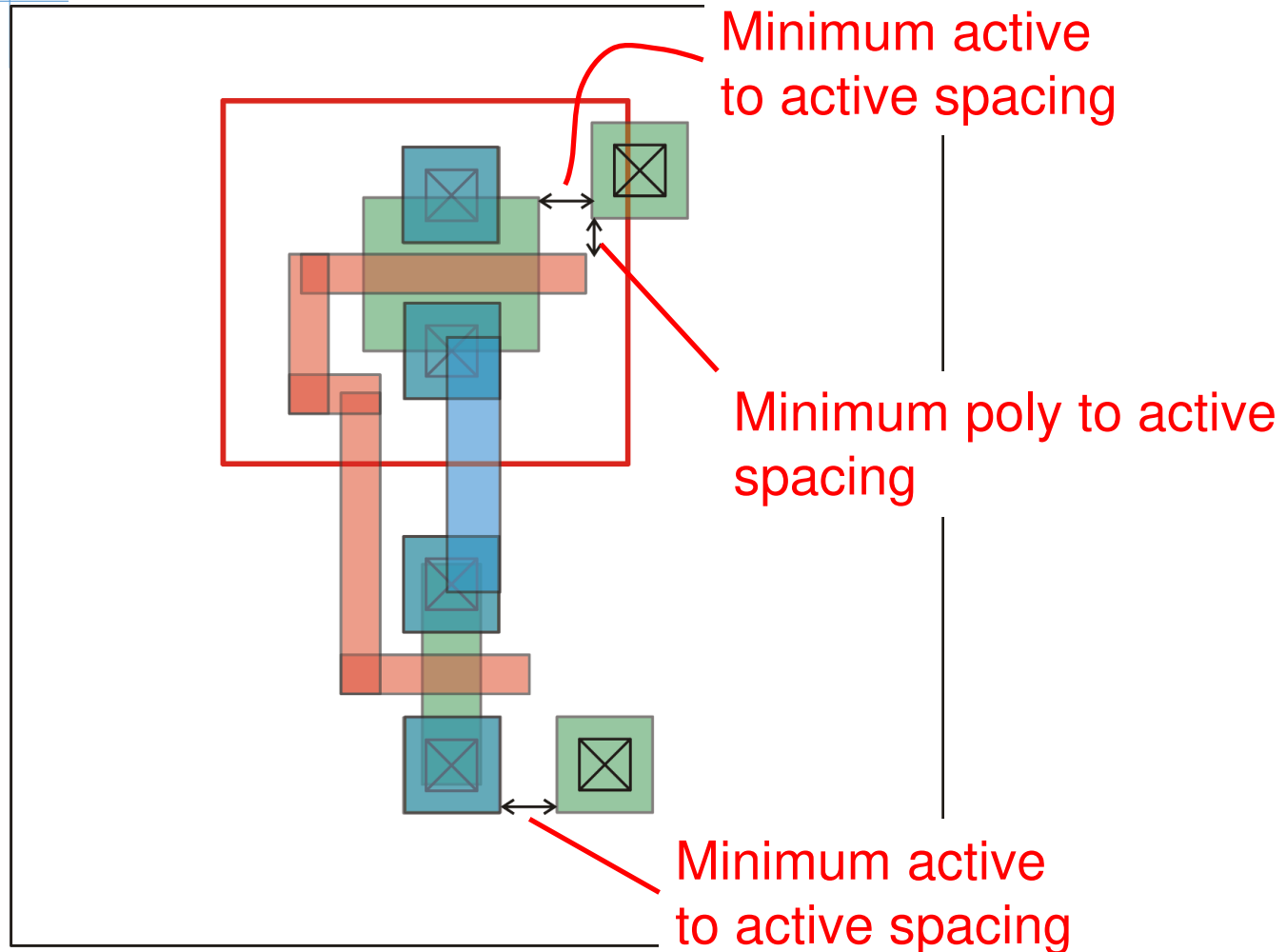
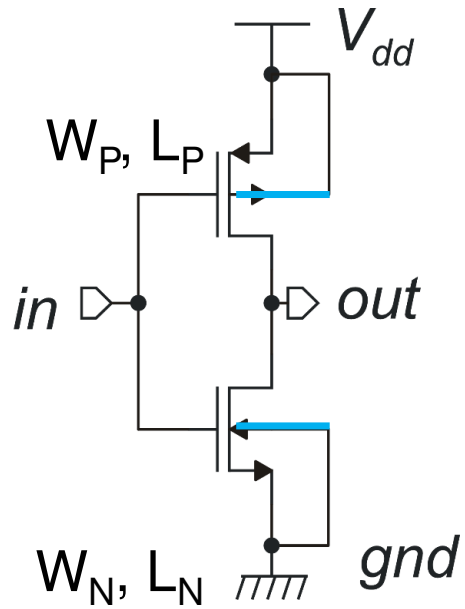
Connect the gates of the n-MOS and p-MOS



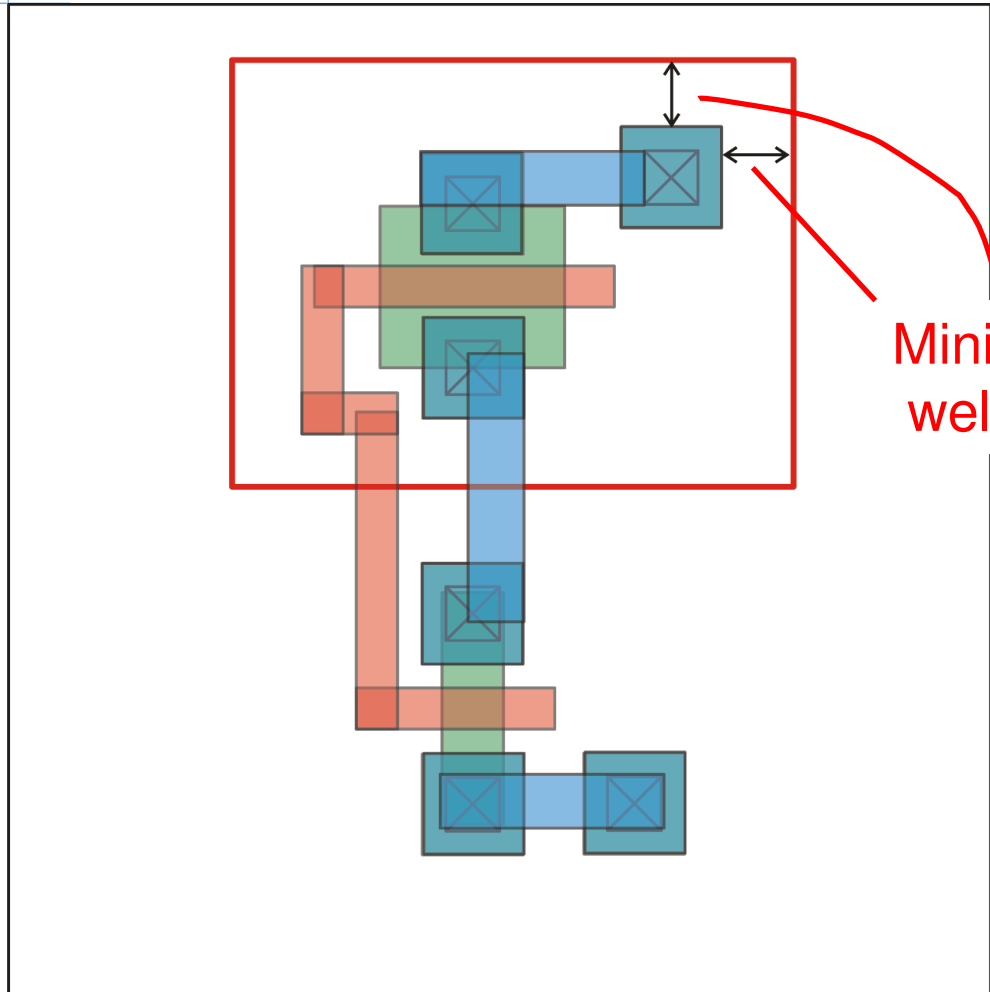
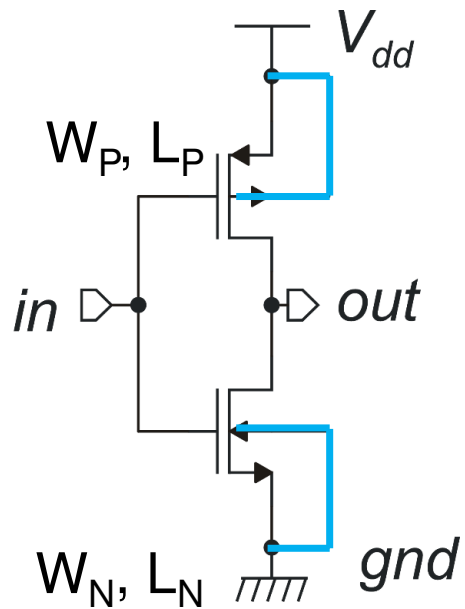
Introduce the metal-1 connections



Introduce the substrate and n-well contacts

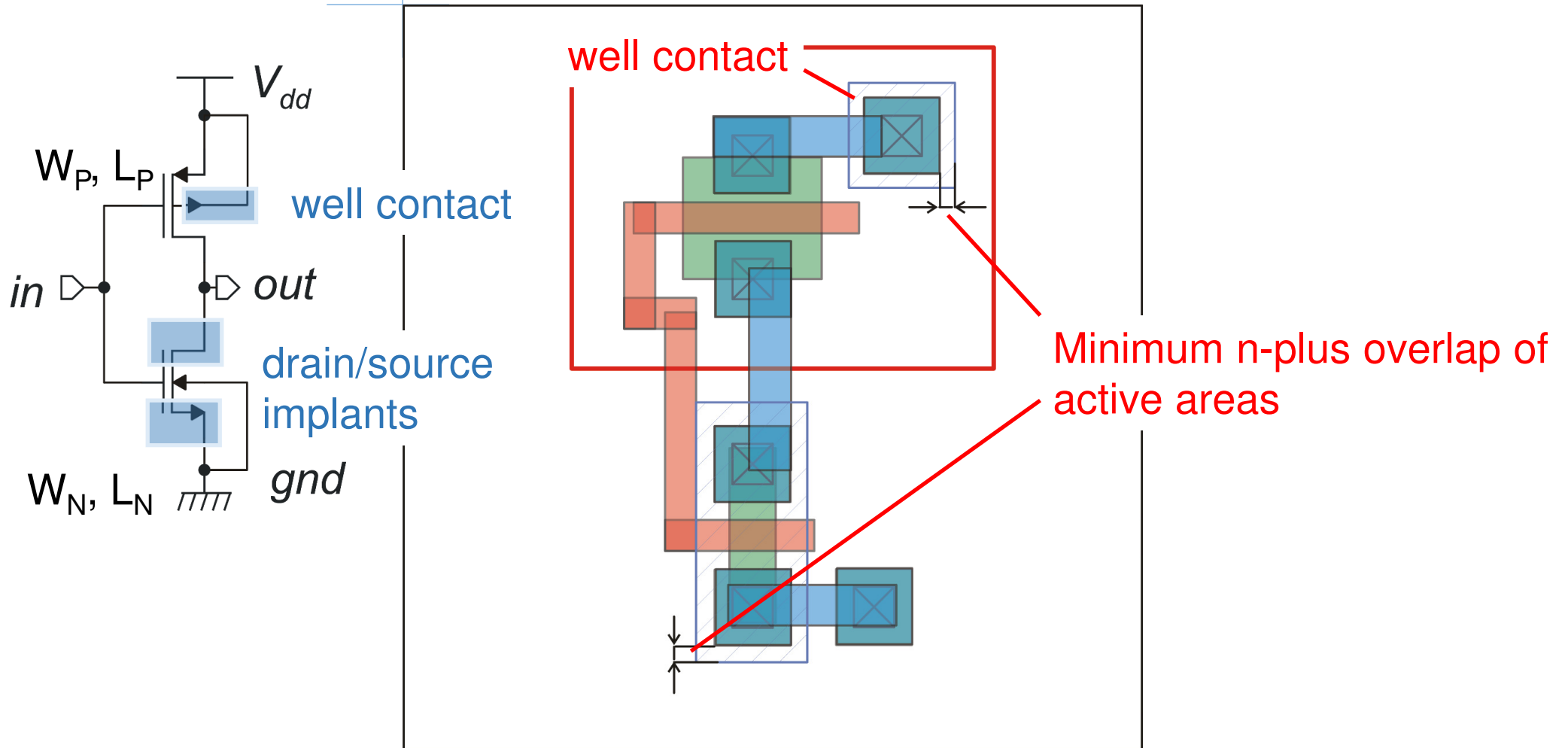


Resize the n-well to comply with all active margins.
Connect sources to bodies

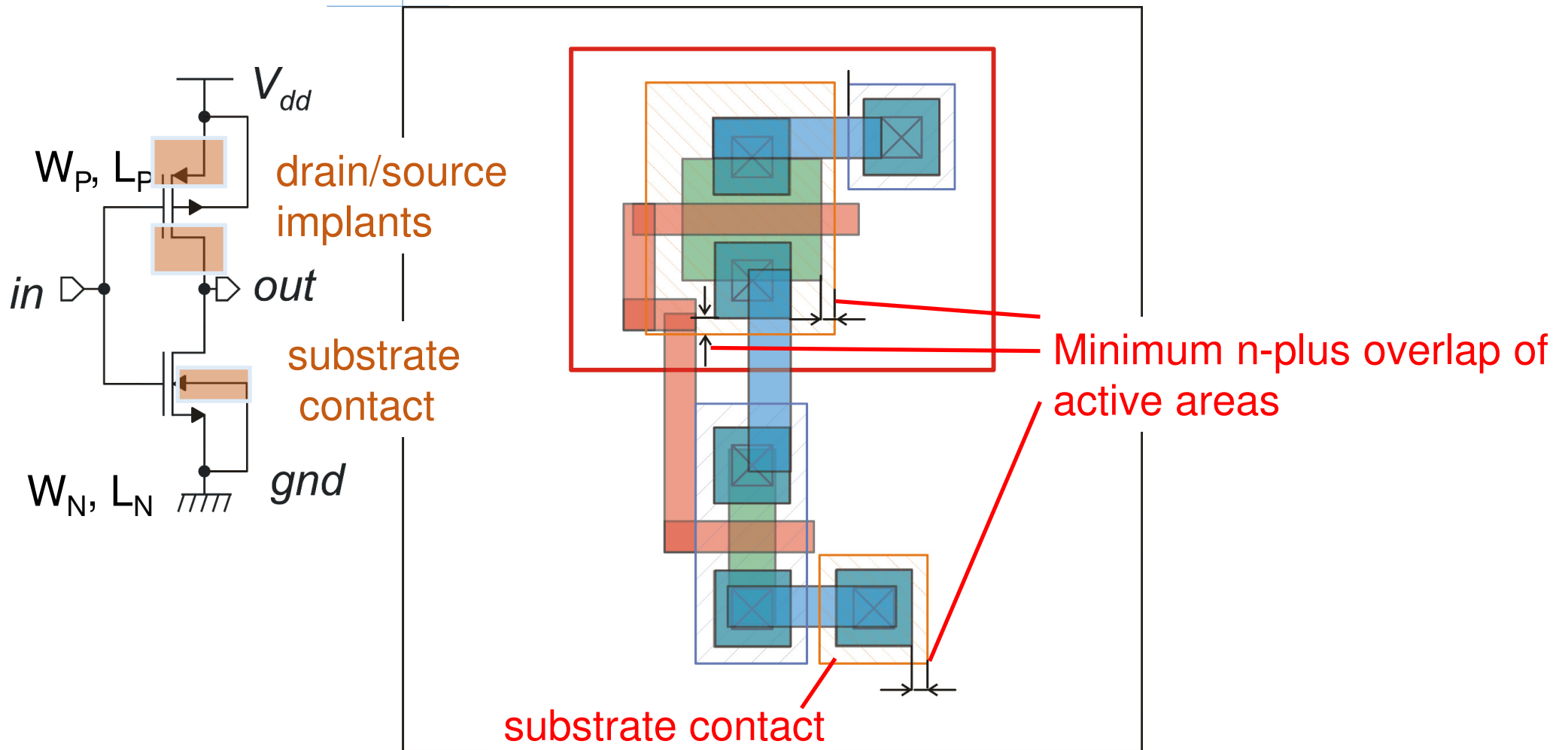


Minimum active to well margin

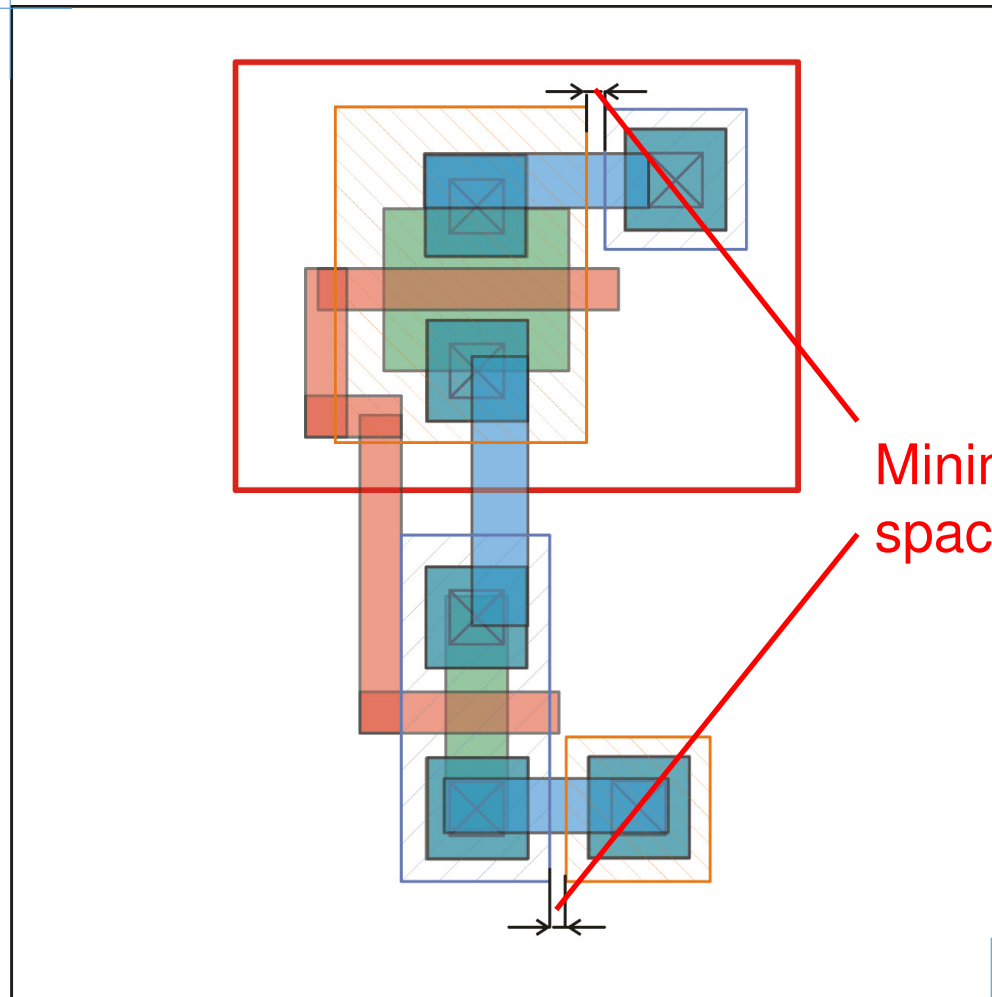
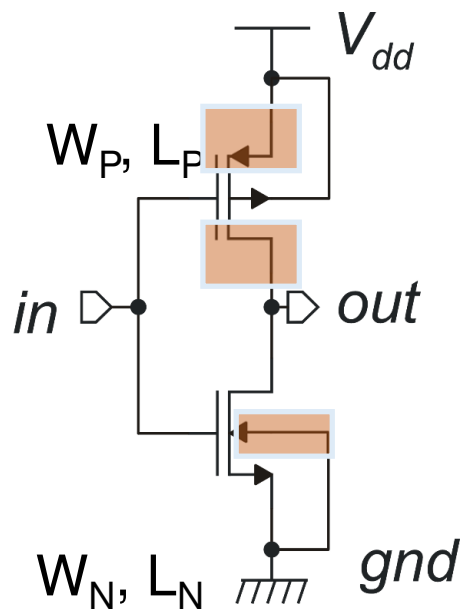
Cover all n-plus active areas with n-plus implant



Same thing with p-plus active areas (p-plus implant)

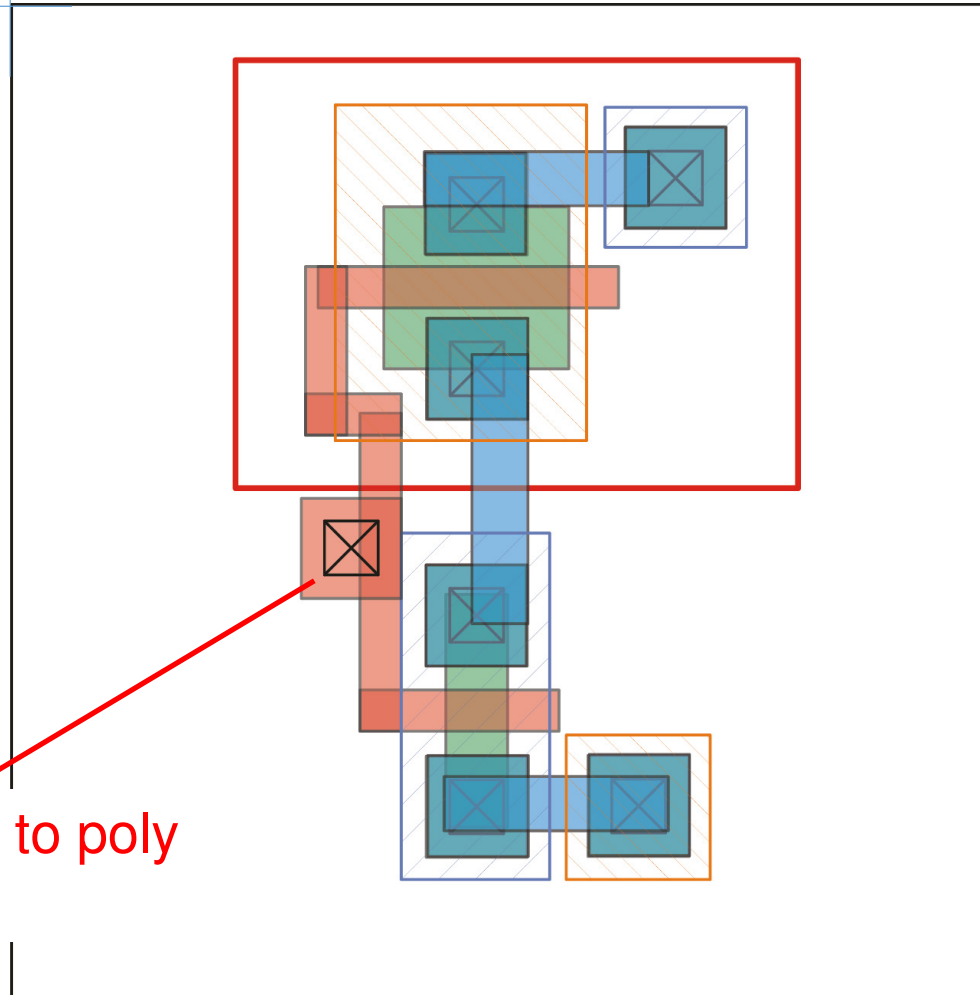
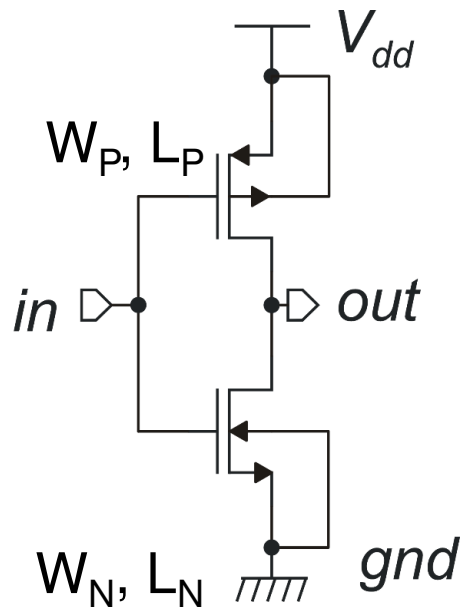


Same thing with p-plus active areas (p-plus implant)



Minimum n-plus to p-plus spacing

Create a poly-metal1 contact if required



Margin of contact to poly
on every-side

Create a poly-metal1 contact if required

