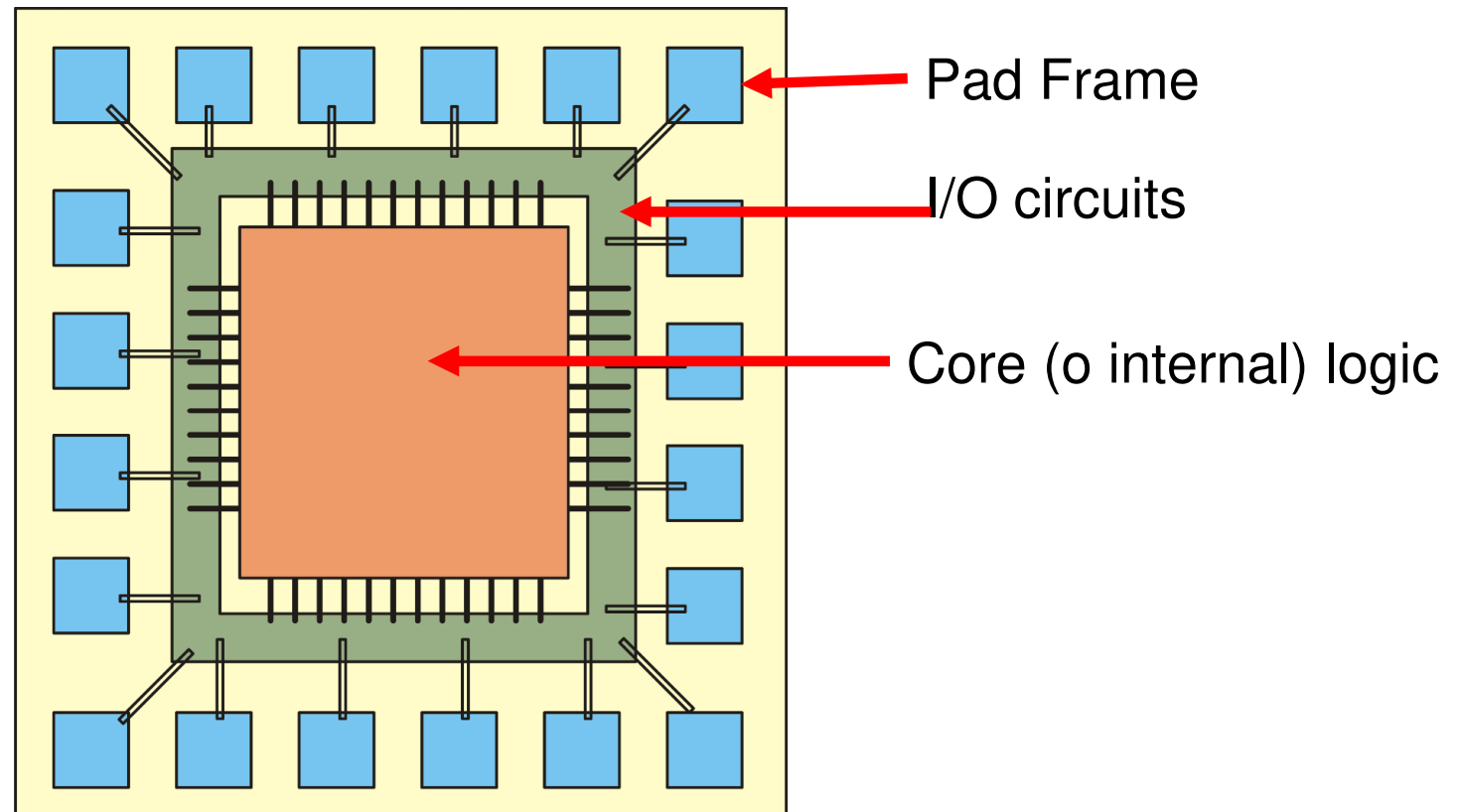
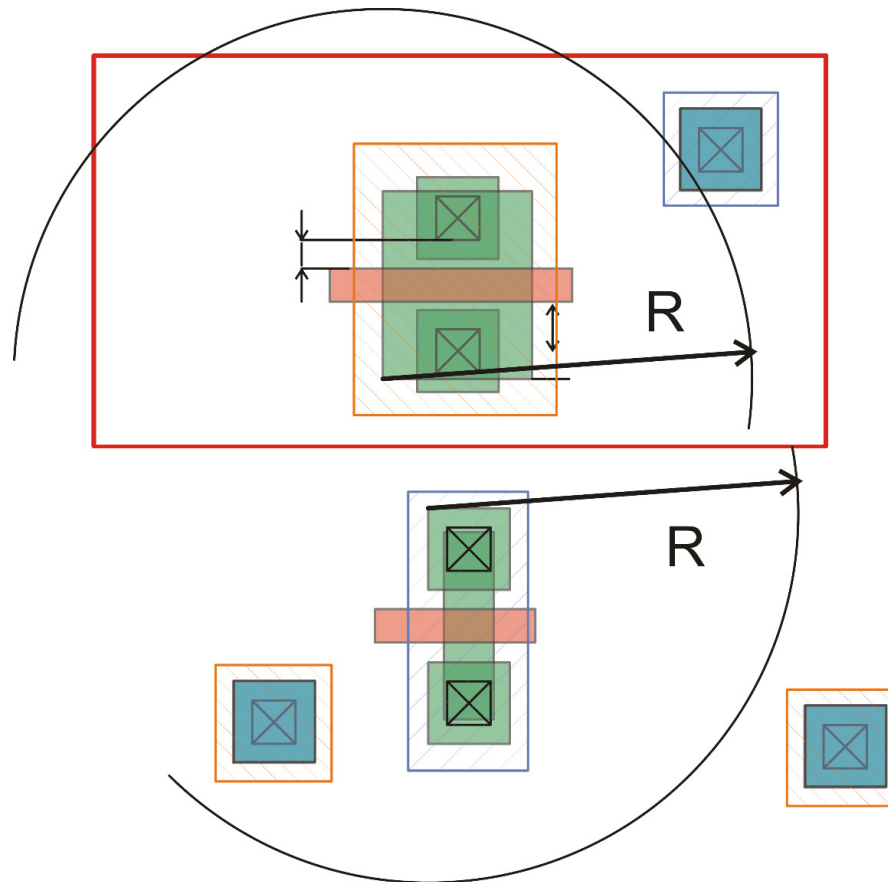


# Typical structure of a digital chip



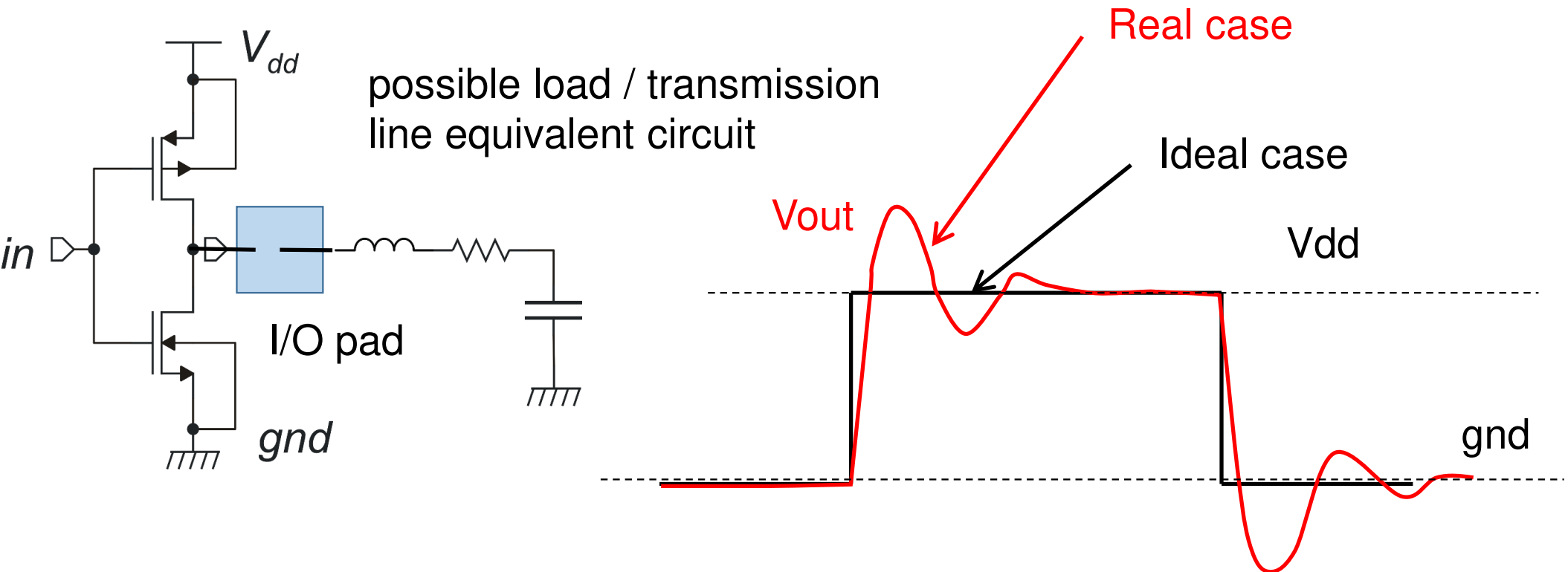
## Latch-up layout rules: core logic



Every part of a p-active area in an n-well must "see" at least one well-tap with a maximum distance  $R$

Every part of an n-active area in the substrate (p-well) must "see" at least one substrate-tap with a maximum distance  $R$

## I/O circuits: over-voltage risk

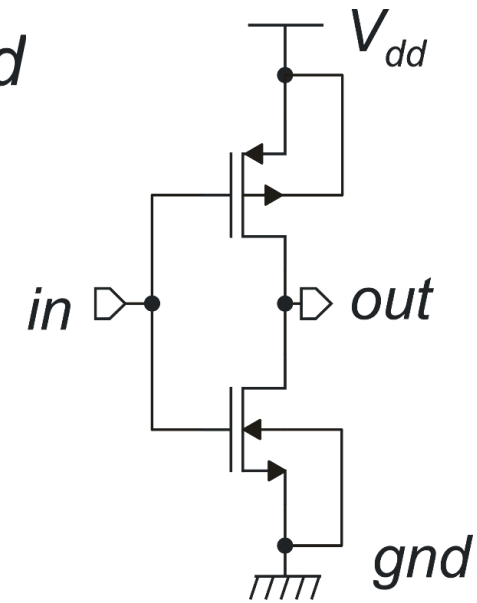
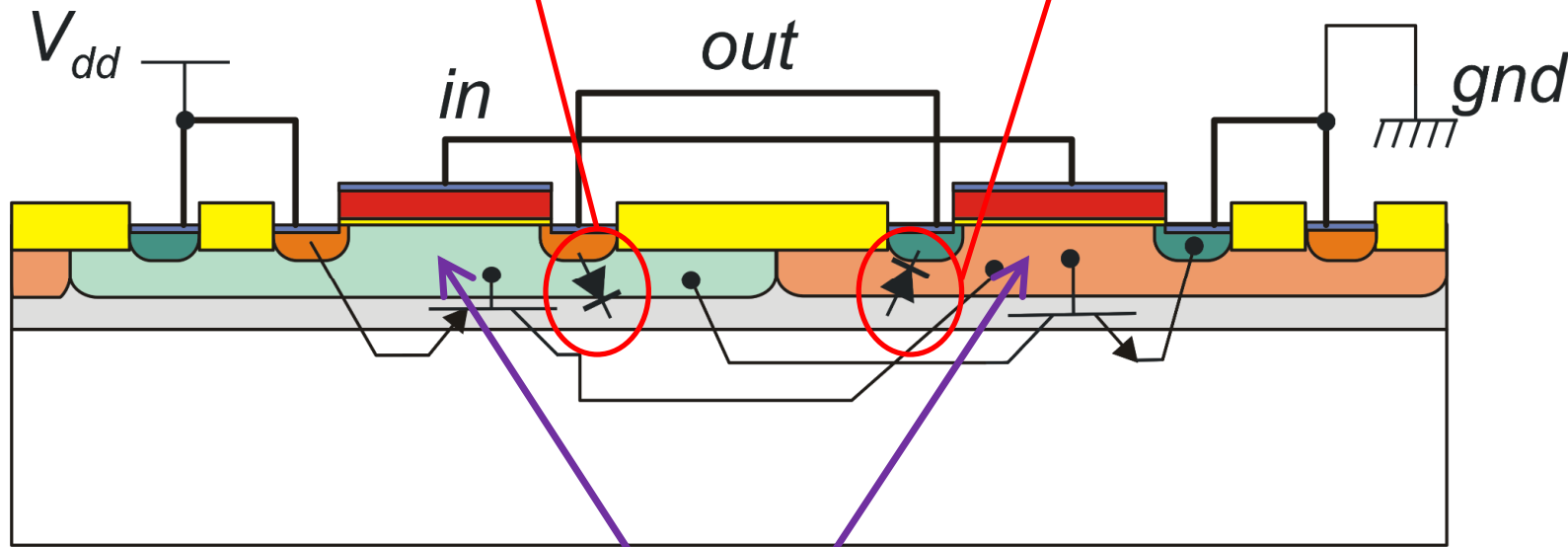


In I/O circuits, the output termination can exceed the  $V_{dd}$  or  $gnd$  rails. This introduces additional risk of latch-up

# Injection of minority carriers

when  $V_{out}$  exceeds  $V_{dd}$ ,  
this diode is turned on

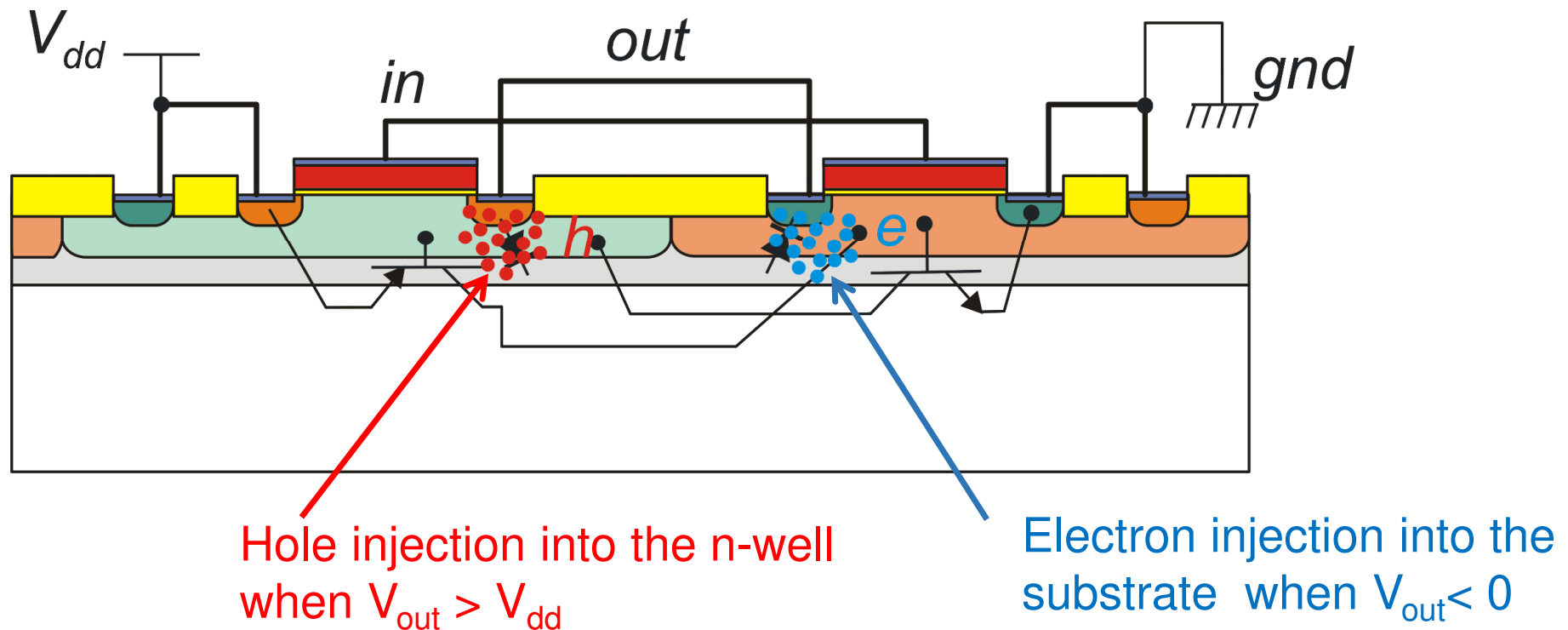
when  $V_{out}$  drops below  $gnd$ ,  
this diode is turned on



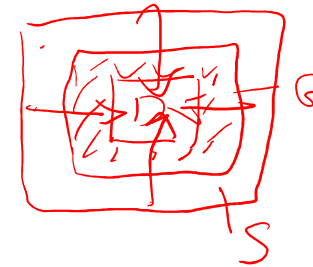
Well: bases of the pnp BJT (collector of npn BJT)  
Substrate: bases of the npn BJT (collector of pnp BJT)

## Injection of minority carriers

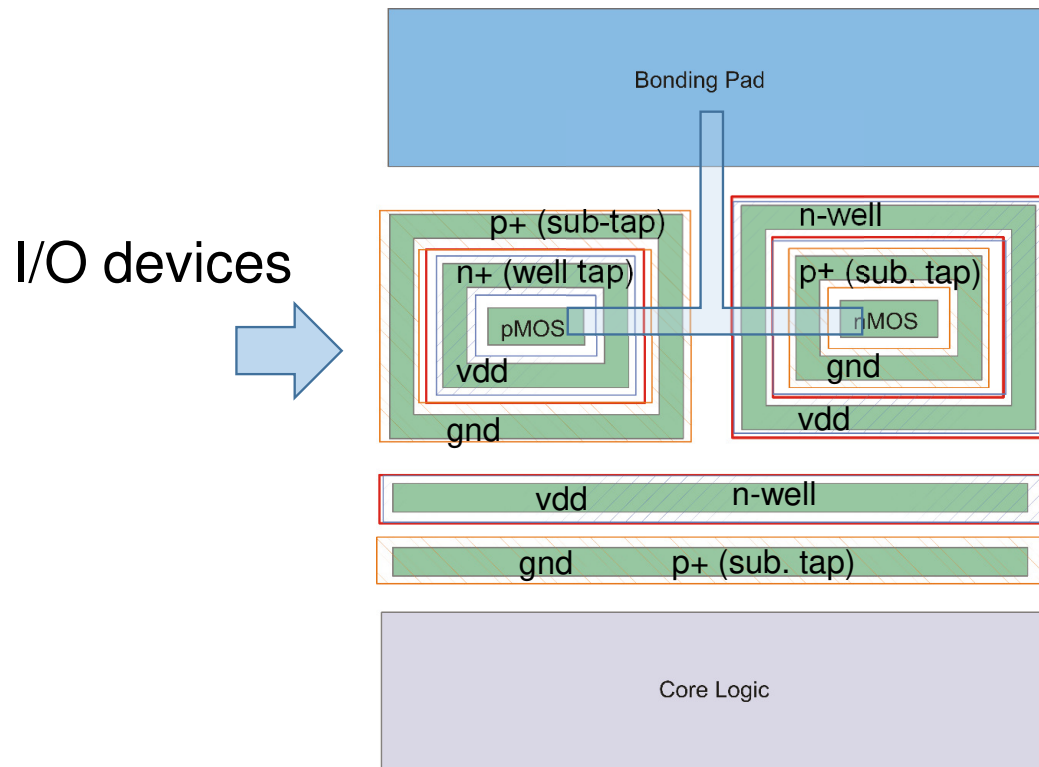
Injection of minority charge carriers into the parasitic BJTs bases may trigger the latch-up phenomenon



# I/O devices: Guard Rings



I/O circuits require additional protection against latch-up



Guard rings are placed around the I/O devices in order to:

- Reduce the resistance between drain/body diffusions to gnd (nMOS) or Vdd (pMOS)
- Collect most of the minority carriers injected by one device before they reach neighboring devices

These guard rings further reduce the effects of the I/O devices on the core logic

## Analog and mixed signal chips

- For the analog section of a System on a Chip, it is not convenient or even impossible to divide the circuit into a core section and an I/O section.
- However, the same rules illustrated for digital chips apply to the output devices of the analog cells (for example, operational amplifiers), which are connected to output pads. High density of substrate / well contacts, guard-rings and particular layout configurations are common practice for the output devices of analog circuits.