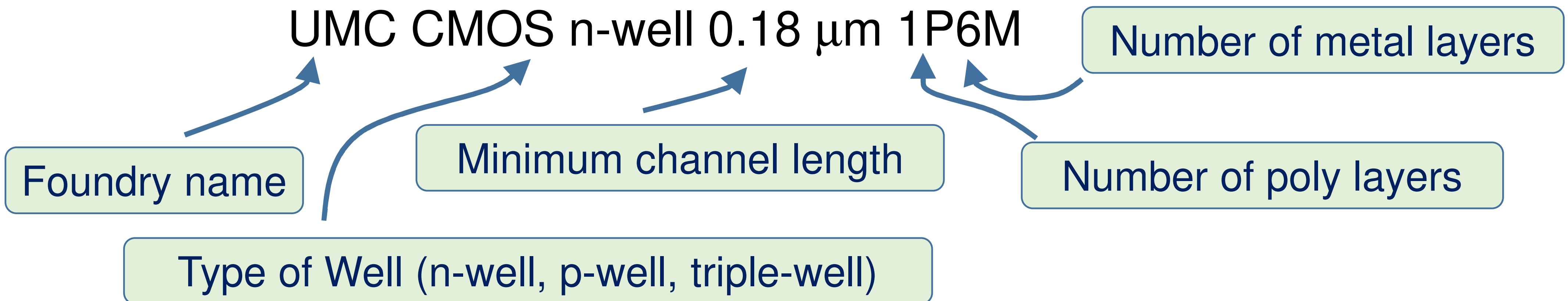
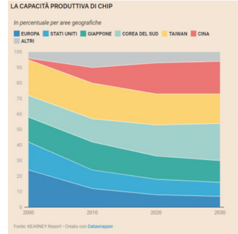
The CMOS Process

- **Planar CMOS** process is used up to the 28 nm technology node.
- For later technology nodes, 3D CMOS MOSFETs (**FinFETs**) are used.
- Planar CMOS processes are still extensively used for **analog** and **mixed-signal** ICs.

Classification of planar CMOS processes: example



Semiconductor Fabrication Plants



TSMC
GF
UMC
INTEL
SAMSUNG
STM

LA CAPACITÀ PRODUTTIVA DI CHIP

In percentuale per aree geografiche

EUROPA · STATI UNITI · GIAPPONE · COREA DEL SUD · TAIWAN · CINA · ALTRI

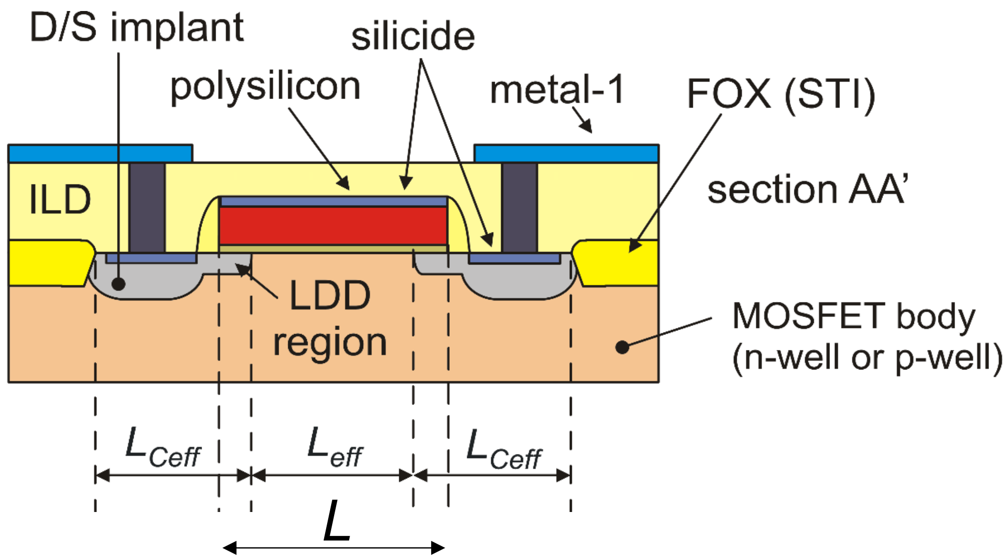
100, 90, 80, 70, 60, 50, 40, 30, 20, 10, 0

2000, 2010, 2020, 2030

Fonte: KEARNEY Report • Creato con Datawrapper

Taiwan:
- TSMC
- UMC
- MICRON
- …

Technology node

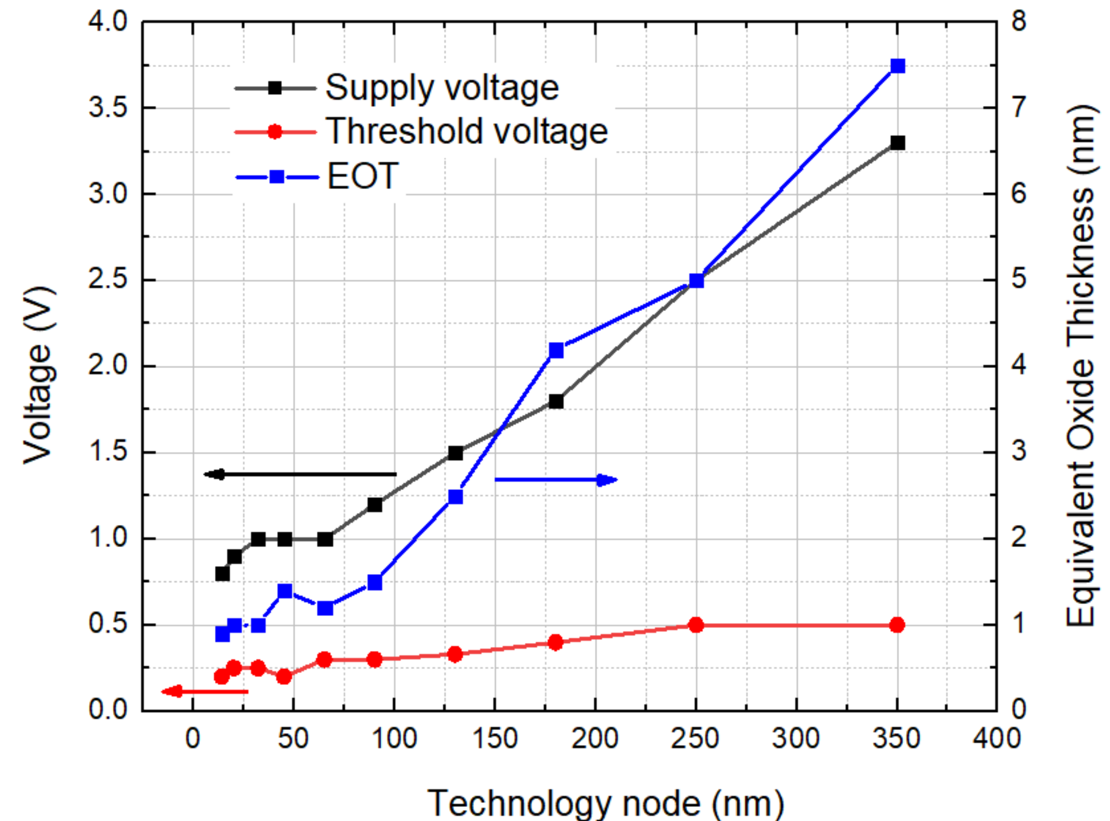


Year	Node (nm)	Half-pitch (nm)	Gate Length L_{eff} (nm)
1997	250	250	250
1999	180	239	140
2001	130	150	65
2003	90	90	37
2005	65	90	32
2007	45	68	38
2009	32	52	29

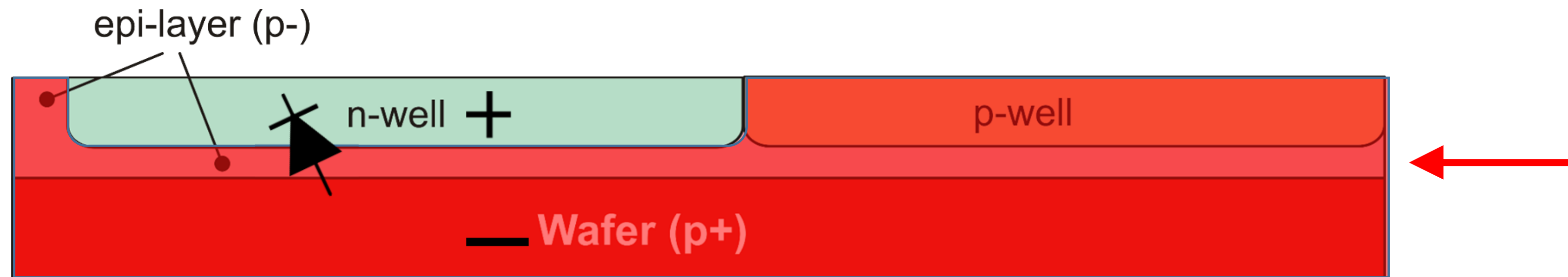
- Until 2000 the technology node represented the minimum channel length (gate length)
- After 180 nm the technology node started representing the half-pitch
- Since 2017 the technology node does not represent any geometrical dimension

Technology Scaling

- Smaller W and L → Higher transistor density, higher f_T
- Lower Vdd and Vth → Lower dynamic power consumption, higher static power consumption
- Lower tox → Higher gate leakage (from SiO2/PolySi to High-k materials/metal gate around 45 nm)

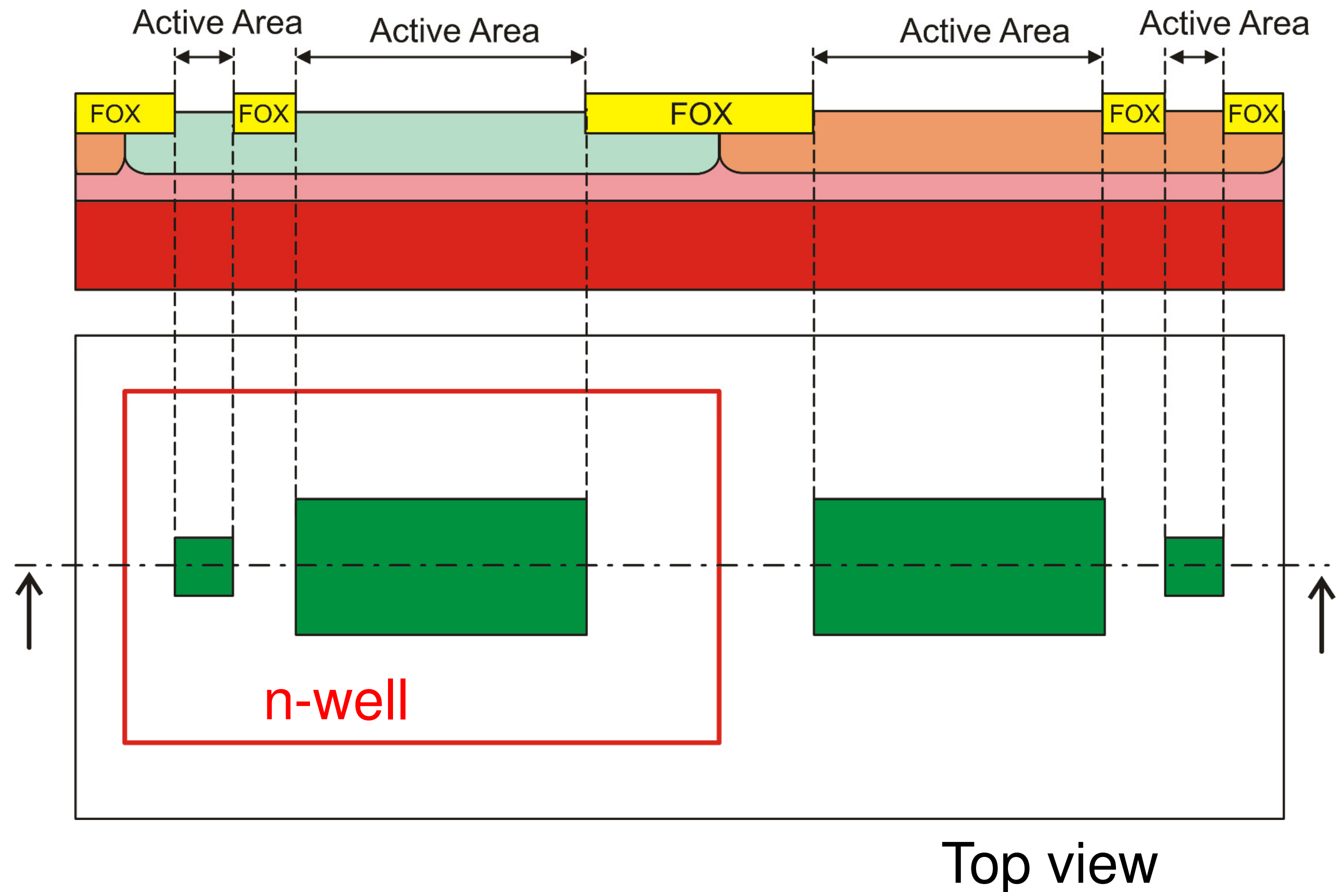


Simplified designer's view of a CMOS Process



- We are considering a simple n-well (twin-Tub) 1P2M process
- The starting substrate is **p-type**: all p-wells are shorted together since there are no insulation junctions with the substrate.
- N-wells are insulated from the substrate if the latter is biased at the lowest voltage in the circuit.
- A very lightly doped epitaxial layer is often present on top of a strongly doped wafer. P-wells are necessary to obtain the optimal doping for n-MOSFETS.

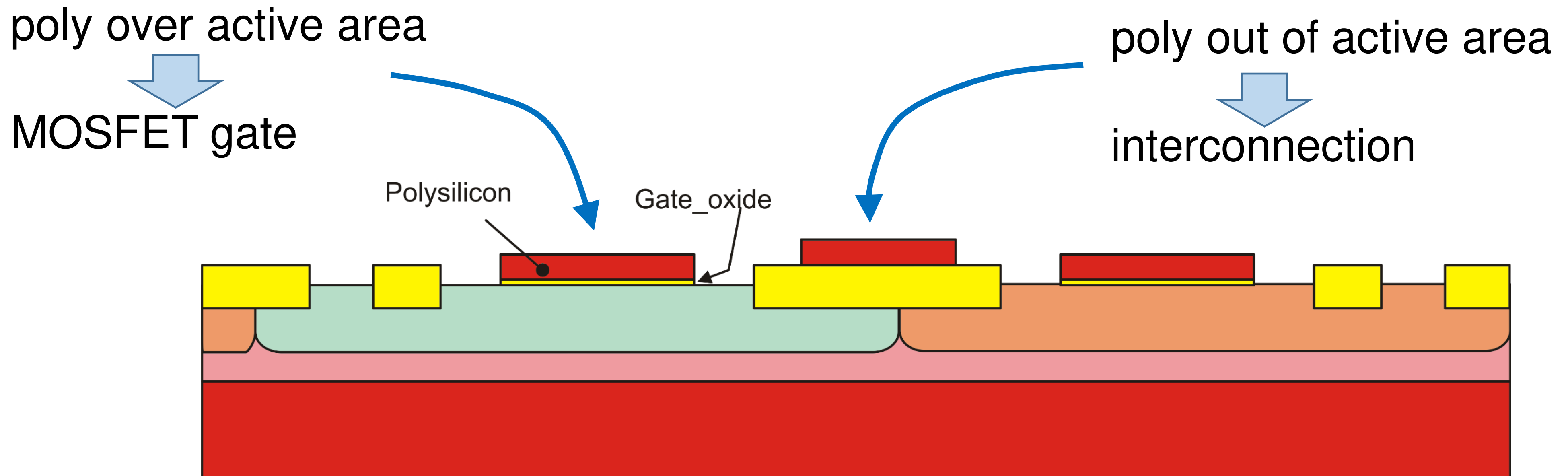
The active areas



Used Layers

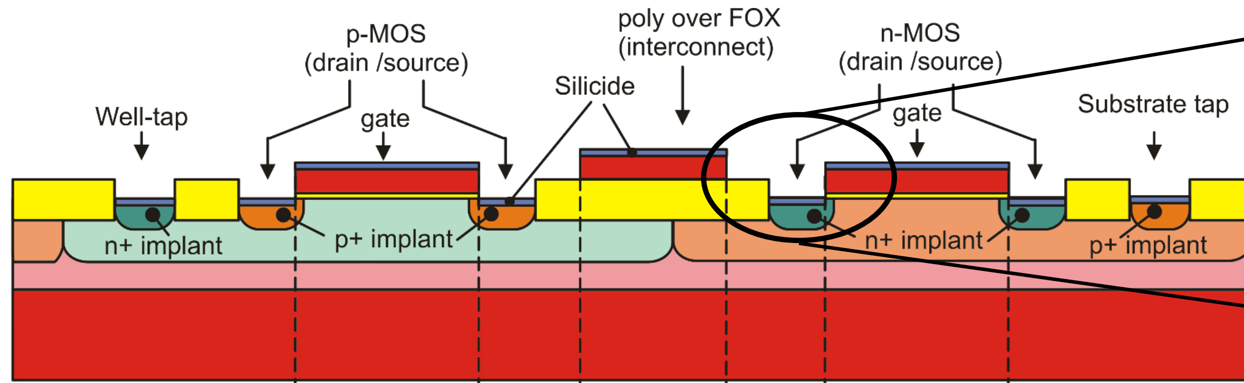
- Active areas are all of the same type.
- They are *specialized* by other layers (e.g. n-well).
- p-wells are often drawn automatically as **not(n-well)**

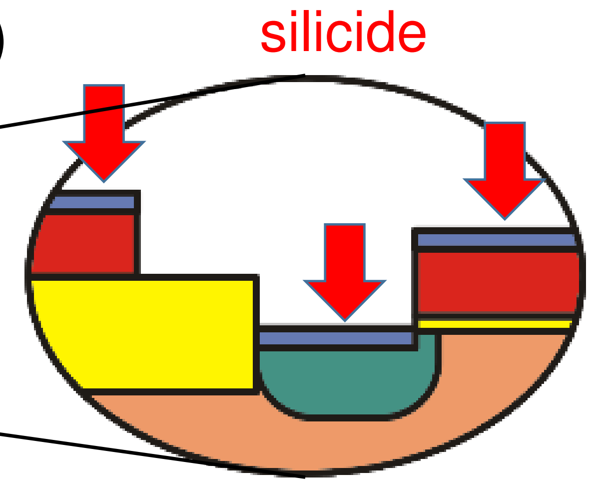
Polysilicon and gate oxide

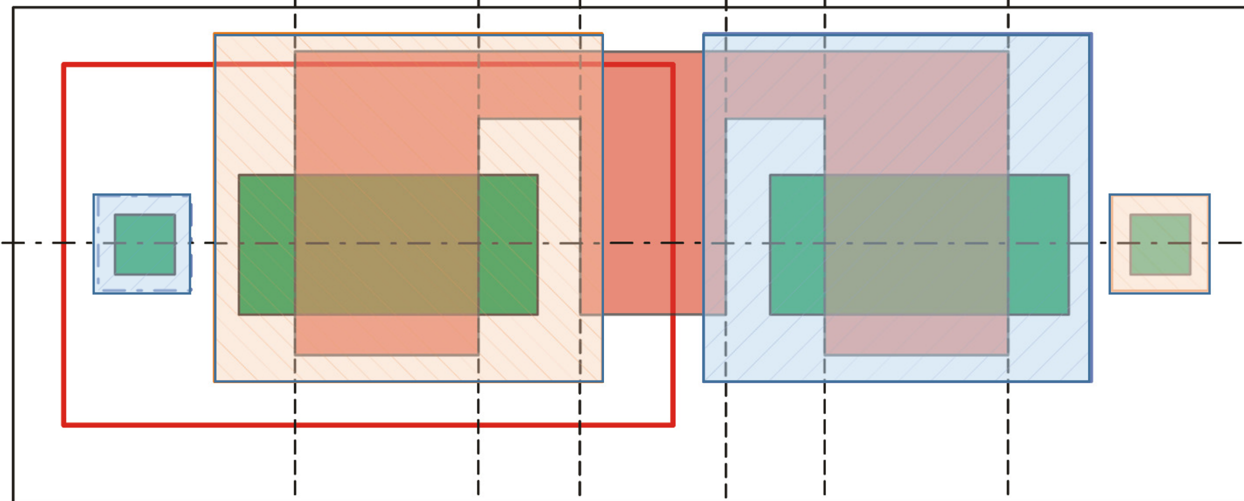


- The gate (thin) oxide is grown on **all** active areas.
- After that, it is covered by the polysilicon layer
- When the poly is patterned, the gate oxide remains only where polysilicon remains, forming the gate.
- Only one layer (poly) is required to control the final result of this step.

FEOL (Front-End Of the Line)



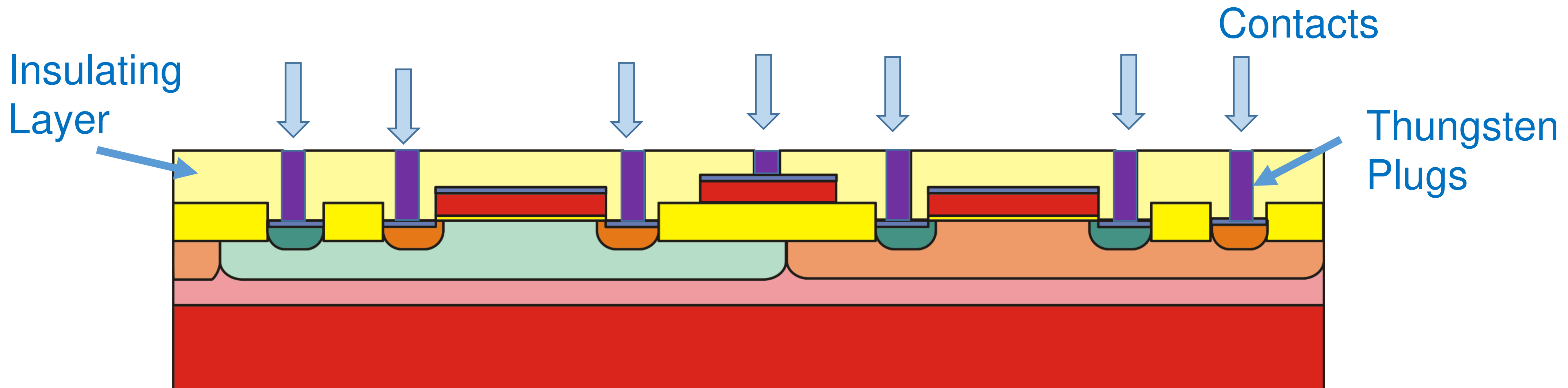




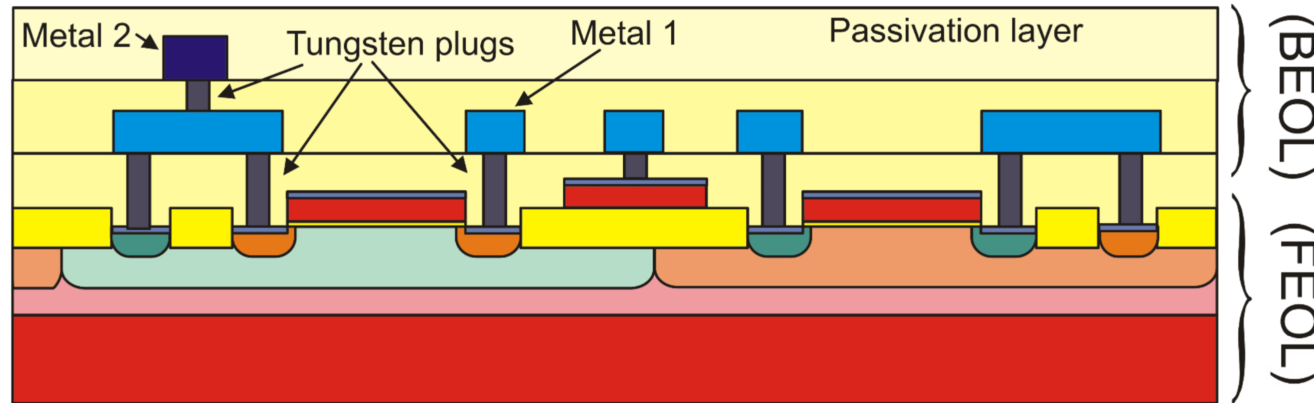
N-well
Active
Poly
N-Plus
P-plus

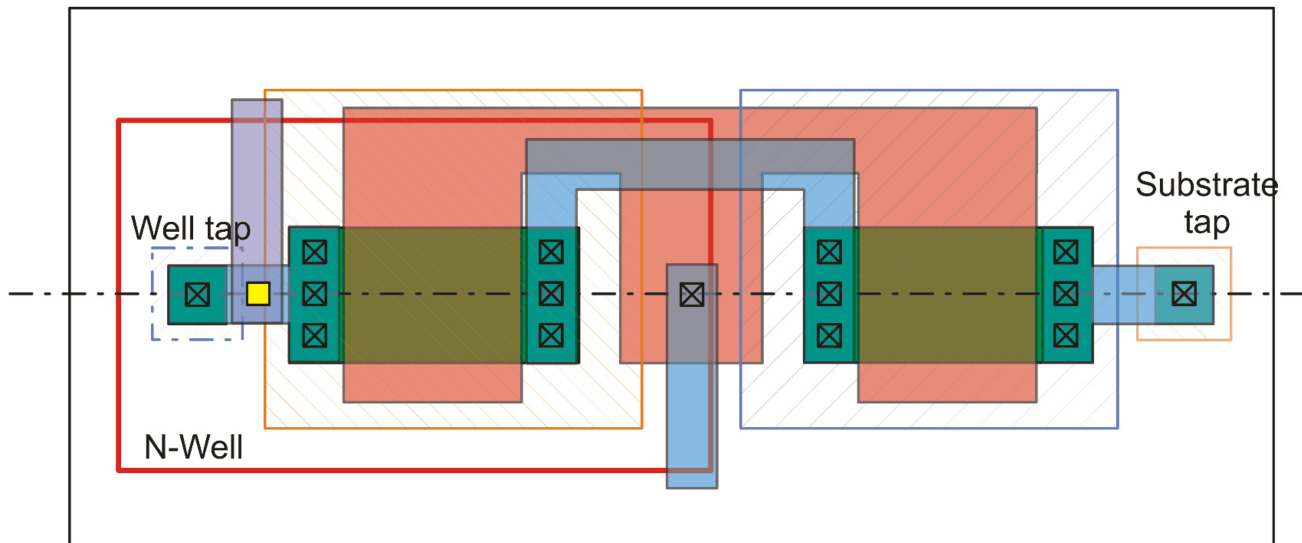
BEOL (Back End Of the Line) - Contacts

- All devices created in the FEOL are covered by an insulating layer and holes are opened only where we want to contact them. These opening are the **CONTACTS**
- Contacts can reach active areas (p+ or n+ doped portions of the substrate) or polysilicon (over the FOX).
- Direct contact of polysilicon over the gates is not allowed

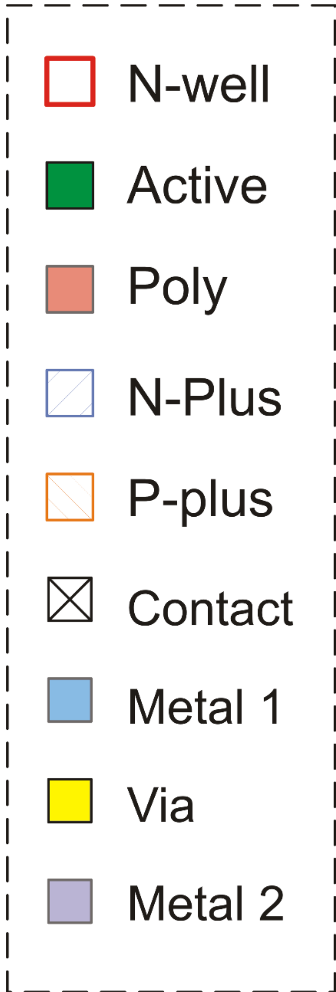


BEOL: The interconnections

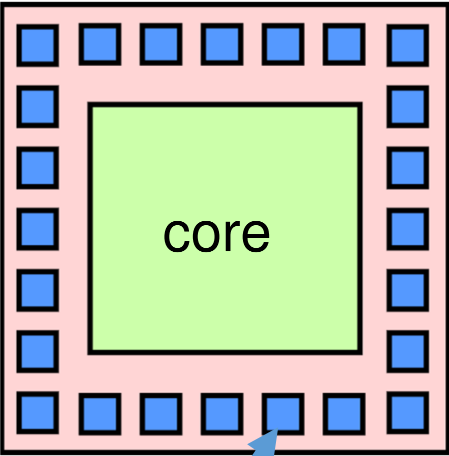




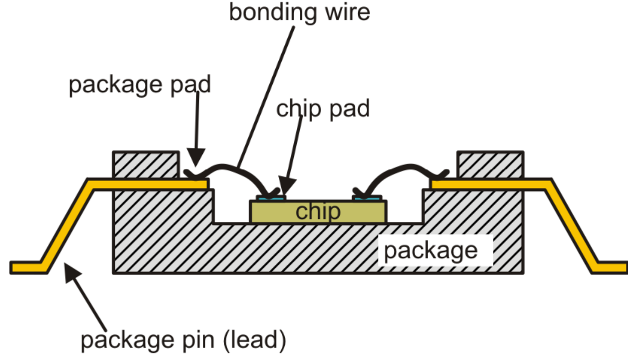
Used Layers



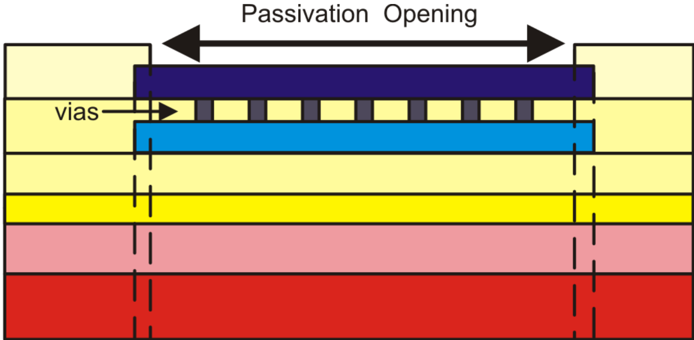
Bonding Pads

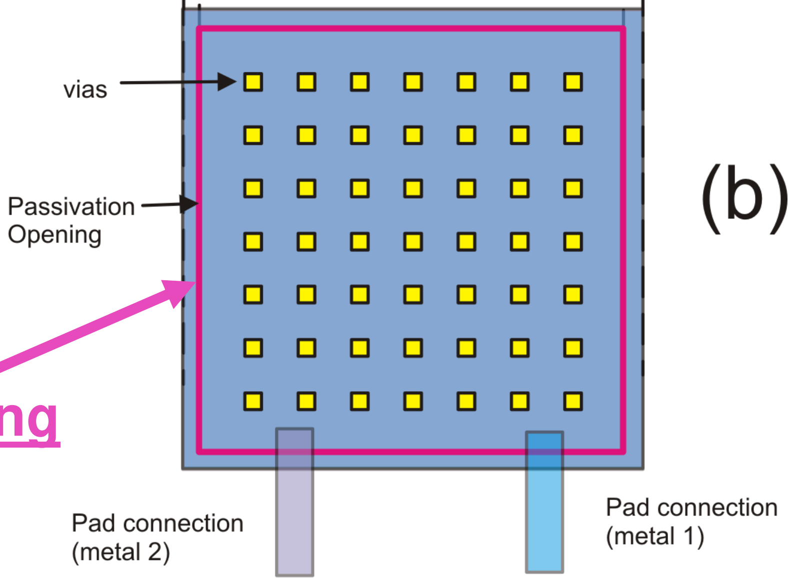


pads
(pad frame)



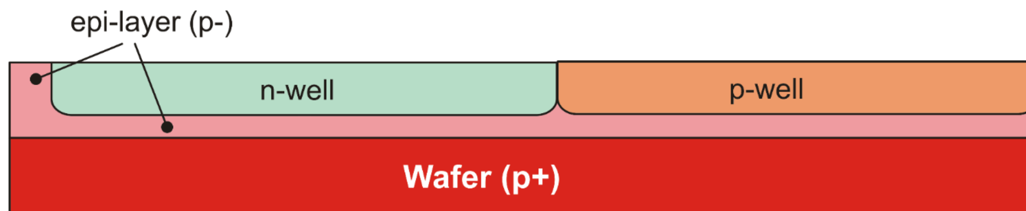
(a)



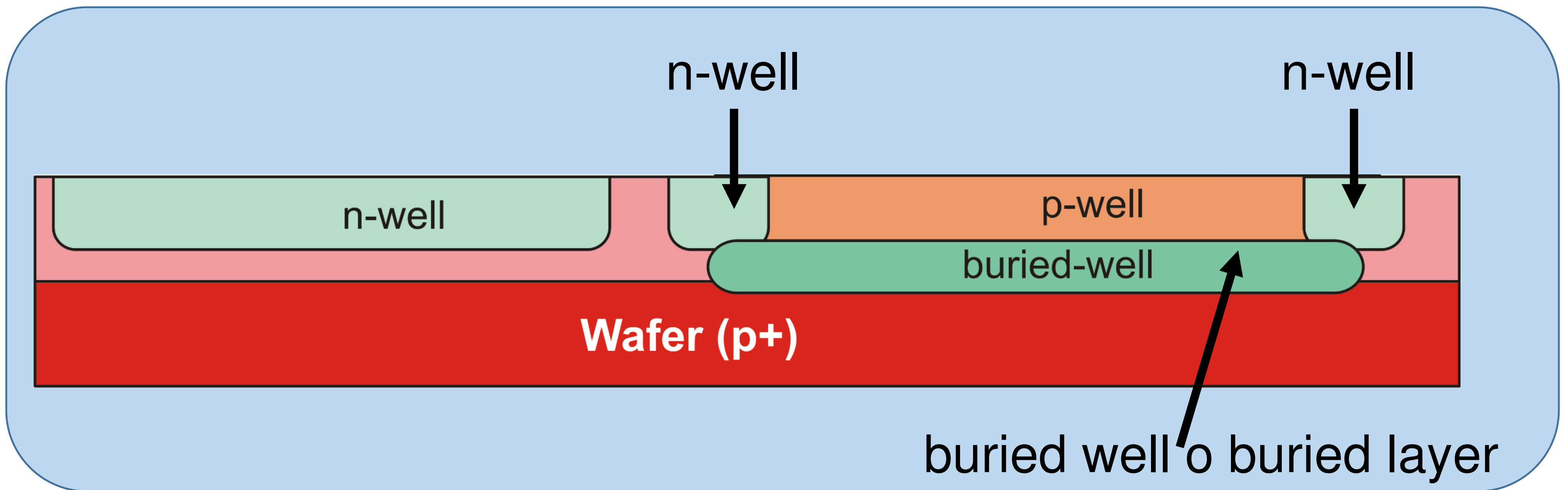


Layer: Passivation Opening

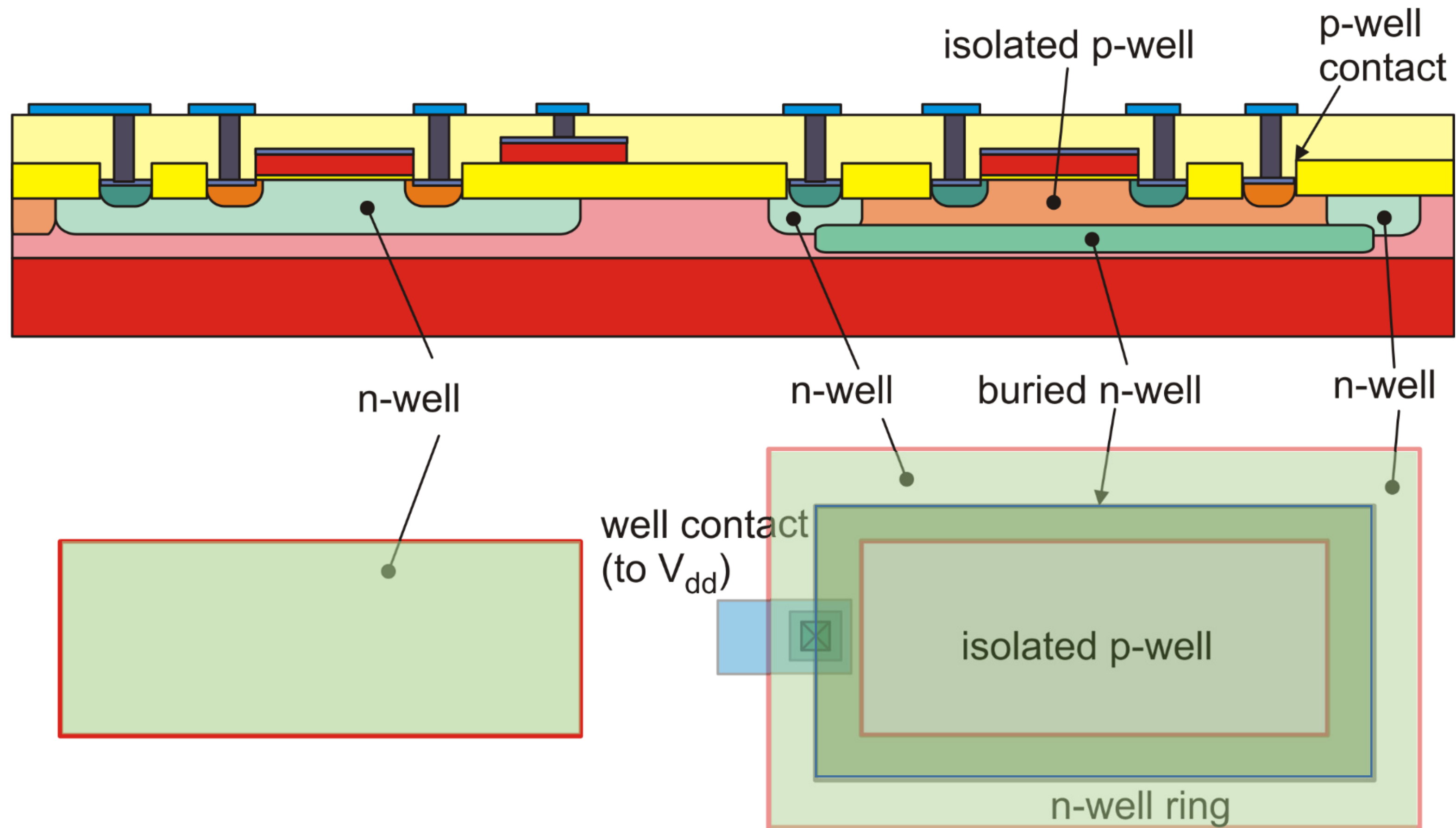
The Triple Well



n-well twin tub



Triple Well: Multiple PWells and NWells at independent voltages



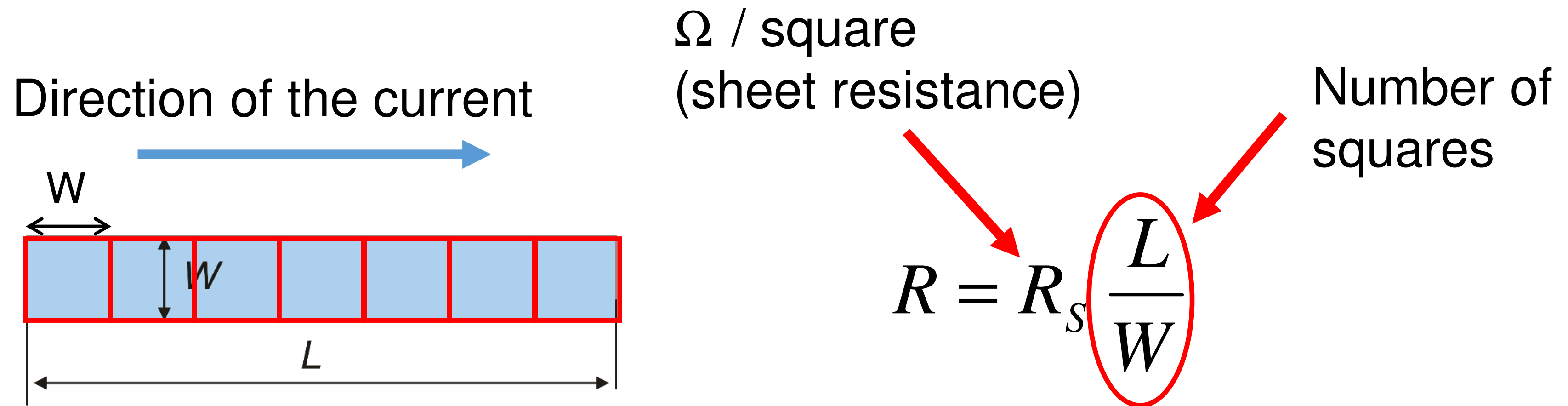
Bipolar processes

Technology	Available Devices	Notes
Bipolar	Vertical NPN, Lateral PNP	Used for precision and/or fast amplifier. **Si-Ge** versions for RF applications
Complementary Bipolar	Vertical NPN, Vertical PNP	
BiFet	BJTs and JFETs	Used for precision / low bias current amplifiers

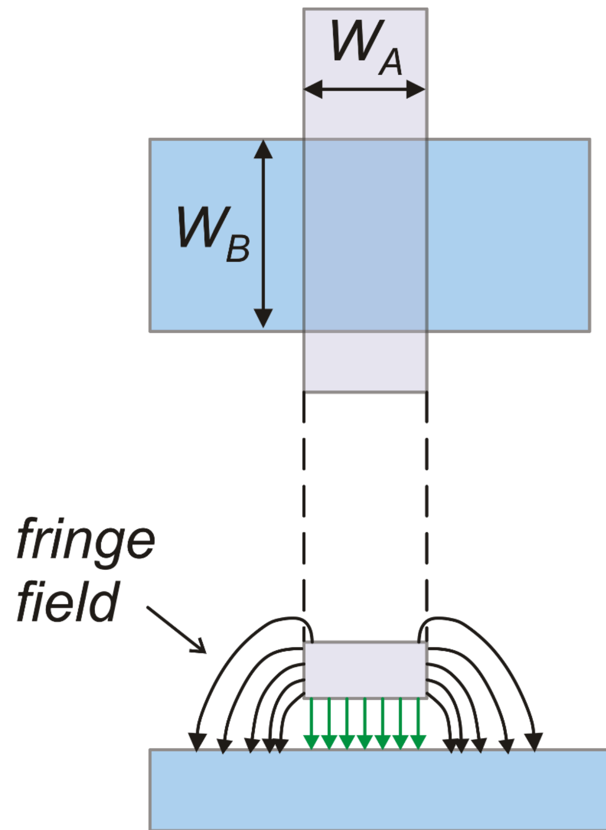
BiCMOS, BCD, SOI

Technology	Available Devices	Notes
BiCMOS	CMOS + BJTs	Mixed Signal ICs High speed digital line drivers
BCD	Bipolar, CMOS, DMOS	Smart Power
SOI Silicon on Insulator.	As CMOS, BiCMOS or BCD	High Voltage and Rad Hard (e.g. space applications)

Resistances in planar ICs



Vertical and lateral capacitances



$A = W_A \cdot W_B$ Area

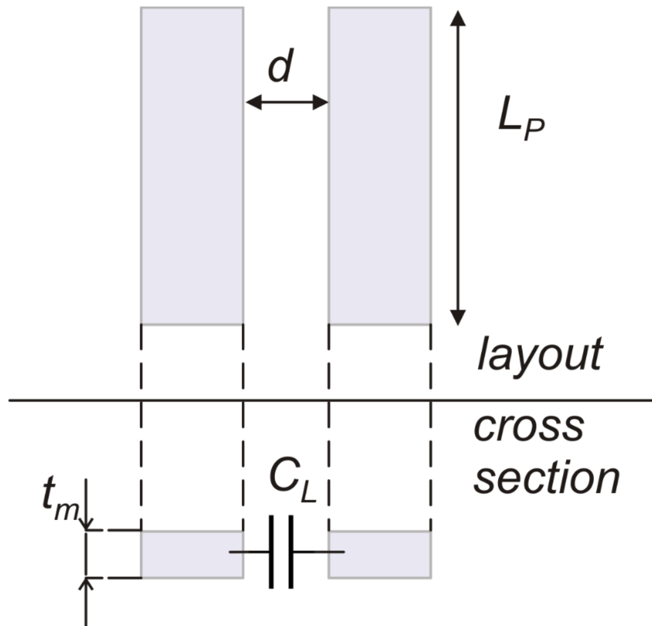
$P = 2W_A + 2W_B$ Perimeter

$$C_V = k_A A + k_P P$$

Capacitance per unit area

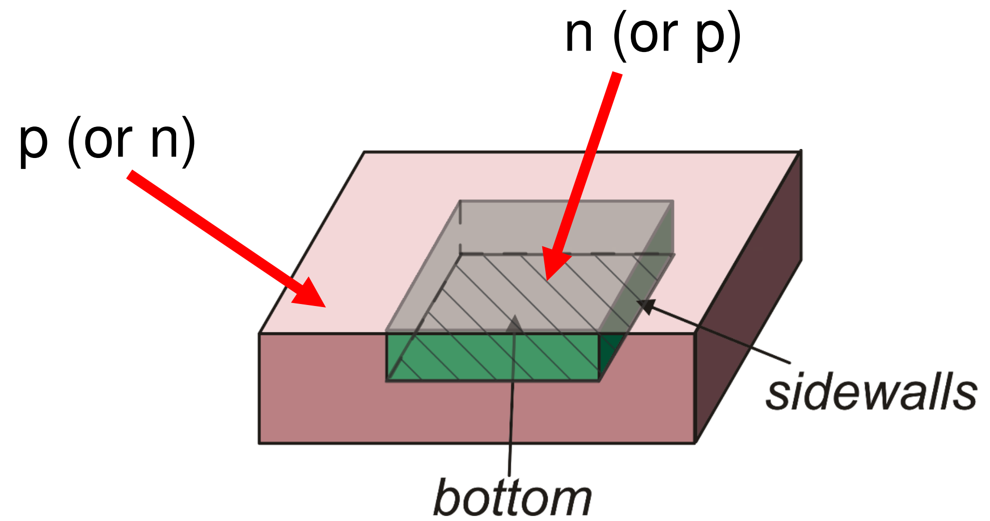
Capacitance per unit perimeter
(Fringe capacitance)

Lateral and Junction Capacitances



Lateral

$$C_L = \varepsilon_d \frac{L_p \cdot t_m}{d}$$



Junction

$$C_{n-p} = C_J A + C_{JSW} P$$