The Meyer Model Revisited: Why is Charge Not Conserved?

MEHMET A. CIRIT, MEMBER, IEEE

Abstract—**A new approach to computer simulation of capacitance effects in MOS transistors is presented. It is shown that charge non-conservation is the result of faulty mathematical modeling of the capacitive nonlinearities in the SPICE circuit simulator, and is not intrinsic to any specific charge or capacitance model. We describe the correct mathematical model. The results of computer simulations using the Meyer capacitance model, which conserves charge, are given for some test circuits.**

INTRODUCTION

A CAPACITANCE model to describe the transient behavior of MOSFET's, including only the first-order effects, was developed by Meyer [1] and has been used in various circuit simulators like SPICE [2] and its derivatives. Although this model is simple and sufficient for most circuit applications and has been used successfully over the years, it has been reported that it fails in some applications where the charge storage properties of MOSFET's are important. These problems, commonly known as charge non-conservation, especially show up in MOS charge pumps, silicon-on-sapphire (SOS) circuits [3], and in the simulation of static RAM's and switched-capacitor circuits [4].

The Meyer model represents the charge storage properties of MOSFET's through three nonlinear capacitances:

$$C_{gd} = \frac{\delta Q_g}{\delta V_{gd}}$$

$$C_{gs} = \frac{\delta Q_g}{\delta V_{gs}}$$

$$C_{gb} = \frac{\delta Q_g}{\delta V_{gb}} \tag{1}$$

where Q_g is the total gate charge, and V_{gd}, V_{gs}, V_{gb} are the bias voltages referenced to the gate terminal. The transient currents are given by

$$i_{gs} = C_{gs}\dot{V}_{gs}$$

$$i_{gd} = C_{gd}\dot{V}_{gd}$$

$$i_{gb} = C_{gb}\dot{V}_{gb} \tag{2}$$

Manuscript received July 12, 1988; revised February 2, 1989 and April 25, 1989. The review of this paper was arranged by Associate Editor J. G. Fossum.

The author was with Sierra Semiconductor Corporation, San Jose, CA. He is now with Adaptec Inc., Milpitas, CA 95035.

IEEE Log Number 8929546.

which depend on the terminal voltages V_{gd}, V_{gs}, V_{gb} in general.

Objections raised to the Meyer model can be summarized as follows:[1]

1) lack of C_{bs} and C_{bd} capacitances resulting from substrate charges;
2) non-conservation of charge, when used in transient circuit simulation;
3) modeling inaccuracies, specifically with regard to non-reciprocal capacitances.

These objections to the Meyer model are disjoint, have nothing to do with each other to a first order. However, they have often been discussed together in the literature, causing confusion. For example, the Meyer model can be easily extended by adding C_{bs} and C_{bd} capacitors which are derived from the substrate charge, without compromising the gate capacitance terms.

Ward [5] identified the use of nonlinear capacitances as the source of non-conservation of charge problems in transient circuit simulation. He introduced a strictly charge based model which eliminated this problem. He also showed that this model can correctly predict the observed non-reciprocal device capacitances. In addition, Ward's model predicts the low-frequency capacitances correctly while the Meyer model does not. Other causes of the charge conservation problems have been identified, such as premature convergence of the Newton–Raphson iteration, and the truncation errors which result during the conversion of differential algebraic circuit equations into algebraic equations [4].

Higher order and more accurately charge oriented models are the state-of-the art in modeling the transient behavior of MOSFET's [6]–[8]. However, the Meyer model is a simple first-order model which has its place in the hierarchy of models of varying complexity and sophistication. It is quite simple to enhance it with C_{bs} and C_{bd}. As we shall show in the following it can conserve charge with proper implementation in a circuit simulator. Therefore, the only objection to the Meyer model remains to be its accuracy due to reciprocity.

The Meyer model is a first-order inaccurate approximation to MOS capacitances. For the analysis and design of circuits which do not exhibit a sensitivity to charge conservation, it is still a valuable model. In addition it is

[1]The author would like to thank the referees for clarifying these points.

0278-0070/89/1000-1033$01.00 © 1989 IEEE

reported to predict the high frequency capacitances more accurately than Ward's model. Although non-reciprocal capacitances are known to be the best fit to experimental data [9], [10], it is also known that a network with non-reciprocal capacitances can generate infinite power at infinite frequency [11]. Therefore, it may be necessary to switch between the current and charge oriented models depending on the frequency domain [12].

In the following we shall show that charge non-conservation problems attributed to the Meyer, or any other nonlinear capacitance model, are actually the result of inaccurate mathematical modeling of the model by the simulator, rather than being a shortcoming of the model itself. After all, the very derivation of the Meyer model assumes that the charges in the channel and gate add up to zero. Because of the nonlinearity and the dependence of Meyer capacitances on several variables, the formulation adopted in simulators like SPICE does not include some first-order terms associated with the model. We shall show that the proper representation of each Meyer capacitor, in a circuit simulator using Newton–Raphson iteration, needs a linear capacitor, a "resistor," and two current sources.

The corrected model has been implemented in Lspice. Lspice is an analog circuit simulator product offered as an option to Silicon Compiler Systems's Lsim[2] mixed-mode analog and digital simulator [13]. We present the simulation results on a charge pump and the switched-capacitor circuit used by Yang *et al.* [4]. With proper representation of the nonlinearities charge non-conservation problem disappear. We also give the small signal representation of the Meyer model and describe its implementation in Newton–Raphson iteration based circuit simulators.

The New Implementation

Unlike the previous approaches as used in SPICE and in the new charge oriented models, our implementation of the Meyer model is strictly current oriented, that is, we do not keep track of the charges stored in the capacitors. In SPICE, each capacitor is assigned a total charge, the time derivative of which is equal to the capacitive transient currents:

$$\begin{aligned} i_{gs} &= \dot{Q}_{gs} \\ i_{gd} &= \dot{Q}_{gd} \\ i_{gb} &= \dot{Q}_{gb}. \end{aligned} \tag{3}$$

Charges Q_{gs}, Q_{gd}, and Q_{gb} are found by numerical integration of the currents defined in (2). This approach would be perfectly acceptable if the calculated charges depended only on the terminal voltages of the associated capacitors. This is not the case with the Meyer model. Forcing the Meyer capacitances to behave like a charge storage element results in the neglect of some first-order terms during Newton–Raphson iteration giving rise to the well-known problems. It is also shown by Sakallah *et al.* [14] that the division of the gate charge into capacitive charges is not consistent with the Meyer model.

Let us assume that we are using an implicit numerical integration scheme like Gear's variable order methods or the trapezoidal method such that the time derivatives can be approximated by a finite sum of the present and past voltages and their derivatives:

$$\dot{V}(t_{n+1}) = \sum_i \alpha_i V(t_{n+i-1}) + \sum_i \beta_i \dot{V}(t_{n-1}) \tag{4}$$

where t_{n+1} is the current time point where the circuit equations are going to be solved. The coefficients α_i and β_i are determined by the integration intervals. For backward Euler $\alpha_0 = 1/h$ where h is the time interval. If the voltage V varies by an amount δV, the corresponding change in its time derivative $\dot{V}$ can be found easily using the expression above as

$$\delta \dot{V} = \alpha_0 \delta V. \tag{5}$$

Let us apply the techniques above to (2) to obtain the "stamp" of Meyer capacitors, assuming that the three bias voltages V_{gs}, V_{gd}, and V_{gb} change by δV_{gs}, δV_{gd}, and δV_{gb}, respectively. Using the relationship

$$\delta i_{gs} = \delta C_{gs} \dot{V}_{gs} + C_{gs} \delta \dot{V}_{gs} \tag{6}$$

one obtains

$$\begin{aligned} \delta i_{gs} = {} & C_{gs} \alpha_0 \delta V_{gs} + \dot{V}_{gs} \frac{\delta C_{gs}}{\delta V_{gs}} \delta V_{gs} \\ & + \dot{V}_{gs} \frac{\delta C_{gs}}{\delta V_{gd}} \delta V_{gd} + \dot{V}_{gs} \frac{\delta C_{gs}}{\delta V_{gd}} \delta V_{gb}. \end{aligned} \tag{7}$$

Only the first term would appear in this expression if the capacitor were a linear capacitor. The other terms represent the nonlinearities. The second term in the above expression acts like a resistor. The equivalent small signal model is shown in Fig. 1. Similarly, for i_{gd} and i_{gb} one can write

$$\begin{aligned} \delta i_{gd} = {} & C_{gd} \alpha_0 \delta V_{gd} + \dot{V}_{gd} \frac{\delta C_{gd}}{\delta V_{gs}} \delta V_{gs} + \dot{V}_{gd} \frac{\delta C_{gd}}{\delta V_{gd}} \delta V_{gd} \\ & + \dot{V}_{gd} \frac{\delta C_{gd}}{\delta V_{gb}} \delta V_{gb} \end{aligned} \tag{8}$$

$$\begin{aligned} \delta i_{gb} = {} & C_{gb} \alpha_0 \delta V_{gb} + \dot{V}_{gb} \frac{\delta C_{gb}}{\delta V_{gs}} \delta V_{gs} \\ & + \dot{V}_{gb} \frac{\delta C_{gb}}{\delta V_{gd}} \delta V_{gd} + \dot{V}_{gb} \frac{\delta C_{gb}}{\delta V_{gb}} \delta V_{gb}. \end{aligned} \tag{9}$$

SPICE does not properly account for the nonlinearity of the capacitances. It accounts only for the very first term in these expressions. All the other terms, which represent the nonlinearity of the Meyer capacitances, are neglected. The neglect of these first-order terms, along with the trun-

[2]Lsim is a trademark of Silicon Compiler Systems Corporation.

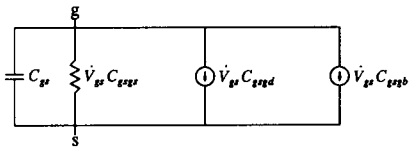


Fig. 1. Small signal model used for modeling C_{gs}. Although we use a resistor symbol in this model, the element does not behave like a resistor in that it has a direction.

cation errors involved in converting to differential-algebraic circuit equations into algebraic equations using (4), and premature convergence are the main reasons for the charge non-conservation observered in transient simulations. Fig. 1 illustrates a small signal model for C_{gs}. The two other Meyer capacitors have the same small signal models as well. The capacitor in this figure is the only component simulated by SPICE. Similarity of this equivalent circuit to the equivalent circuits of charge based nonlinear non-reciprocal models should be noted. However, there is no channel charge partitioning.

We would like to stress that there is absolutely nothing new in the formulation presented above, as the derivation of small signal models from large signal models is a standard well-understood procedure within the framework of Newton–Raphson iterative solution method. However, the technique seems to have been applied only to the large signal currents through the channel in circuit simulators like SPICE, leading to inconsistent and unpredictable results in the case of transient currents. The same procedures which apply to large signal channel currents should be extended to transient currents as well. This is not done in the implementations of the Meyer model in SPICE and its derivatives, which use the Newton–Raphson iteration to solve the nonlinear circuit equations.

The Meyer Model

The method described above can be applied to any model and results in nine new small signal parameters in addition to the three capacitors of the Meyer model. However, only six of the new parameters are independent of each other, as they all share a common integrator Q_g. The new small signal parameters are given by

$$C_{gsgs} = \frac{\delta C_{gs}}{\delta V_{gs}} \quad C_{gsgb} = \frac{\delta C_{gs}}{\delta V_{gb}} \quad C_{gsgd} = \frac{\delta C_{gs}}{\delta V_{gd}}$$

$$C_{gbgs} = \frac{\delta C_{gb}}{\delta V_{gs}} \quad C_{gbgb} = \frac{\delta C_{gb}}{\delta V_{gb}} \quad C_{gbgd} = \frac{\delta C_{gb}}{\delta V_{gd}}$$

$$C_{gdgs} = \frac{\delta C_{gd}}{\delta V_{gs}} \quad C_{gdgb} = \frac{\delta C_{gd}}{\delta V_{gb}} \quad C_{gdgd} = \frac{\delta C_{gd}}{\delta V_{gd}} \tag{10}$$

and the off-diagonal terms satisfy the relationships

$$\begin{aligned} C_{gsgd} &= C_{gdgs} \\ C_{gsgb} &= C_{gbgs} \\ C_{gdgb} &= C_{gbgd} \end{aligned} \tag{11}$$

as can be seen easily from the definition of the capacitances in (2). We shall derive these parameters for the Meyer model.

In the linear region of transistor operation, neglecting the body effects, the total gate charge is given by

$$Q_g(V_{gs}, V_{gd}) = \frac{2}{3} C_0 \frac{V_{gdt}^3 - V_{gst}^3}{V_{gdt}^2 - V_{gst}^2} \tag{12}$$

where $V_{gst} = V_{gs} - V_{th}$, $V_{gdt} = V_{gd} - V_{th}$, V_{th} is the threshold voltage, and $C_0 = WLC_{ox}$ is the gate oxide capacitance. The charge equation for the saturation region, $V_{gdt} = 0$, can be found as

$$Q_g = \tfrac{2}{3} C_0 V_{gst}. \tag{13}$$

Using (2) the Meyer capacitances can be found as

$$C_{gs} = \frac{2}{3} C_0 \left[1 - \frac{V_{gdt}^2}{(V_{gdt} + V_{gst})^2} \right] \tag{14}$$

$$C_{gd} = \frac{2}{3} C_0 \left[1 - \frac{V_{gst}^2}{(V_{gdt} + V_{gst})^2} \right] \tag{15}$$

and

$$C_{gb} = 0. \tag{16}$$

For the saturation region of the transistor, $V_{gdt} = 0$, the Meyer capacitances are given by

$$C_{gs} = \tfrac{2}{3} C_0 \tag{17}$$

$$C_{gd} = 0 \tag{18}$$

$$C_{gb} = 0. \tag{19}$$

The small signal parameters can be easily found as well:

$$\frac{\delta C_{gs}}{\delta V_{gd}} = -2 C_0 \frac{V_{gdt} V_{gst}}{(V_{gdt} + V_{gst})^3} \tag{20}$$

$$\frac{\delta C_{gs}}{\delta V_{gs}} = 2 C_0 \frac{V_{gdt} V_{gdt}}{(V_{gdt} + V_{gst})^3} \tag{21}$$

$$\frac{\delta C_{gd}}{\delta V_{gs}} = -2 C_0 \frac{V_{gdt} V_{gst}}{(V_{gdt} + V_{gst})^3} \tag{22}$$

$$\frac{\delta C_{gd}}{\delta V_{gd}} = 2 C_0 \frac{V_{gst} V_{gst}}{(V_{gdt} + V_{gst})^3}. \tag{23}$$

All the other derivatives are zero. Since the capacitive behavior of the transistor in the saturation region is linear, all of the new small signal parameters in this region are zero.

Examples

A Newton–Raphson implementation of the Meyer model, taking into account all the first-order terms in the linearized transient currents, has been implemented in Lspice. Here we shall give the simulation results on some problem circuits. In our implementation, we neglected the

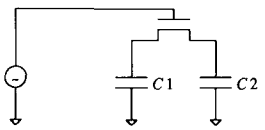


Fig. 2. "Charge pump" circuit used for charge conservation test.

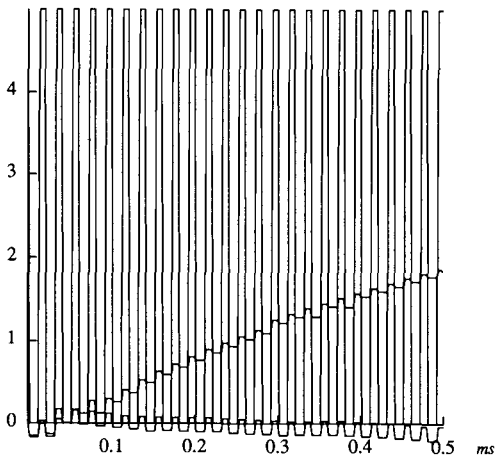


Fig. 3. Output waveform for the "Charge pump" in Fig. 2. Decaying waveform is the SPICE result. The Lspice result eventually stabilizes at a point where V_{gs} is equal to the threshold voltage, at which point there is no more charge left to be pumped to the side capacitors, and the Meyer capacitors vanish.

bulk charges and assumed that the threshold voltage is fixed. The version of SPICE used in these examples is 2G6. Although the documentation accompanying the software claims it has charge conserving models, and although there is code for implementing Ward model, we found that the charge conserving models were never being invoked for any set of model parameters. In any case the original Meyer model was the only MOS capacitance model used by SPICE.

Fig. 2 shows the traditional charge conservation test case. The capacitors are initially uncharged. Charge is injected into them as the gate voltage is pulsed. Fig. 3 shows the results of Lspice and SPICE simulations. While Lspice results indicate that the waveform approaches a steady state, determined by the threshold voltage, SPICE waveforms decay.

Another interesting example is the switched capacitor circuit used in [4] where due to charge non-conservation, charge transfers through the pass transistors in Fig. 4 are not modeled correctly by SPICE. The results of Lspice simulation are shown in Fig. 5. Fig. 6 shows the SPICE waveform. Fig. 8 shows the activity at the intermediate node of this circuit as calculated by SPICE. As pointed out in (4), SPICE gives contradictory results on this circuit. Compared to the Lspice results shown in Fig. 7, SPICE indicates higher amounts of currents going into the intermediate node, but the output node rises much more slowly than with Lspice.

Stability of the new model and the repeatability of the results is excellent compared to SPICE when the simulation interval is extended over long periods of time. As far as the execution speed is concerned, the new model is not

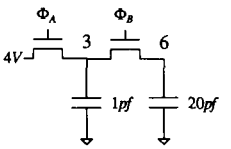


Fig. 4. A switched-capacitor low-pass filter.

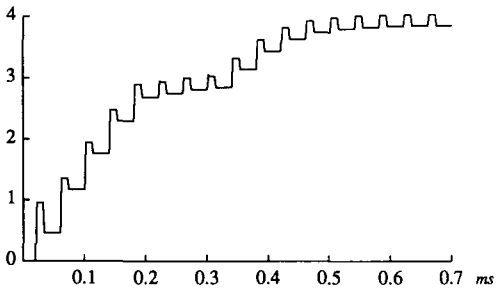


Fig. 5. Lspice output for the switched-capacitor circuit of Fig. 4.

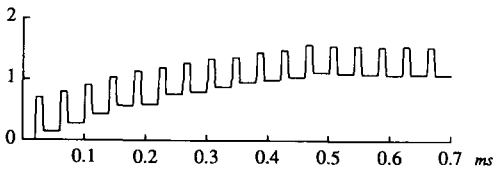


Fig. 6. SPICE output for the switched-capacitor circuit of Fig. 4. Waveform is actually falling off very slowly.

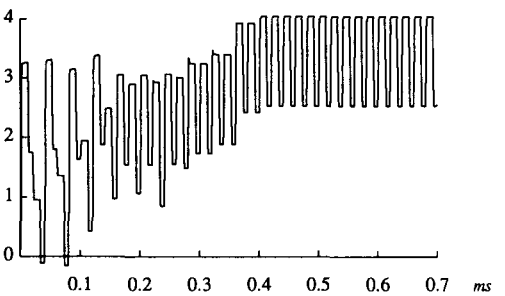


Fig. 7. Lspice waveforms for the intermediate node of the switched-capacitor circuit shown in Fig. 4.

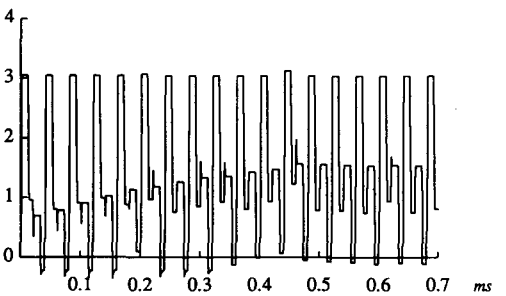


Fig. 8. SPICE waveforms for the intermediate node of the switched-capacitor circuit shown in Fig. 4.

introducing any significant overhead, at least in the case of the first-order model described here.

Conclusions

This paper has presented a new circuit simulation model for the transient analysis of the MOS transistors. It has

been shown that the charge non-conservation problems attributed to Meyer model, or any other current based model, is the result of the neglect of some first-order terms which arise as a result of the linearization of the transient currents through the nonlinear capacitances.

A strictly current oriented formulation of the transient behavior requires nine additional small signal parameters to account for the nonlinearities which can be interpreted as new current sources which supplant the usual capacitive currents. Some of these current sources have been neglected in the implementations of the Meyer model resulting in unexpected circuit behavior in some charge sensitive circuits.

The new Meyer capacitance model was implemented taking into account the hitherto neglected first-order terms. Using the new implementation, none of the test circuits exhibit any symptoms of charge non-conservation.

It should be noted that transient formulation of the nonlinear capacitances described above applies equally well to other semiconductor devices.

Readers should take note of the inherent inaccuracy of the Meyer model which can be significant in some simulations. This inaccuracy is due to implicit neglect of the non-reciprocity and other higher order effects.

ACKNOWLEDGMENT

The author would like to thank A. Cao for drawing his attention to this problem and for providing him with the test circuits.

REFERENCES

[1] J. E. Meyer, "MOS models and circuit simulation," *RCA Rev.*, vol. 32, pp. 42–63, 1971.

[2] L. W. Nagel, "SPICE2: A computer program to simulate semiconductor circuits," ERL-M520, Electronics Res. Lab., Univ. Calif., Berkeley, 1975.

[3] D. E. Ward and R. W. Dutton, "A charge oriented model for MOS transistor capacitances," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 703–707, 1978.

[4] P. Yang, B. D. Epler, and P. K. Chatterjee, "An investigation of the charge conversation problem for MOSFET circuit simulation," *IEEE Solid-State Circuits*, vol. SC-18, pp. 128–138, 1983.

[5] D. E. Ward, "Charge-based modeling of capacitance in MOS transistors," Stanford Electronics Lab. Tech. Rep. G201-11, Stanford Univ., CA, 1981.

[6] B. J. Sheu, D. L. Scharfetter, C. Hu, and D. O. Pederson, "A compact IGFET charge model," *IEEE Trans. Circuits Syst.*, vol. CAS-31(8), pp. 745–748, 1984.

[7] B. J. Sheu, D. L. Scharfetter, and H. C. Poon, "Compact short channel IGFET model (CSIM)," Electronics Res. Lab. Rep. M84/20, Univ. Calif., Berkeley, 1984.

[8] B. J. Sheu, D. L. Scharfetter, P. K. Ko, and M. C. Jeng, "BSIM—Berkeley short Channel IGFET Model for MOS Transistors," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 558–565, 1987.

[9] J. J. Paulos and D. A. Antoniadis, "Limitations of quasi-static capacitance models for the MOS transistor," *IEEE Trans. Electron Devices Lett.*, vol. EDL-4, pp. 221–224, 1983.

[10] J. J. Paulos, D. A. Antoniadis, and Y. P. Tsividis, "Measurement of intrinsic capacitances of MOS transistors," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 238–239, 1982.

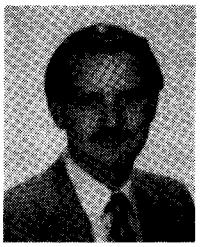
[11] L. A. Glasser and D. W. Dobberpuhl, *Design and Analysis of VLSI Circuits*. Reading, MA: Addison-Wesley, 1985, p. 97.

[12] C. Turchetti, P. Prioretti, G. Masetti, E. Profumo, and M. Vanzi, "A Meyer-like approach for the transient analysis of digital MOS IC's," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 499–507, 1986.

[13] P. Odryna, K. Nazareth, and C. Christensen, "A workstation-based mixed mode circuit simulator," in *Proc. 23th DAC*, 1986.

[14] K. A. Sakallah, Yao-Tsung Yen, and S. G. Greenberg, "The Meyer model revisited: Explaining and correcting the charge non-conservation problem," in *Proc. ICCAD*, pp. 204–207, 1987.

*



Mehmet A. Cirit received the B.Sc. degree in physics from the Middle East Technical University, Ankara, in 1971, and the M.Sc. and Ph.D. degrees in theoretical physics, from the University of Wisconsin, Madison, in 1974 and 1976, respectively.

From 1976 to 1980 he was an assistant professor at Hacettepe University in Ankara teaching physics and mathematics, and involved in high energy nuclear collision research. He also taught physics and electronics at Montclair State College, Montclair, NJ, in 1981. He was a member of technical staff at Skantek Corporation, Warren, NJ, from 1982 to 1985 doing image processing. From 1985 to 1988 he worked for the Silicon Compiler Systems Corporation, Warren, developing timing analyzers and circuit simulators for VLSI CAD. At present he is with Adaptec Inc., Milpitas, CA. His current interests are device modeling, circuit simulation, reliability, and testability.