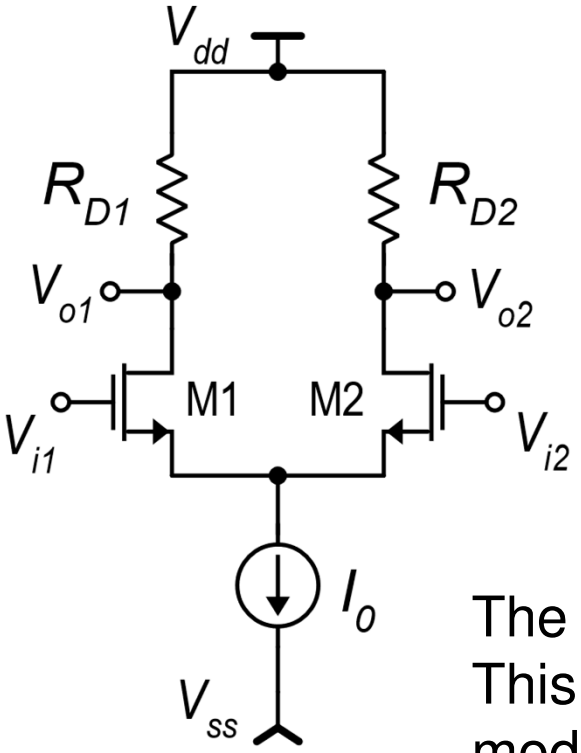
CMOS differential amplifier with resistive load: limitations



1. The S/E version has a poor CMRR (large A_c) and large input offset voltage
2. Both the S/E and fully-diff. versions reach low voltage gains at small supply voltage

Problem 1: Consider the output voltage in the fully-differential case with no resistor mismatch:

$$V_{OD} = R_D\left(I_{D2} - I_{D1}\right) \quad (\text{for } R_{D1} = R_{D2})$$

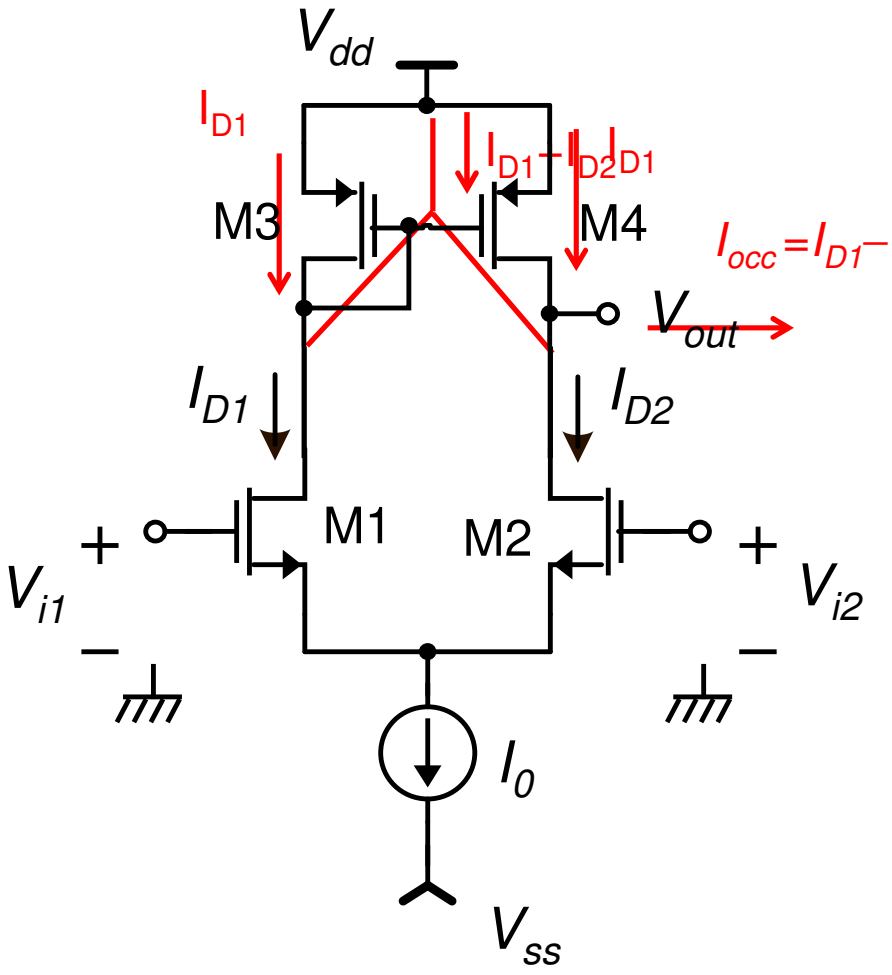
The drain current difference appears:
This reduces A_c (I_{D1} and I_{D2} tend to be equal for only common mode applied) and the output voltage for V_D=0 is affected only by matching errors.

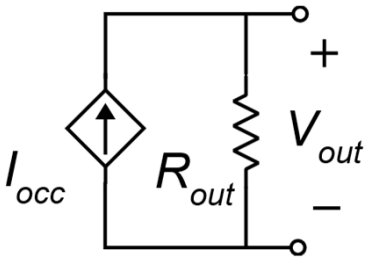
Solution for a S/E amplifier: produce the current difference (I_{D1}-I_{D2}) and then put it into a single resistor. **Problem 2:** Do not use a passive component for the resistor

CMOS differential amplifier with current mirror load

Specifications

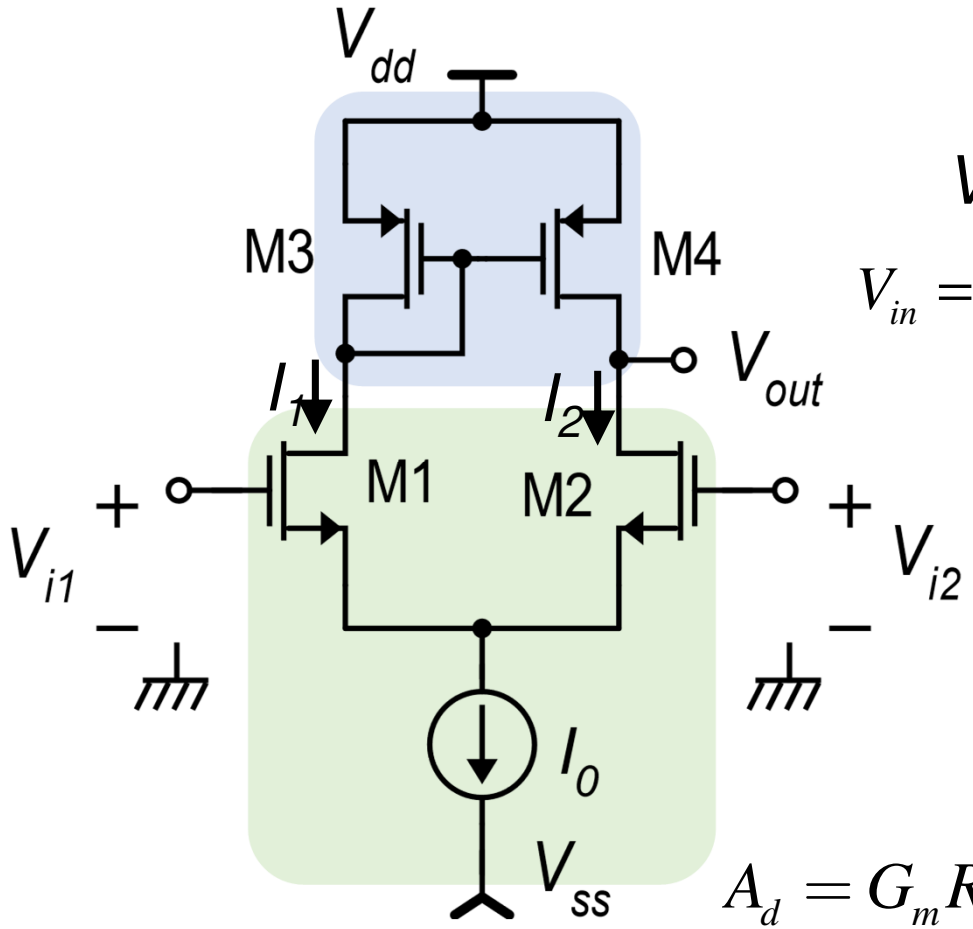
- We need a S/E output port
- High CMRR (> 80 dB)
- High gain (~ 40 dB) even at low supply voltages (V_{dd}–V_{ss}).

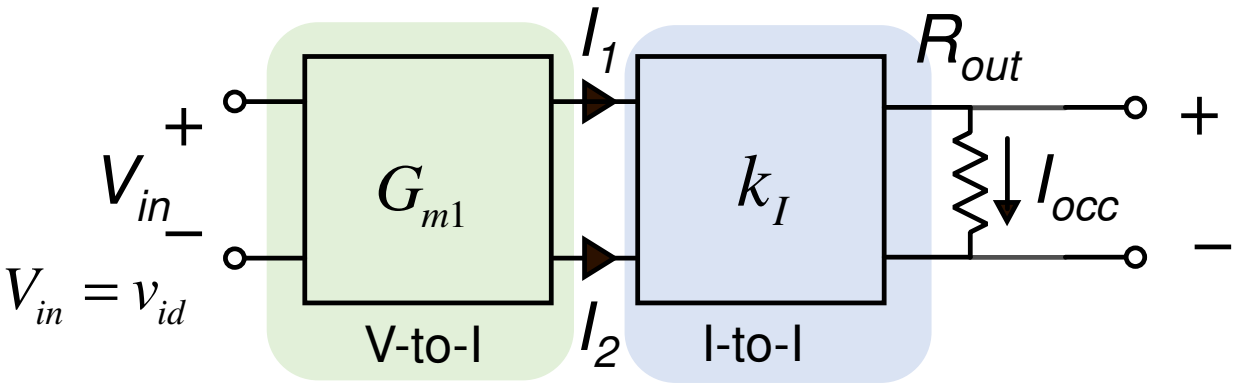




$$I_{occ} = g_{m1} v_{id}$$

Subunits of the amplifier with mirror load





$$(I_1 - I_2) = G_{m1} V_{in} \qquad I_{occ} = k_I (I_1 - I_2)$$

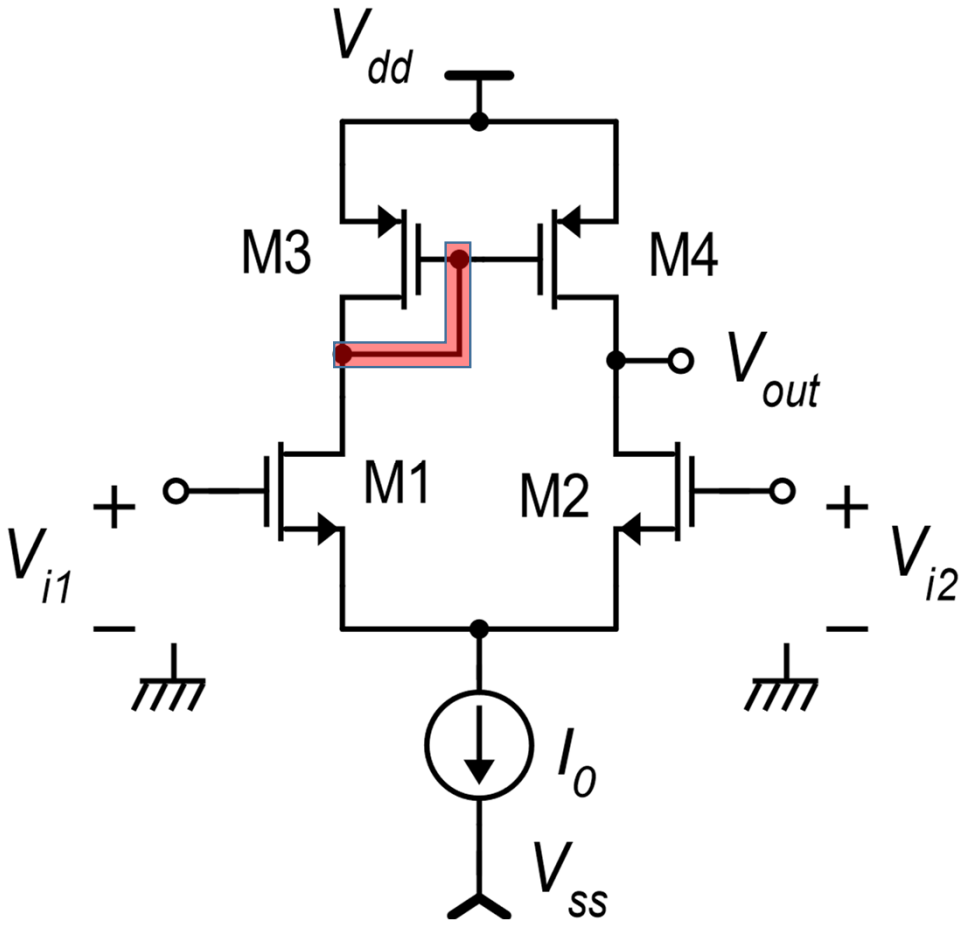
$$G_{m1} = g_{m1} \quad (= g_{m2}) \qquad k_I = 1$$

$$I_{occ} = G_m V_{in}$$

$$G_m = G_{m1} k_I = g_{m1}$$

$$A_d = G_m R_{out} = g_{m1} R_{out}$$

Operating point : V_{id}=0



$$V_{i1} = V_{i2} = V_C$$

Symmetrical stimulus, but ….

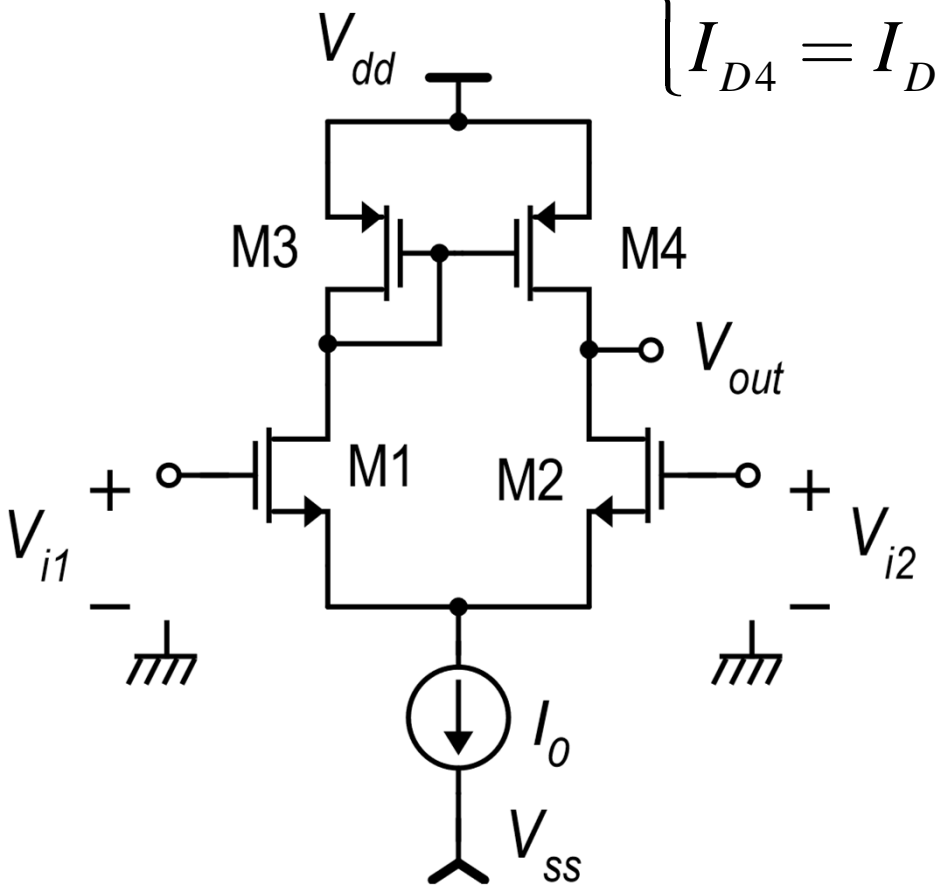
The circuit is not symmetrical

$$I_{D1} = I_{D2} \text{ exactly?}$$

$$I_D = f\left(V_{GS}, V_{BS}, V_{DS}\right)$$

Demonstration of the exact symmetry of the electrical solution for V_{id}=0

$$\begin{cases} I_{D3} = I_{D1} \\ I_{D4} = I_{D2} \end{cases}$$



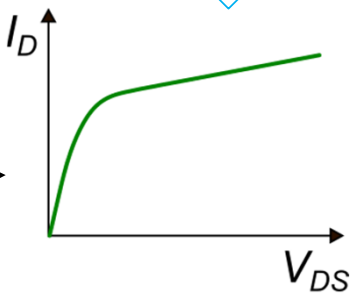
With fixed V_{GS} and V_{BS}, I_D is a monotone function of V_{DS} (or $|V_{DS}|$ for a *p*-MOS.

M1 and M2

$$V_{iD} = 0 \Rightarrow V_{GS1} = V_{GS2}$$

$$V_{S1} = V_{S2} \Rightarrow V_{BS1} = V_{BS2}$$

$$V_{DS1} = V_{DS2} \; ?$$

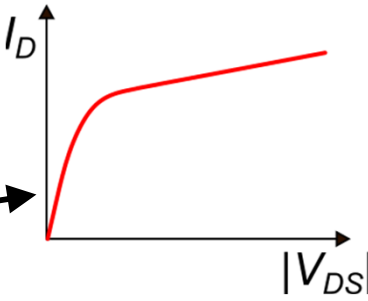


M3 and M4

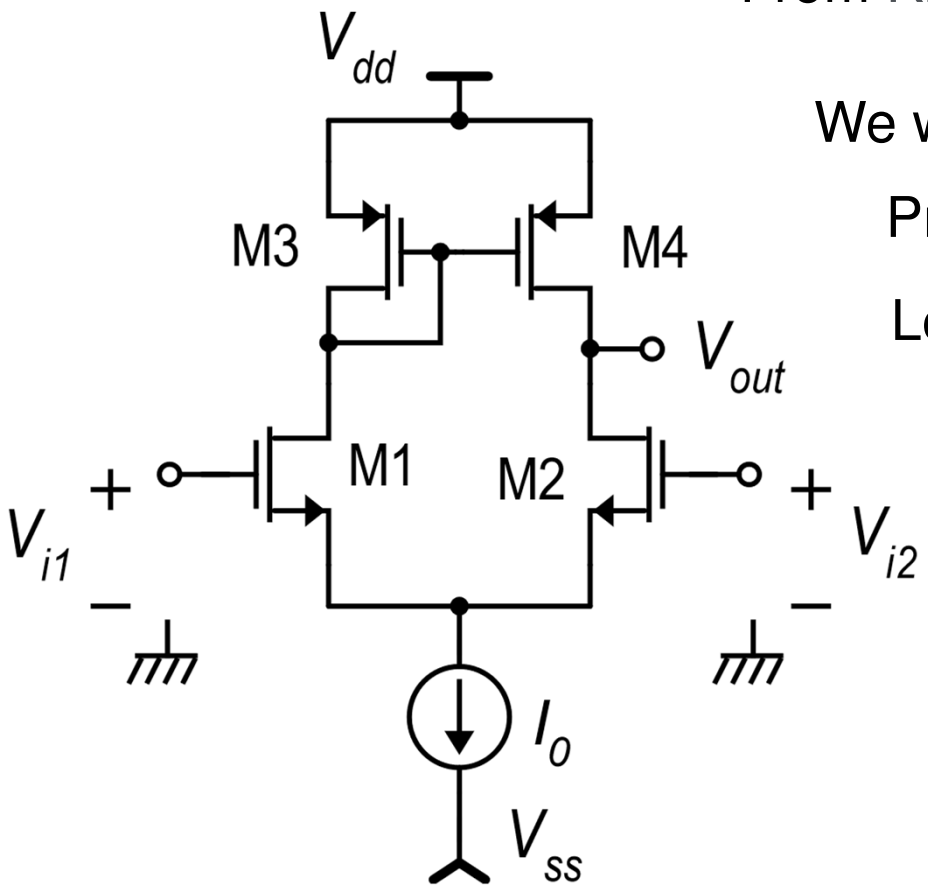
$$V_{GS3} = V_{GS4}$$

$$V_{BS3} = V_{BS4}$$

$$V_{DS3} = V_{DS4} \; ?$$



Demonstration of the exact symmetry of the electrical solution for $V_{id}=0$



From Kirchhoff #2: $V_{DS1} + |V_{DS3}| = V_{DS2} + |V_{DS4}|$

We want to demonstrate that: $I_{D1} = I_{D2}$

Proof by contradiction:

Let us suppose: $I_{D1} > I_{D2}$

$$\begin{cases} I_{D3} = I_{D1} \\ I_{D4} = I_{D2} \end{cases}$$

$V_{DS1} > V_{DS2}$

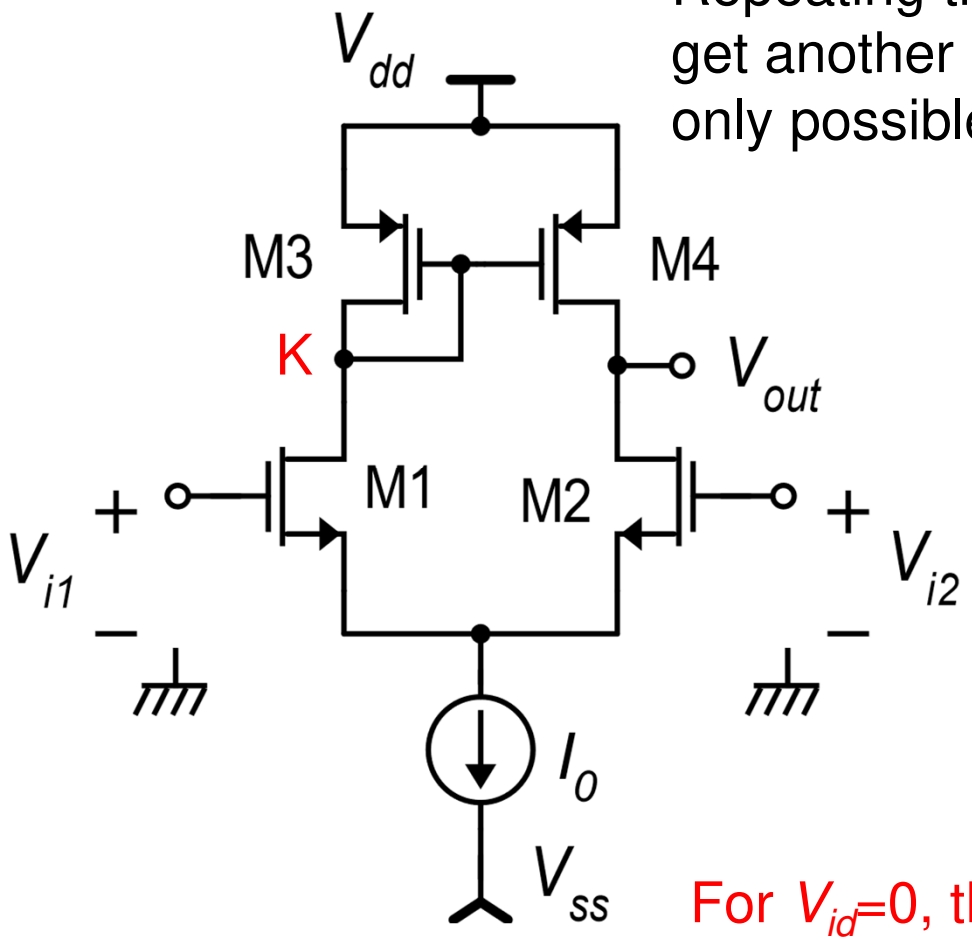
$I_{D3} > I_{D4}$

$|V_{DS3}| > |V_{DS4}|$

$V_{DS1} + |V_{DS3}| > V_{DS2} + |V_{DS4}|$

Contradiction

Demonstration of the exact symmetry of the electrical solution for $V_{id}=0$



Repeating the procedure for $I_{D1}<I_{D2}$ we get another contradiction; thus, the only possible solution is:

$$\begin{cases} I_{D1} = I_{D2} \\ I_{D3} = I_{D4} \end{cases}$$

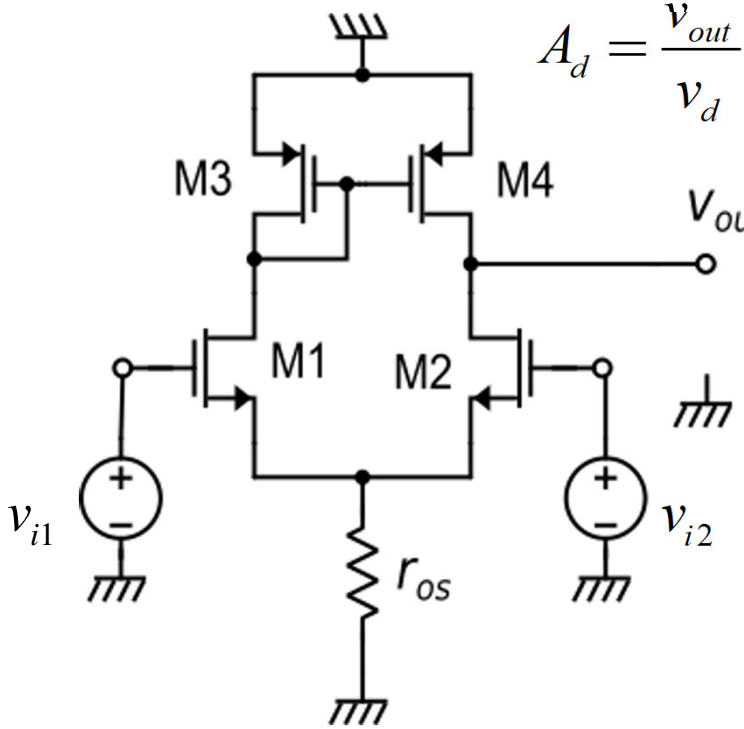
$$\begin{cases} V_{DS1} = V_{DS2} \\ |V_{DS3}| = |V_{DS4}| \end{cases}$$

$$\begin{cases} V_K = V_{dd} - |V_{DS3}| \\ V_{out} = V_{dd} - |V_{DS4}| \end{cases}$$

$$V_{out} = V_K$$

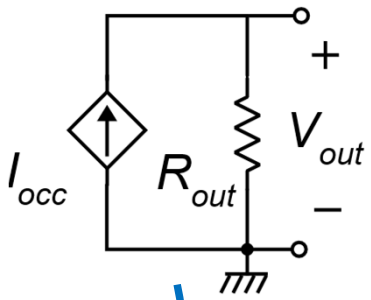
For $V_{id}=0$, the electrical solution is perfectly symmetrical

Differential mode gain



Small-signal equivalent circuit

$$A_d = \left.\frac{v_{out}}{v_d}\right|_{v_c=0}$$



Norton equivalent circuit of the output port

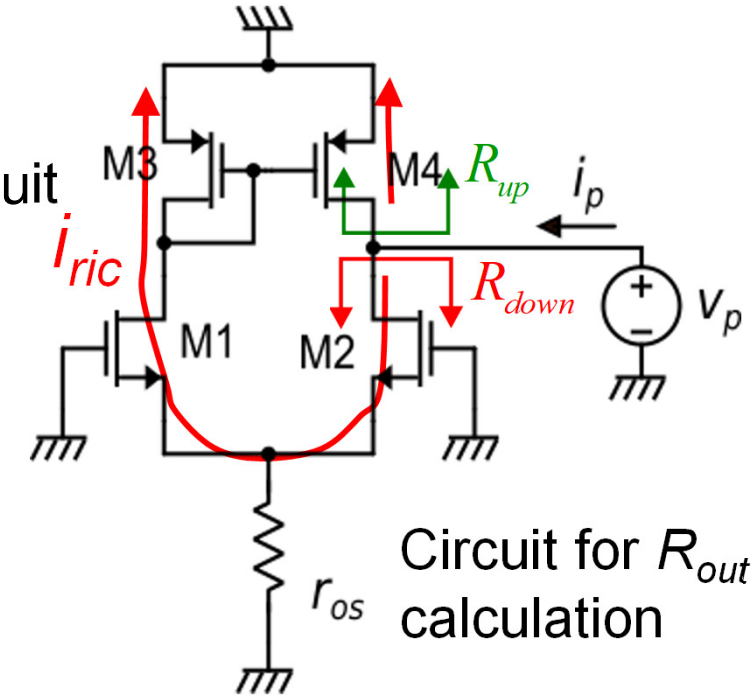
$$v_{out} = i_{occ} R_{out}$$

$$i_{occ} = i_{d4} - i_{d2} \cong i_{d1} - i_{d2} = g_m v_d$$

$$v_{out} = g_m v_d R_{out} \Rightarrow A_d = g_m R_{out}$$

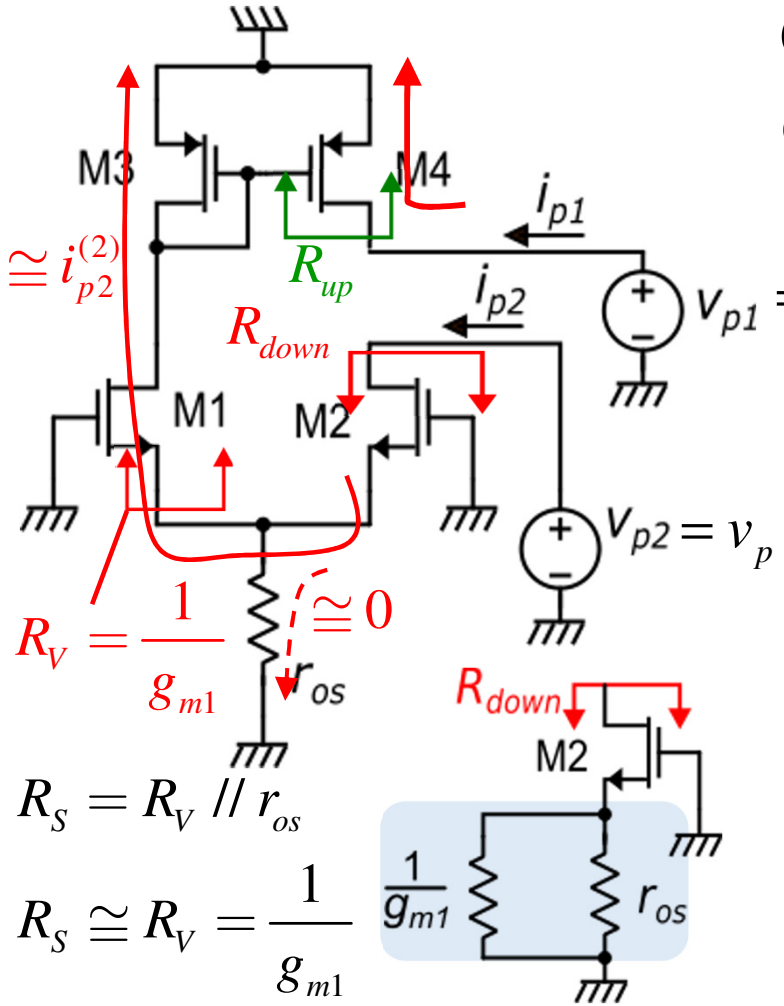
$$R_{out} = R_{up} \,//\, R_{down}$$

$$i_p = \frac{v_p}{R_{up}} + \frac{v_p}{R_{down}} + i_{ric}$$



Circuit for R_{out} calculation

Differential mode gain: R_{out} calculation.



$$R_S = R_V \,//\, r_{os}$$

$$R_S \cong R_V = \frac{1}{g_{m1}}$$

Case 1: $v_{p1} = v_p,\ v_{p2} = 0 \rightarrow i_{p1} = i_{p1}^{(1)},\ i_{p2} = i_{p2}^{(1)}$

Case 2: $v_{p1} = 0,\ v_{p2} = v_p \rightarrow i_{p1} = i_{p1}^{(2)},\ i_{p2} = i_{p2}^{(2)}$

For the superposition theorem: $i_p = i_{p1}^{(1)} + i_{p2}^{(1)} + i_{p1}^{(2)} + i_{p2}^{(2)}$

Case 1: $i_{p1}^{(1)} = \frac{v_p}{R_{up}},\ i_{p2}^{(1)} = 0 \quad R_{up} = r_{d4}$

Case 2:

$$i_{p2}^{(2)} = \frac{v_p}{R_{down}} \qquad i_{p1}^{(2)} \cong i_{p2}^{(2)}$$

$$\frac{g_{m2}}{g_{m1}} = 1$$

$$R_{down} = R_S + r_{d2}\left(1 + g_{m2}R_S\right) = 2r_{d2}$$

$$i_p = \frac{v_p}{r_{d4}} + 0 + \frac{v_p}{2r_{d2}} + \frac{v_p}{2r_{d2}} = v_p\left(\frac{1}{r_{d4}} + \frac{1}{r_{d2}}\right)$$

$$R_{out} = \frac{v_p}{i_p} = \left(\frac{1}{r_{d2}} + \frac{1}{r_{d4}}\right)^{-1} = r_{d2} \,//\, r_{d4}$$

Differential mode gain

$$R_{out} = r_{d2} // r_{d4} \qquad A_d = g_{m1}\left(r_{d2} // r_{d4}\right)$$

The gain is of the order of $\frac{g_m r_d}{2}$
Independently from the supply voltage

$$A_d = g_{m1}\left(\frac{1}{\frac{1}{r_{d2}} + \frac{1}{r_{d4}}}\right) \qquad r_d = \frac{1}{\lambda I_D} \qquad A_d = g_{m1}\left(\frac{1}{\lambda_2 I_{D2} + \lambda_4 I_{D4}}\right)$$

$$A_d = \frac{g_{m1}}{I_{D1}}\left(\frac{1}{\lambda_2 + \lambda_4}\right) \leftarrow I_{D2} = I_{D4} = I_{D1}$$

Differential mode gain

$$A_d = \frac{g_{m1}}{I_{D1}}\left(\frac{1}{\lambda_2 + \lambda_4}\right)$$

$$\frac{g_m}{I_D} \triangleq \frac{1}{V_{TE}}$$

$$V_{TE} = \begin{cases} \dfrac{V_{GS} - V_t}{2} \\ mV_T \end{cases}$$

In strong inversion.
Minimum V_{TE}=50 mV

In weak inversion.
V_{TE} ≅35-40 mV

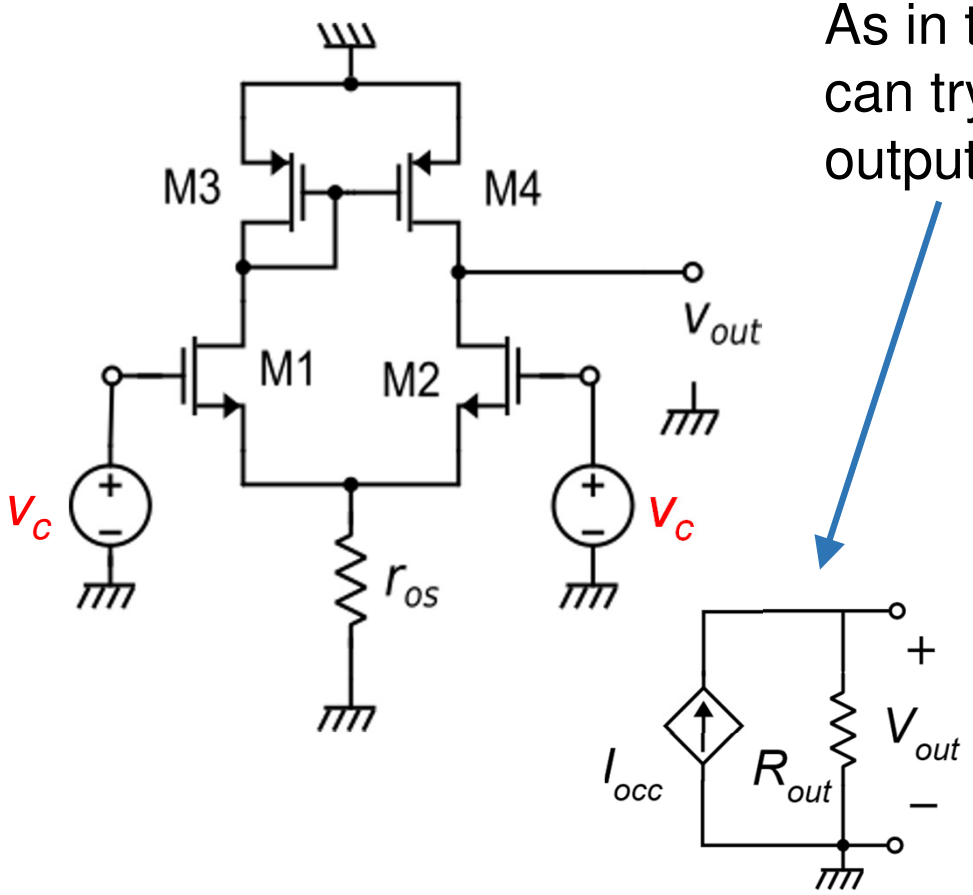
$$A_d = \frac{1}{V_{TE1}}\left(\frac{1}{\lambda_2 + \lambda_4}\right)$$

In order to obtain a large differential-mode gain it is necessary to:

- Set V_{TE} to a small value
- Use long MOSFETs (small λ)

Common mode gain

As in the case of differential input voltage, we can try to use the Norton equivalent circuit of the output port.



$$v_{out} = i_{occ} R_{out} \qquad R_{out} = r_{d2} \,//\, r_{d4}$$

$$i_{occ} = i_{d1} - i_{d2}$$

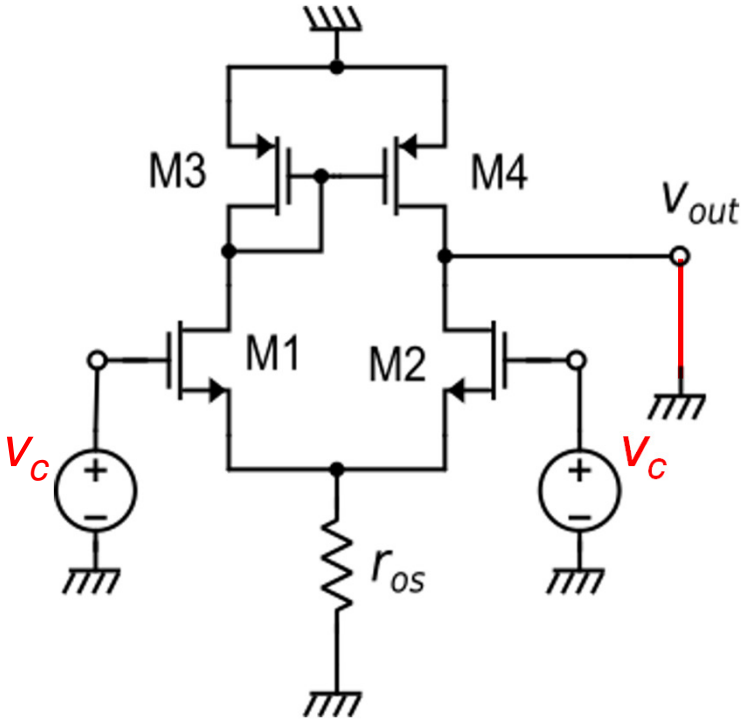
$$\text{for } v_d = 0 \quad i_{d1} = i_{d2} = \frac{v_c}{2r_{os}}$$

$$i_{occ} = 0$$

$$v_{out} = 0 \Rightarrow A_c = 0 \Rightarrow CMRR = \infty$$

Is it possible??

Common mode gain



The problem occurs when we calculate i_{occ}. Placing a short circuit across the output port, disrupts the symmetry:

$$v_{ds4} = 0 \quad v_{ds3} = -\frac{1}{g_{m3}} i_{d1} \neq 0$$

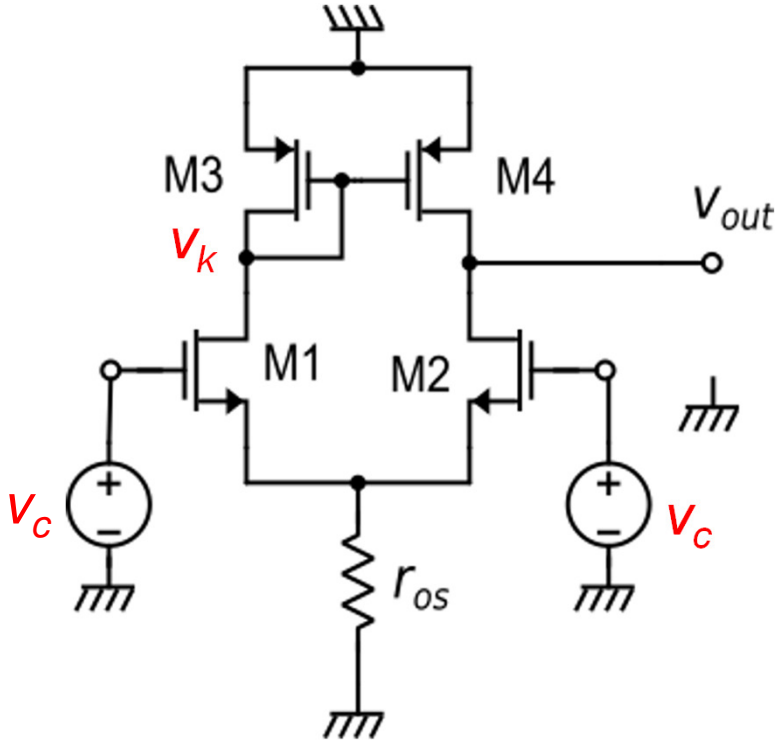
$$v_{ds1} = -\frac{1}{g_{m3}} i_{d1} - v_{s1} \quad v_{ds2} = -v_{s1} \neq v_{ds1}$$

$$i_{d1} \neq i_{d2}$$

$$i_{d3} \neq i_{d4}$$

$$i_{occ} = i_{d4} - i_{d2} \neq 0$$

Common mode gain



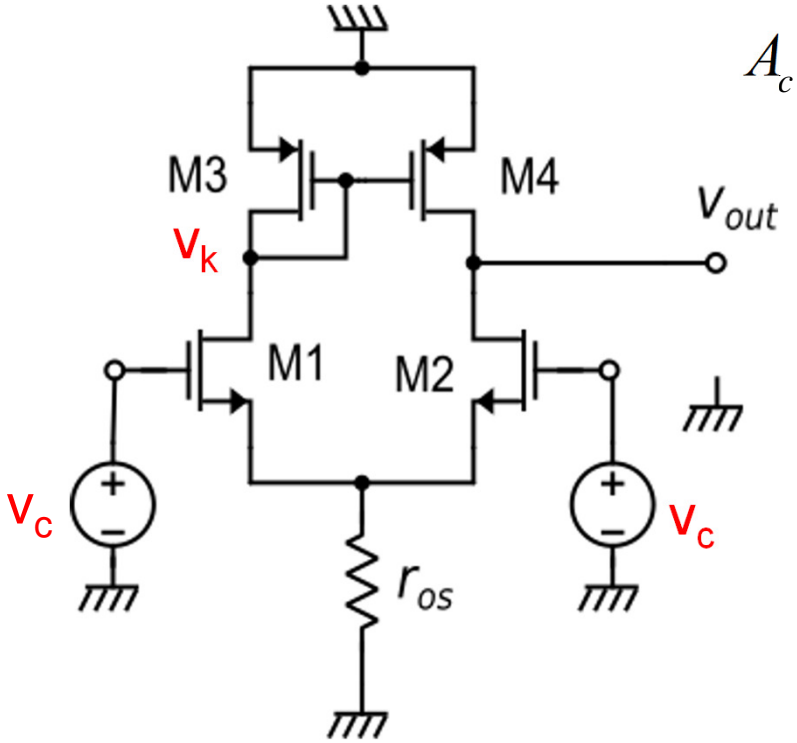
It is possible to exactly calculate i_{occ}, taking into account the actual i_{d1}/i_{d2} ratio and i_{d4}/i_{d3} ratio ….

… but this is a very tedious approach
There is a much simpler way:

Let us remove the short circuit and directly calculate v_{out}. Now , for v_{id}=0, the circuit is symmetric again and, in particular: v_k=v_{out}

$$v_{out} = v_k = -\frac{1}{g_{m3}} i_{d1} \cong -\frac{v_c}{2 r_{os} g_{m3}}$$

Common mode gain



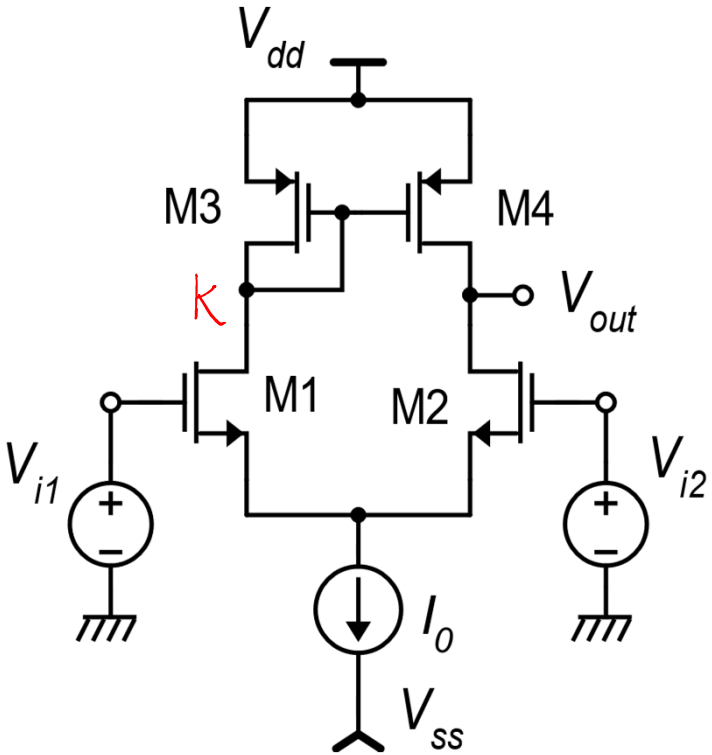
$$A_c = \left.\frac{v_{out}}{v_c}\right|_{v_d=0} = -\frac{1}{2g_{m3}r_{os}} \qquad A_d = \left.\frac{v_{out}}{v_d}\right|_{v_c=0} = g_{m1}\left(r_{d2} \,//\, r_{d4}\right)$$

$$CMRR = \left|\frac{A_d}{A_c}\right| = 2g_{m3}r_{os}g_{m1}\left(r_{d2} \,//\, r_{d4}\right) \approx \left(g_m r_d\right)^2$$

for $r_{os}=r_d$
(worst case: the tail is the output branch of a simple current mirror) and considering all g_m's and r_d's equal for simplicity

A CMRR of 80 dB can be easily reached

Large-signal dc transfer function



$$V_{i1} = V_C + \frac{V_D}{2} \qquad V_{i2} = V_C - \frac{V_D}{2} \qquad V_C = constant$$

$$V_{out}(V_D)$$

For V_D=0:

$$V_{out}(0) = V_k(0) = V_{DD} - |V_{GS3}|$$

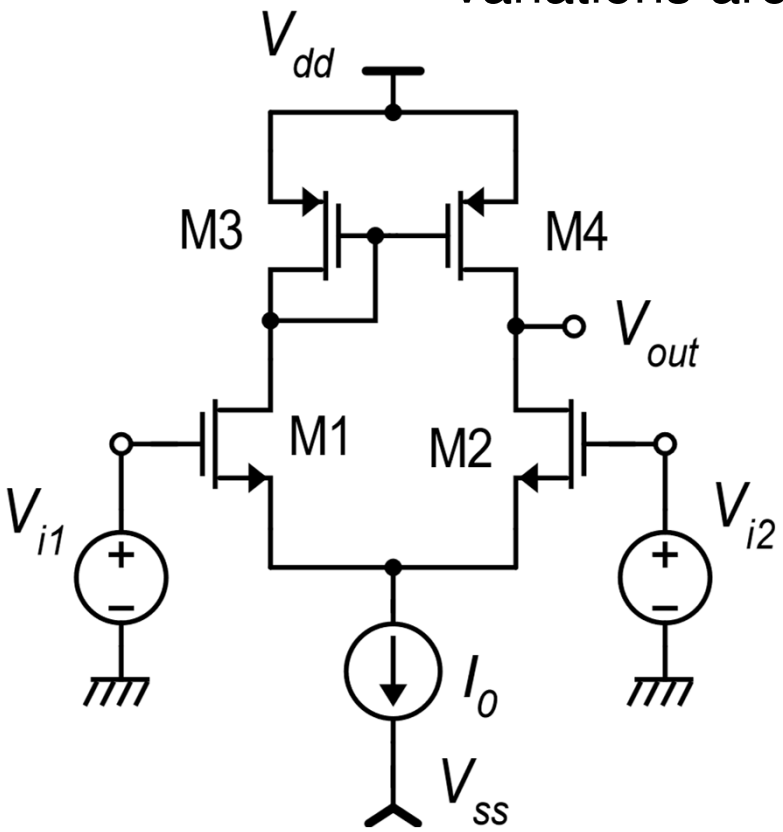
$$|V_{GS3}| = |V_{tp}| + |V_{GS} - V_{tp}|_3$$

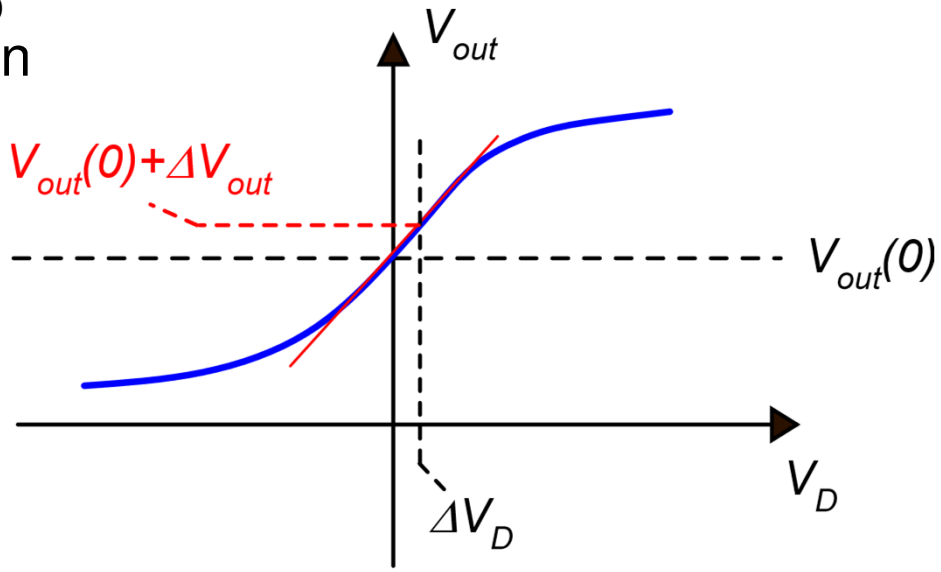
In strong inversion

$$\sqrt{\frac{2I_{D3}}{\beta_3}}$$

Large-signal dc transfer function

V_{out} variations for small V_D variations around the origin





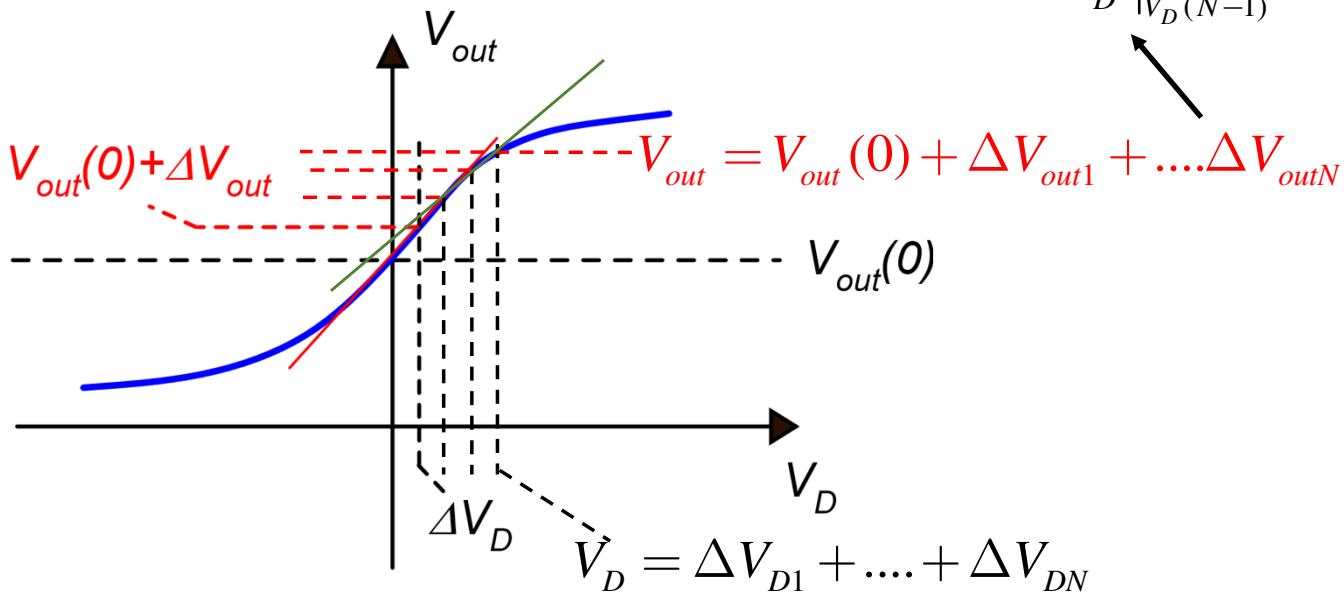
$$\Delta V_{out} = R_{out}\Delta I_{OCC}$$

g_{m1}

$$\Delta I_{OCC} = \Delta V_D \left(\frac{dI_{occ}}{dV_D} \right)_{V_D=0}$$

Moving away from the origin, step by step

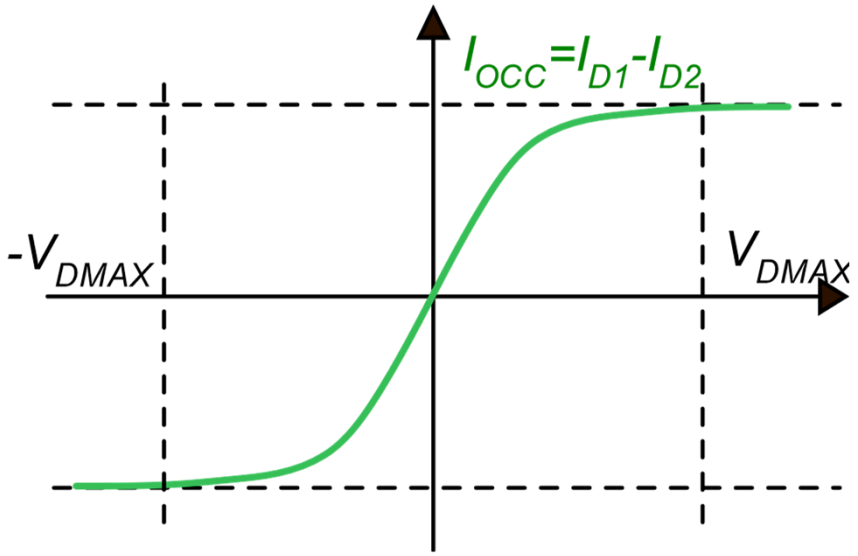
$$\Delta V_{outN} = V_{out}(N-1) + \Delta V_{DN} \left.\frac{\partial V_{out}}{\partial V_D}\right|_{V_D(N-1)}$$

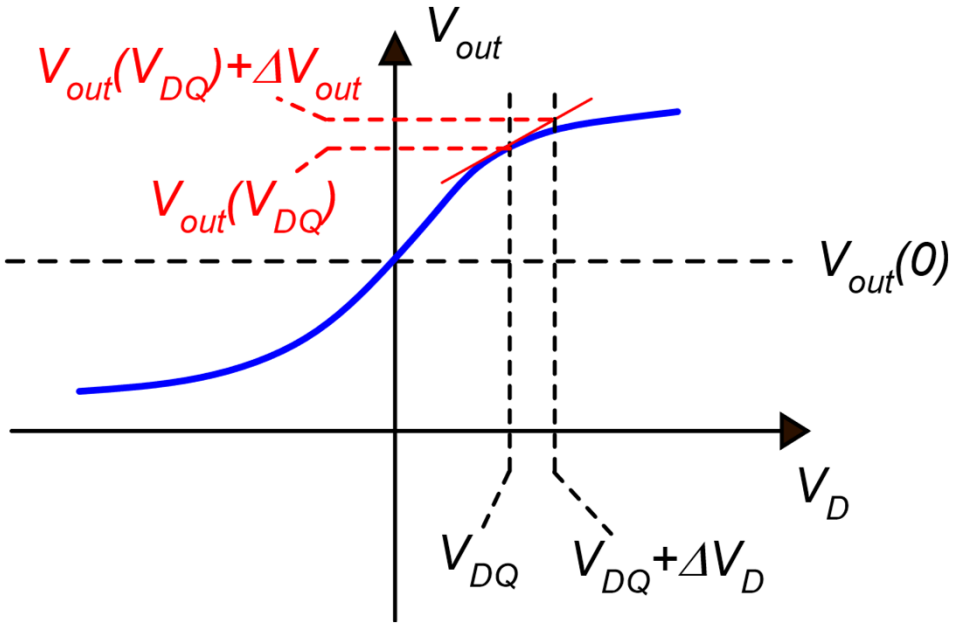


Large-signal dc transfer function

$$\Delta V_{out} = R_{out}\left(V_{DQ}\right)\Delta I_{OCC}$$

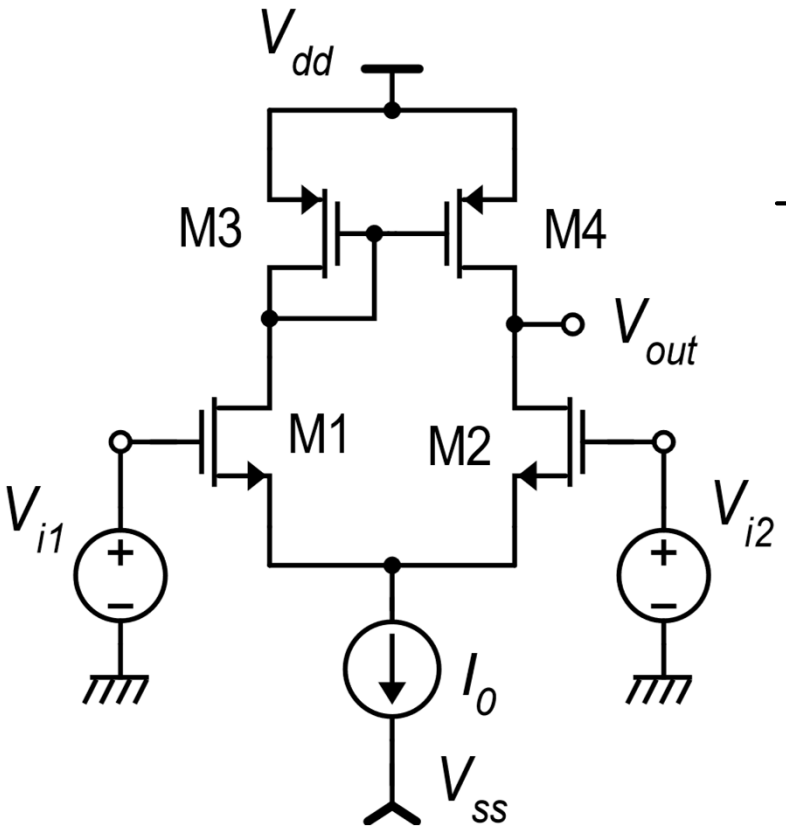
$$\Delta I_{OCC} = \Delta V_D \left(\frac{dI_{occ}}{dV_D}\right)_{V_D = V_{DQ}}$$

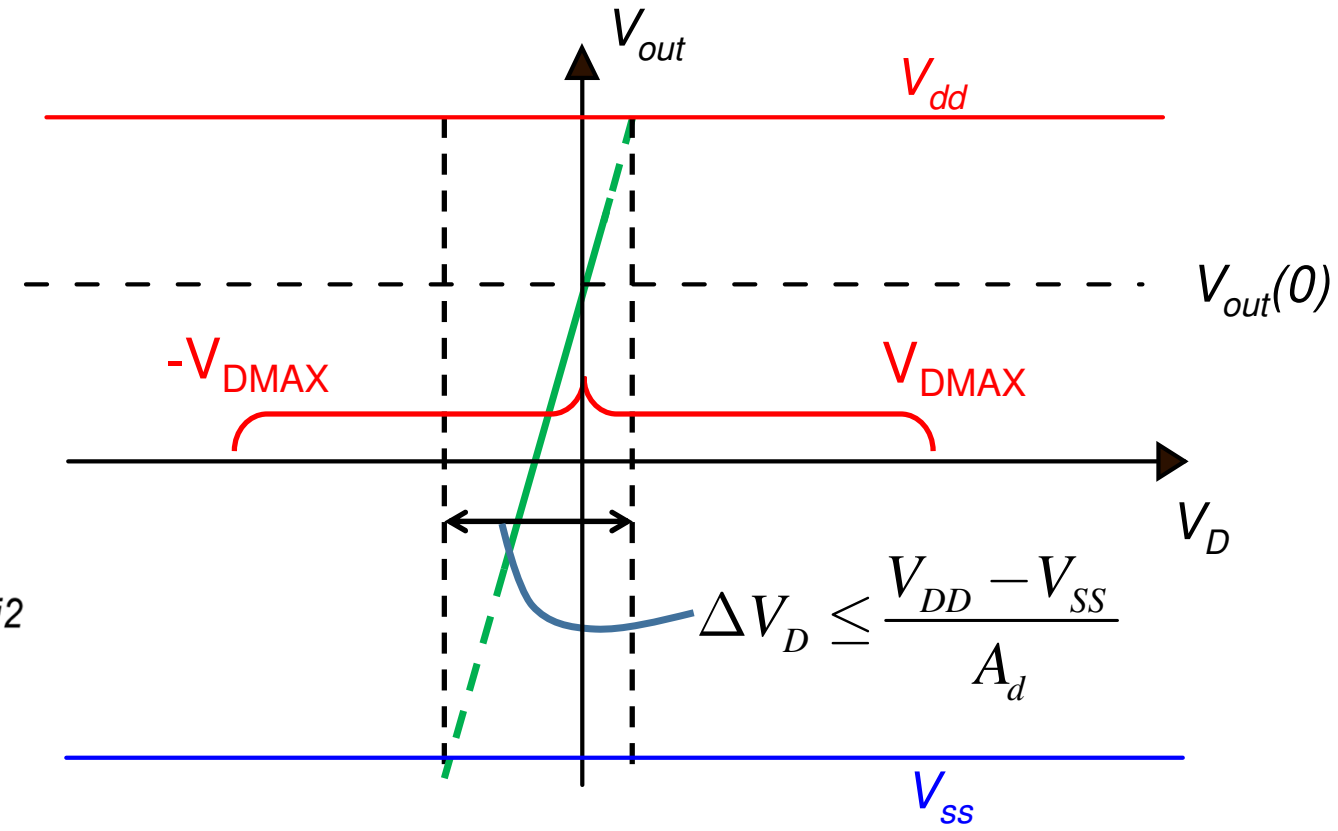




$$\Delta V_{out} = \Delta V_D R_{out}\left(V_{DQ}\right)\left(\frac{dI_{occ}}{dV_D}\right)_{V_D = V_{DQ}}$$

Approximate dc transfer characteristic

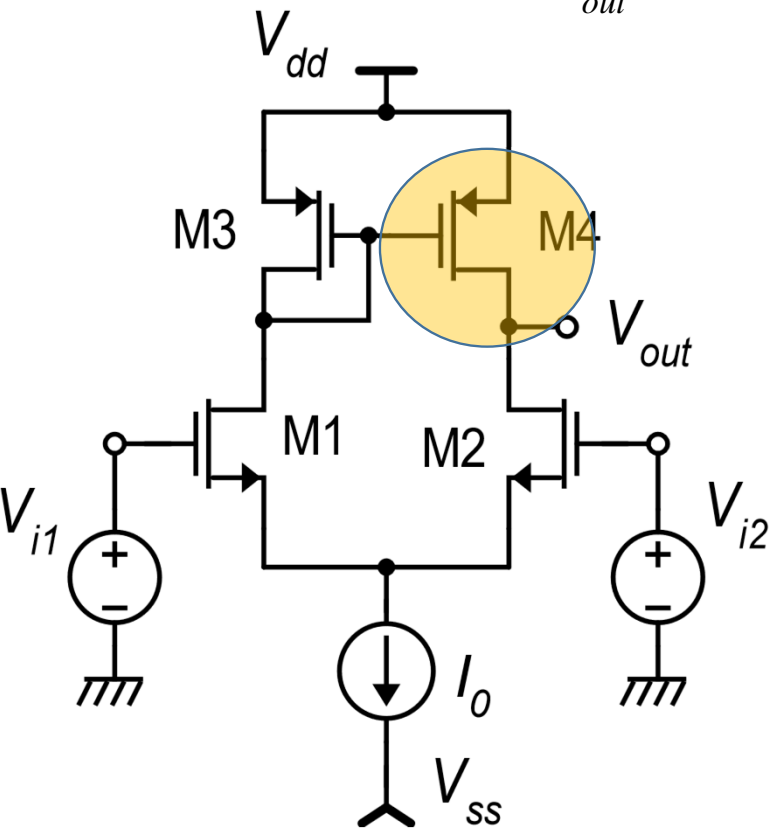




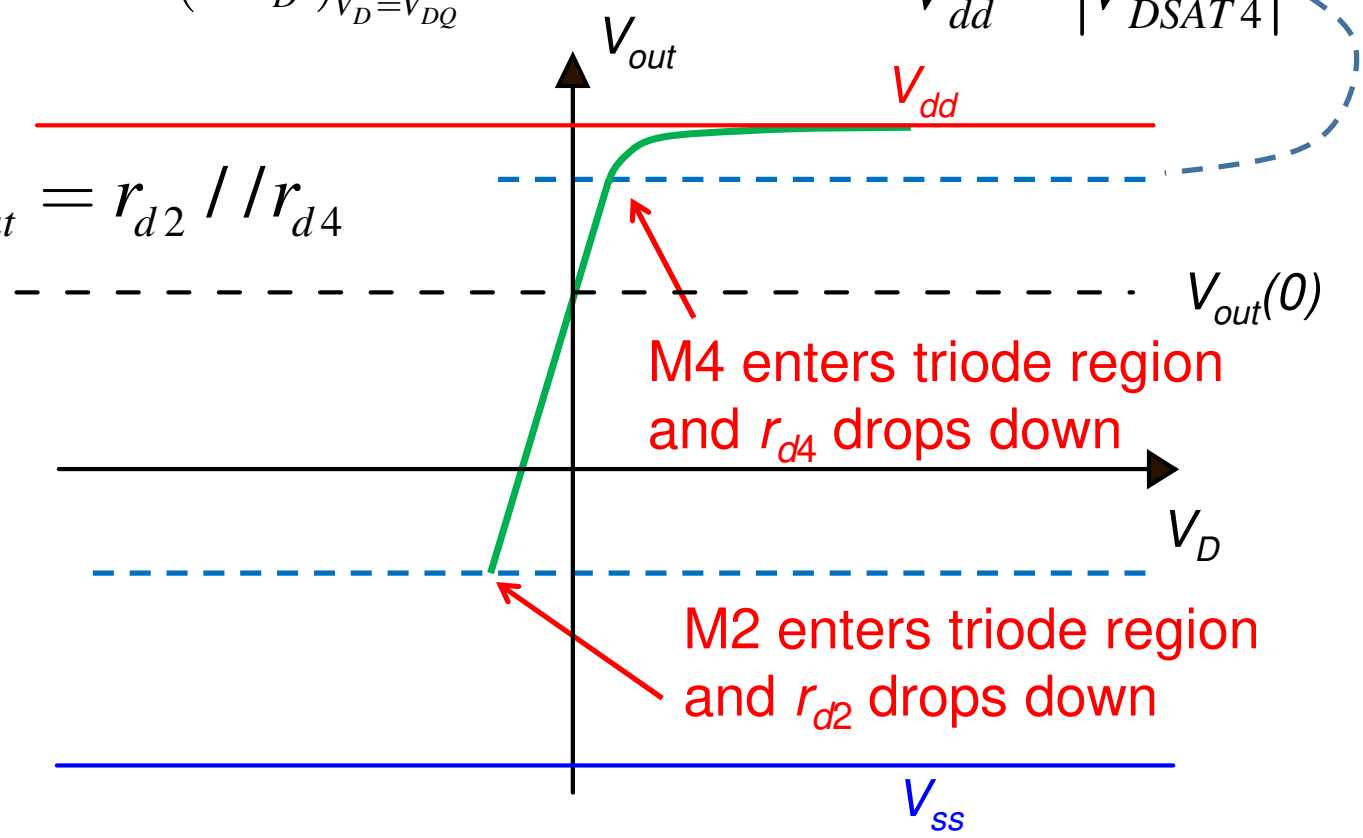
Example: A_d=100, V_{dd}-V_{ss}=5V ΔV_D<50 mV

$$\Delta V_{out} = \Delta V_D R_{out}\left(V_{DQ}\right)\left.\frac{dI_{occ}}{dV_D}\right|_{V_D=V_{DQ}}$$

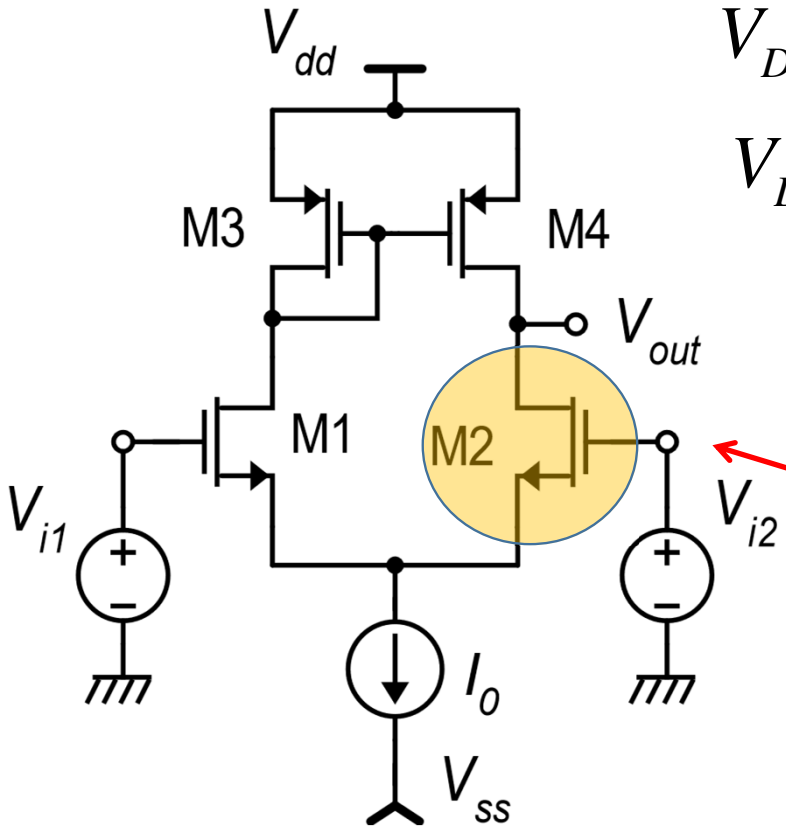
Practically constant and equal to g_{m1}



$R_{out} = r_{d2} \,//\, r_{d4}$



Minimum output voltage



$$V_{DS2} \geq V_{DSAT2}$$

$$V_{DS2} = V_{out} - V_{S2} = V_{out} - \left(V_{i2} - V_{GS2}\right) \geq V_{DSAT2}$$

$$V_{out} \geq V_{i2} - V_{GS2} + V_{DSAT2}$$

$$V_C - \frac{V_D}{2}$$

V_D in the linear zone is at most a few tens mV

V_C varies between V_{SS} and V_{DD}

$$V_{out} \geq V_C - V_{GS2} + V_{DSAT2}$$

Minimum output voltage

$$\min\left(V_{out}\right) = V_C - V_{GS2} + V_{DSAT2}$$

Strong inversion

$$V_{DSAT2} = V_{GS2} - V_{tn}$$

$$\min\left(V_{out}\right) = V_C - V_{tn}$$

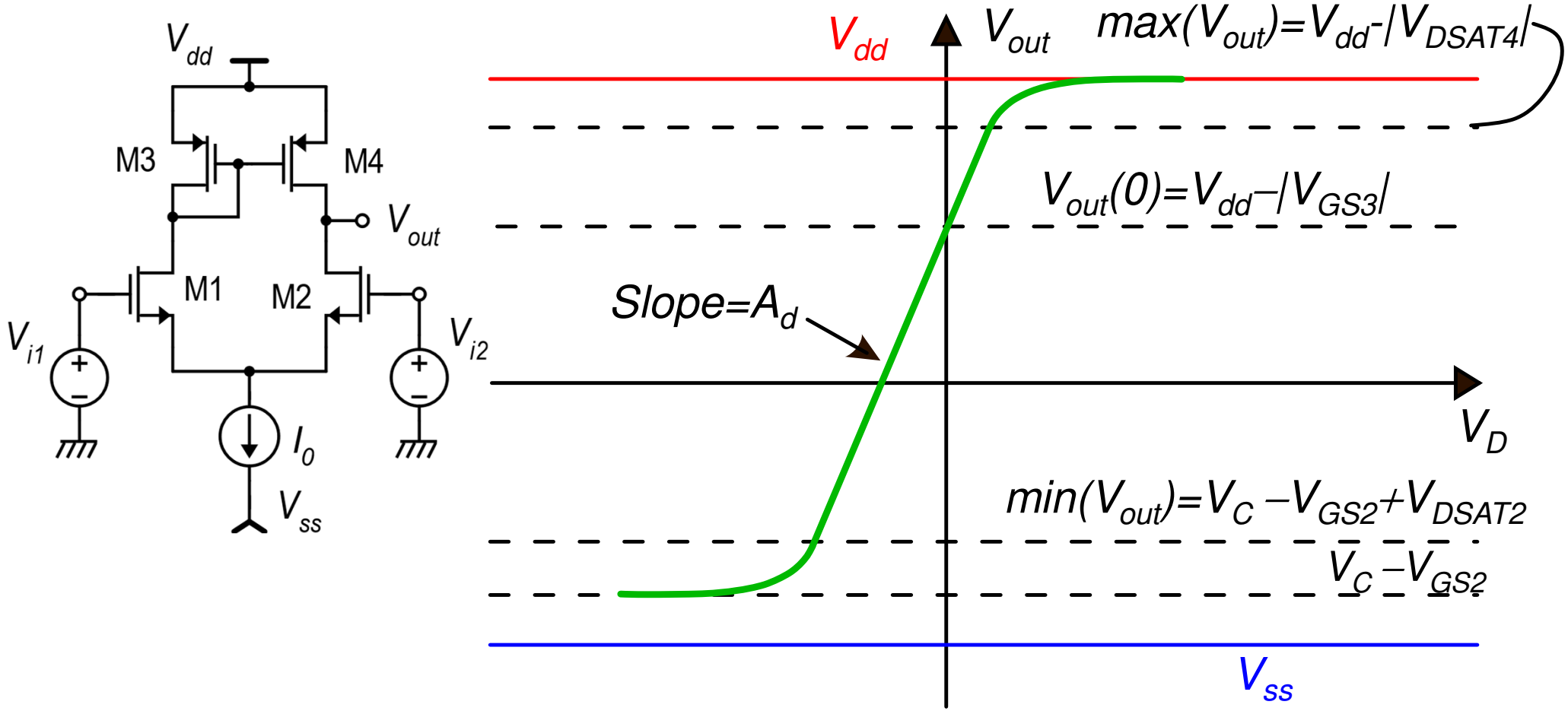
Weak inversion

$$V_{DSAT2} \cong 100 \text{ mV}$$

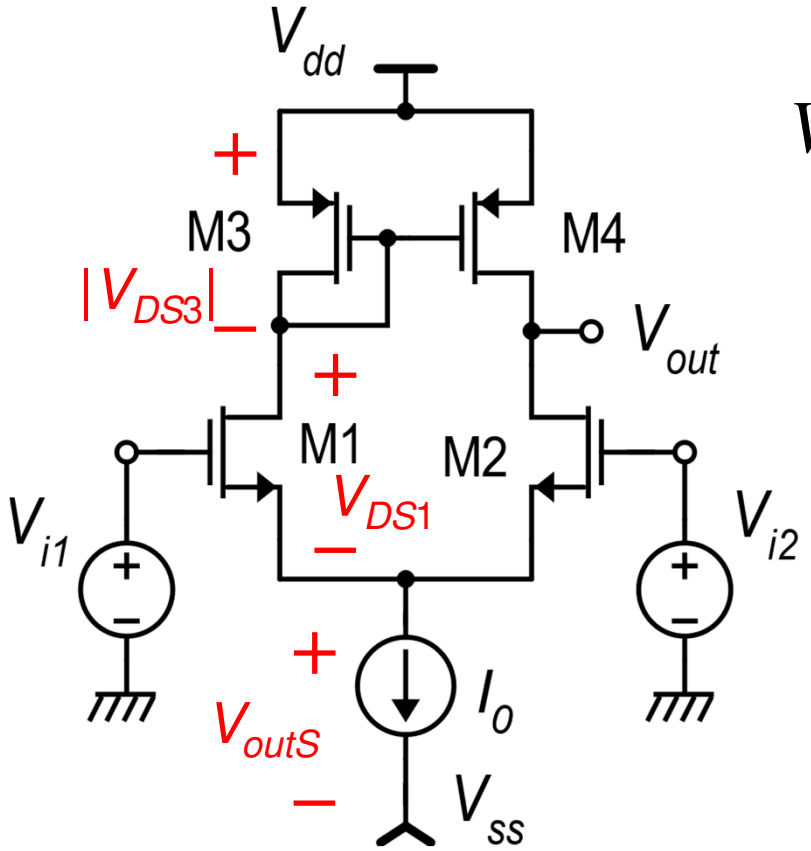
$$V_{GS2} \cong V_{tn}$$

$$\min\left(V_{out}\right) = V_C - V_{tn} + 100 \text{ mV}$$

Complete dc transfer characteristic



Minimum supply voltage V_{dd}-V_{ss}



$$V_{dd} - V_{ss} = V_{outS} + V_{DS1} + |V_{DS3}|$$

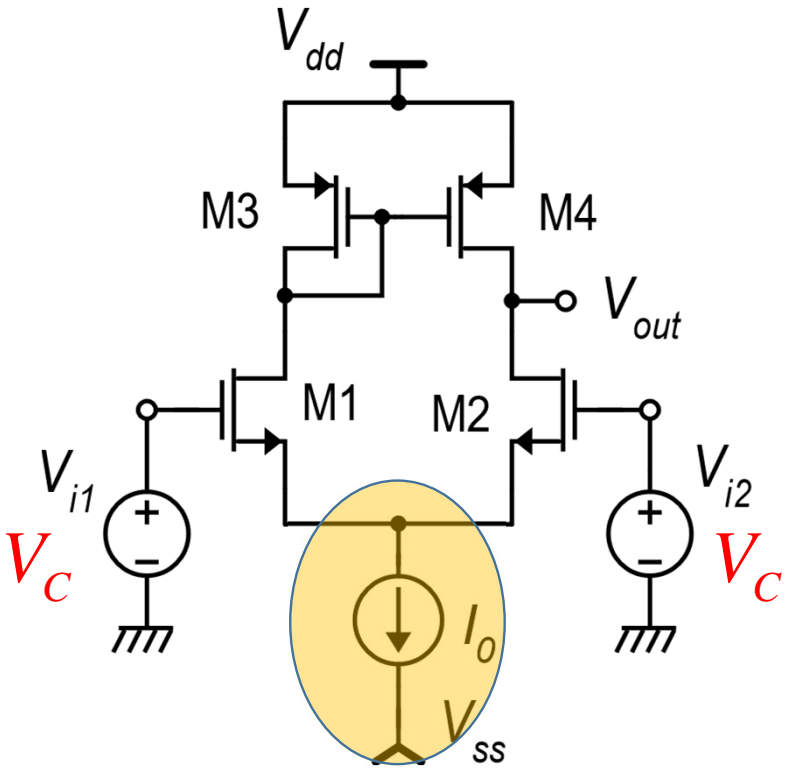
$$V_{DS3} = V_{GS3} \qquad \min(V_{outS}) = V_{MIN}$$

$$\min(V_{dd} - V_{ss}) = V_{MIN} + V_{DSAT1} + |V_{GS3}|$$

Example: V_{MIN}=100 mV
V_{DSAT2}=100 mV
$|V_{GS3}|$=0.5 V

$$\min(V_{dd} - V_{ss}) \cong 0.7 \text{ V}$$

Input common mode range



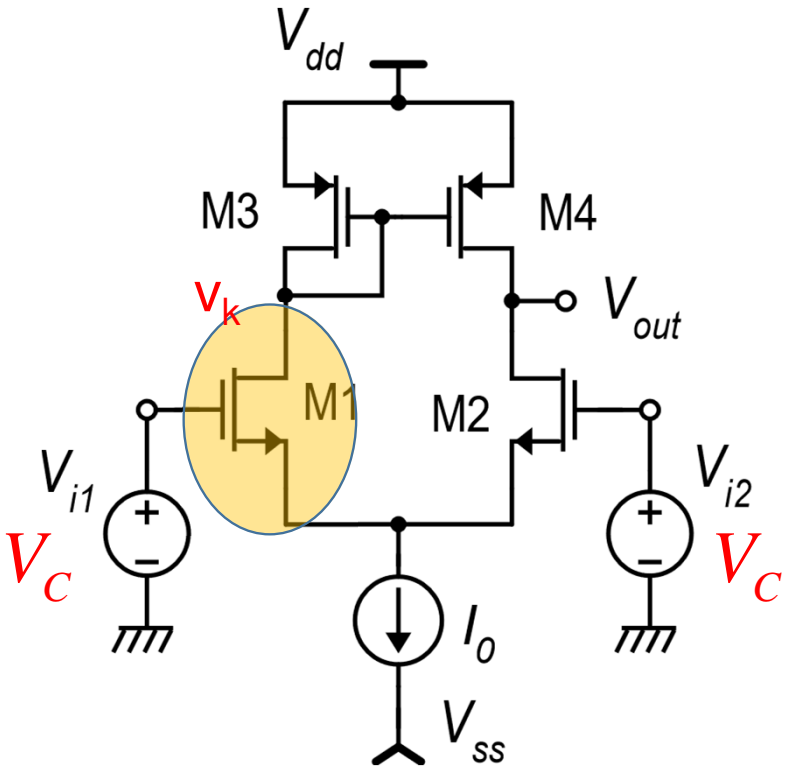
Lower limit

As V_C is progressively decreased, also V_S decreases at the same pace and eventually the voltage across the current source I_0 will get smaller than the minimum value V_{MIN}. From that point on, I_0 will rapidly decrease, turning off the stage.

$$\min\left(V_C\right) = V_{SS} + V_{MIN} + V_{GS1}$$

Input common mode range

Upper limit



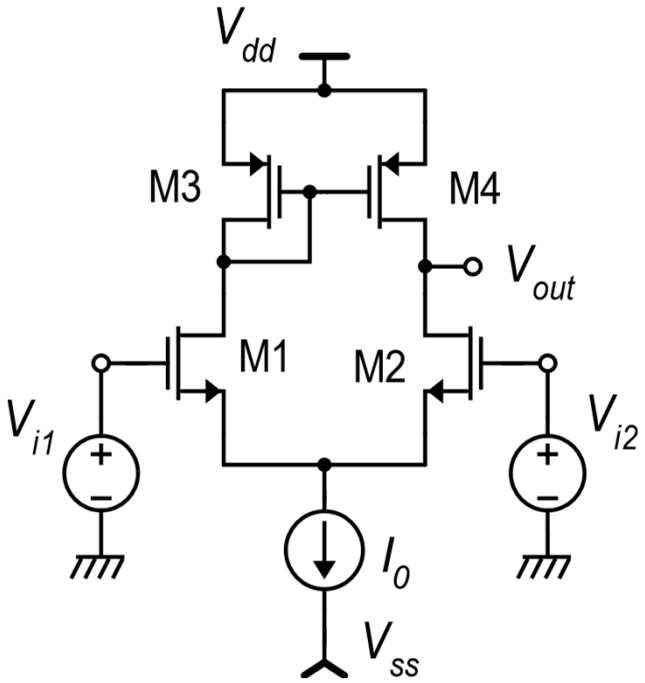
As V_C is progressively increased, also V_S increases at the same pace. Since $V_{out}=V_K=V_{D2}=V_{D1}$ is fixed, eventually V_{DS1} and V_{DS2} will drop below the saturation voltage.

$$V_{DS1}=V_K-V_{S1}\geq V_{DSAT1}$$

$$V_{dd}-\left|V_{GS3}\right|-\left(V_C-V_{GS1}\right)\geq V_{DSAT1}$$

$$V_{dd}-\left|V_{GS3}\right|+V_{GS1}-V_{DSAT1}\geq V_C$$

Input common mode range



$$V_{dd} - \left|V_{GS3}\right| + V_{GS1} - V_{DSAT1} \geq V_C$$

$$\left|V_{GS3}\right| = \left|V_{tp3}\right| + \left|V_{GS3} - V_{tp3}\right|$$

$$V_{GS1} = V_{tn1} + \left(V_{GS1} - V_{tn1}\right)$$

These overdrive voltages can be made close to zero by design

$$\max\left(V_C\right) =$$

$$= V_{dd} - \left|V_{tp3}\right| + V_{tn1} - \left|V_{GS3} - V_{tp3}\right| + \left(V_{GS1} - V_{tn1}\right) - V_{DSAT1}$$

This difference can be >0 because: $V_{tn1} > \left|V_{tp3}\right|$ (V_{t1} is affected by body effect)

The input common mode voltage can get even slightly higher than V_{dd}