1 Considerations on the cascode architecture

Premise: the common-gate amplifier

The common gate (CG) stage is shown in Fig. 1.1 (a), where i_S and r_{s_out} form the input signal source (Norton equivalent circuit) and r_{bias} model the equivalent small signal resistance of the circuit used to bias the CG stage. For a large number of applications, it is convenient to model the CG stage as a current amplifier with ideally unity gain. For this reason, the output signal is represented in Fig. 1.1 (a) by the current i_{out}. In Fig. 1.1 (b), the output resistance of the input source, $r_{s\text{-}out}$ is combined with the bias resistance forming the parallel resistance $r_s=r_{s\text{-}out} \,//\, r_{bias}$. The output terminal of the CG stage (drain) is connected to the ideal voltage source V_{out} in Fig. 1.1 (a) and (b). For the small signal analysis, this corresponds to closing the output termination to ground (output short circuit). In these conditions, i_{out} is the output short-circuit current of the CG stage.

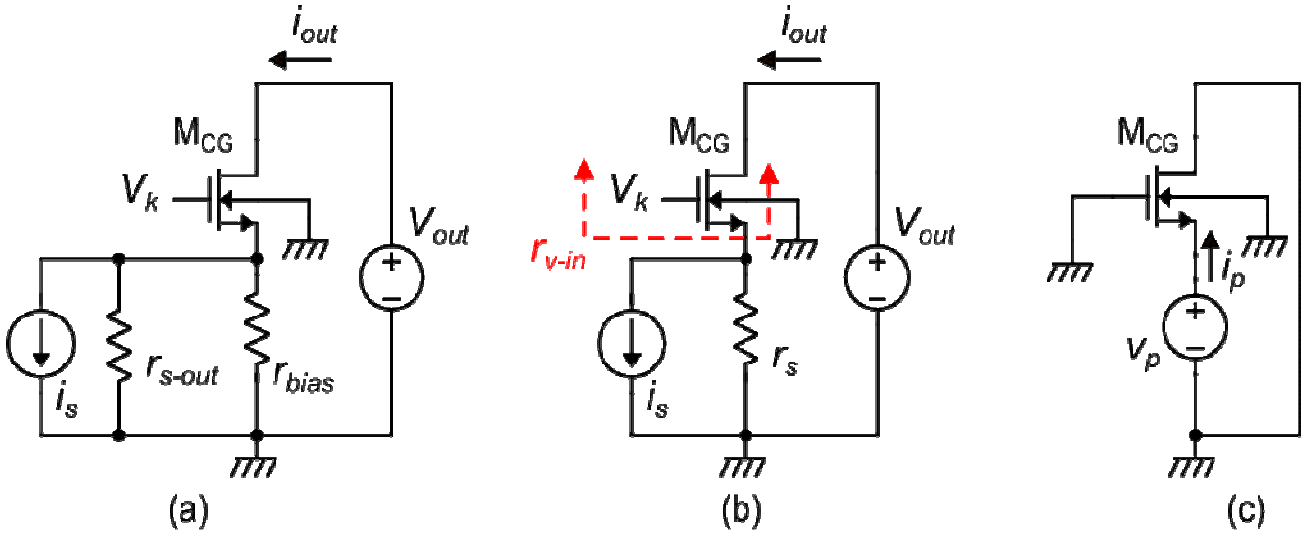

Fig. 1.1. (a) Cascode stage used as a current amplifier of unity gain; (b) fusion of the source resistance with the bias resistance (c) small signal circuit for r_{v_in} calculation.

In order to determine the actual current gain, it is convenient to first calculate the input resistance of the stage, indicated with $r_{v\text{-}in}$ in Fig. 1.1 (b). Referring to the circuit in Fig. 1.1 (c), the input resistance is equal to:

$$r_{v-in} = \frac{v_p}{i_p} = \frac{v_p}{-i_d} = \frac{v_s}{-i_d} \tag{1.1}$$

The drain current (small signal variation) is given by:

$$i_d = \left(g_m v_{gs} + g_{mb} v_{bs} + g_d v_{ds}\right) = -v_s \left(g_m + g_{mb} + g_d\right) \tag{1.2}$$

where $g_d=1/r_d$. and g_{mb} is the body transconductance of the MOSFET, given by:

$$g_{mB} = (m-1)\cdot g_m \tag{1.3}$$

and m is a coefficient generally varying in the range 1.2-1.3 (see chapter on MOSFET models).

Substituting (1.2) into (1.1) we obtain:

$$r_{v-in} = \frac{1}{(g_m + g_{mb} + g_d)} \cong \frac{1}{(g_m + g_{mb})} = \frac{1}{mg_m} < \frac{1}{g_m} \tag{1.4}$$

Expression (1.4) demonstrate that the input resistance is relatively low. It is possible to easily find the amplifier gain considering that the fraction of is that is transferred to i_{out} is the one that flows into $r_{v\text{-}in}$, while the current in r_S is lost. From the current divider formed by r_S and $r_{v\text{-}in}$ we find:

$$\frac{i_{out}}{i_s} = \frac{r_S}{r_S + r_{v-in}} \cong \frac{r_S}{r_S + 1/mg_m} = \frac{mg_m r_S}{1 + mg_m r_S} \tag{1.5}$$

The ideal condition is clearly represented by $mg_m r_S >> 1$, resulting in a current gain close to 1.

The cascode stage

A cascode stage is the cascade of a common-source (CS) and a CG stage. A simple cascode architecture involving two n-MOSFETs is shown in Fig. 1.2. M1 is the CS stage, while M_2 is the CG one. The output terminal of the cascode stage (M_2 drain), is connected to the voltage source V_{out}. Then, when we calculate the v_{in} to i_{out} transfer function, the output terminal is short-circuited.

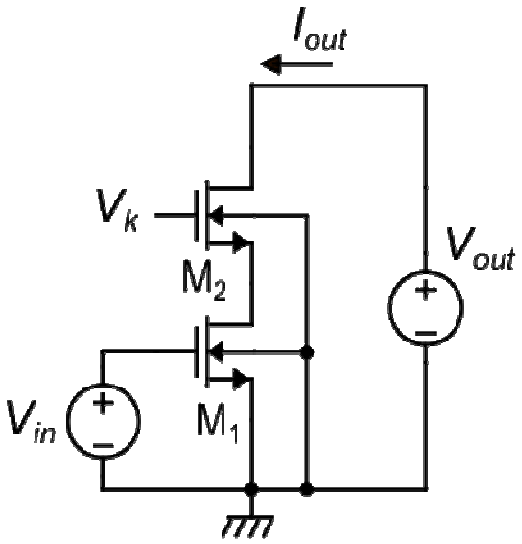

Fig. 1.2. Cascode topology with main voltages indicated.

The constant bias voltage V_K sets the V_{DS} of M1, according to the following relationship:

$$V_{DS1} = V_K - V_{GS2} \tag{1.6}$$

When both M_1 and M_2 work in saturation region, V_{GS2} has a weak dependence on $I_{D2}=I_{D1}$, so that V_{DS1} can be considered to be nearly constant. To obtain a correct quiescent point, V_k and V_{out} must be such that both M_1 and M_2 are in saturation region. The value of V_{DS1} in this condition will be indicated as V_{DS1Q}. Voltage V_{in} includes both a constant bias component, $V_{in}(0)$, and a small signal component, v_{in}.

Small signal analysis of the cascode stage: v_{in} to i_{out} transfer function.

In this analysis, V_{out} is constant, then, in the equivalent small-signal circuit, the output terminal is connected to ground. Considering the CG model of Fig.1.1 (a), in the cascode stage of Fig. 1.2 the CS stage feeds the CG stage with a current $i_S=g_{m1}v_{in}$, while $r_S=r_{d1}$. Then, indicating with $A_{I\text{-}CG}$ the current gain of the CG stage and applying (1.5), we find the following transfer function:

$$\frac{i_{out}}{v_{in}} = \frac{A_{I-CG}\, g_{m1} v_{in}}{v_{in}} = g_{m1} \frac{m_2 g_{m2} r_{d1}}{1 + m_2 g_{m2} r_{d1}} \tag{1.7}$$

If $gm_2rd_1>>1$, the output current is very close to $g_{m1}v_{in}$, i.e., in terms of output short-circuit current, the CG stage can be considered transparent. The advantage of cascading a CG stage to a CS stage is twofold:

1. A much larger output resistance than a single CS stage
2. A reduced Miller effect with respect to CS stages used as voltage amplifiers.

In this document, we will limit to analyze the mechanism by which the output resistance is boosted.

Small signal analysis of the cascode stage: effects of v_{out} variations and consequences on the output resistance.

Let us consider the effects of small signal variations applied to V_{out}, when V_k and V_{in} are constant, i.e. their small signal components are zero. First, we can write:

Using the small signal equations of M_1 and M_2, with $v_{in}=0$, we find:

$$i_{d1} = v_{ds1} g_{d1} \tag{1.8}$$

$$i_{d2} = g_{m2} v_{gs2} + g_{mB2} v_{bs2} + g_{d2} v_{ds2} \tag{1.9}$$

Using the following obvious relationships:

$$\begin{cases} i_{d2} = i_{d1} = i_{out} \\ v_{gs2} = v_{bs2} = -v_{s2} = -v_{ds1} \\ v_{ds2} = v_{out} - v_{s2} \end{cases} \tag{1.10}$$

we can put (1.8) and (1.9) together, obtaining:

$$v_{out} g_{d2} = v_{s2} \left(g_{m2} + g_{mB2} + g_{d2} + g_{d1} \right) \tag{1.11}$$

Solving (1.11) for v_{out} we find:

$$v_{ds1} = v_{s2} = \frac{v_{out}}{m_2 \dfrac{g_{m2}}{g_{d2}} + 1 + \dfrac{g_{d1}}{g_{d2}}} \tag{1.12}$$

where $g_{m2}+g_{mb2}=m_2g_{m2}$. Using the more familiar "r_d" parameters we finally obtain:

$$v_{ds1} = v_{s2} = \frac{v_{out}}{m_2 g_{m2} r_{d2} + 1 + \frac{r_{d2}}{r_{d1}}} \tag{1.13}$$

As long as M_2 is in saturation, $g_{m2}r_{d2} >> 1$, therefore the $v_{ds1} << v_{out}$.

As a result, considering that:

$$v_{out} = v_{ds1} + v_{ds2} \tag{1.14}$$

we find that:

$$v_{out} \cong v_{ds2} \tag{1.15}$$

Equations (1.13) and (1.15) are well representative of the mechanisms that produces the typically high output resistance of cascode structures. In fact, M_2 "absorbs" the largest part of V_{out} variations and "protects" M_1. More precisely, v_{out} variations are transmitted to M_1 through an attenuation of the order of $g_{m2}r_{d2}$. Therefore, as V_{out} varies, V_{DS1} is practically kept constant. Since $V_{GS1}=V_{in}$=constant in this analysis and $V_{BS1}=0$, I_{D1} is controlled only by V_{DS1}. If the latter is nearly constant, then also I_{out} ($=I_{D1}$) is nearly constant confirming the high output resistance.

From (1.8) and (1.13), the output resistance can be easily found:

$$R_{out} = \frac{v_{out}}{i_{out}} = \frac{v_{out}}{i_{d1}} = \frac{v_{out}}{v_{ds1}} r_{d1} = r_{d1} + r_{d2}\left(1 + m g_{m2} r_{d1}\right) \tag{1.16}$$

Large-signal output characteristics of the cascode stage

As V_{out} is progressively reduced, V_{DS2} diminishes at same pace. When eventuallyV_{DS2} gets lower than V_{DSAT2}, so that M_2 gets into triode region, $g_{m2}r_{d2}$ starts getting progressively smaller and M_2 is no more effective in protecting M_1 from V_{out} variations. From this point onward, also V_{DS1} start decreasing and the output current variations becomes more and more important, so that the output resistance enhancement produced by the cascode structure is disrupted.

The V_{out} value at which the output resistance starts increasing significantly is then given by:

$$\min\left(V_{out}\right) \equiv V_{MIN} = V_{DS1} + V_{DSAT2} \tag{1.17}$$

Note that V_{DS1} is determined by V_K and by V_{GS2}, through equation (1.6). Depending on the circuit used to produce V_k, V_{DS1} can be significantly higher than V_{DSAT1}.

The behavior of V_{DS1} and V_{DS2} as a function of V_{out}, corresponding to above discussion, are depicted in Fig. 1.3(a). Note that V_{DS1} is practically constant for $V_{out}>V_{MIN}$. while V_{DS2} follows V_{out}. When V_{out} drops below V_{MIN}, V_{DS1} starts decreasing significantly since the protective effects of M_2 vanishes. Eventually, V_{DS2} gets close to zero and V_{DS1} practically coincides with V_{out}.

The effect on the output current is depicted in Fig. 1.3(b). For $V_{out}>V_{MIN}$, the output current is practically constant, and the curve has only a very small derivative, given by $(Rout)^{-1}$. If V_{DS1Q} is designed to be significantly larger than V_{DSAT1}, as soon as V_{out} gets smaller than V_{MIN}, M_1 is still in saturation with a good margin. At this point, the protective action of M_2 is less effective and V_{DS1} starts to vary as V_{out}. The I_{out} variations are much larger than in the correct V_{out} interval ($V_{out}>V_{MIN}$), but the

behavior of the stage is not yet catastrophic, since M_1, being in saturation, is still relatively insensitive to V_{DS} variations. Eventually, when also V_{DS1} gets smaller than V_{DSAT1}, I_{out} shows a strong dependence on V_{out}. The V_{out} value at which $V_{DS1} = V_{DSAT1}$ is indicated with V_L in Fig. 1.3(b); the correct operating interval is the region for $V_{out} > V_{MIN}$.

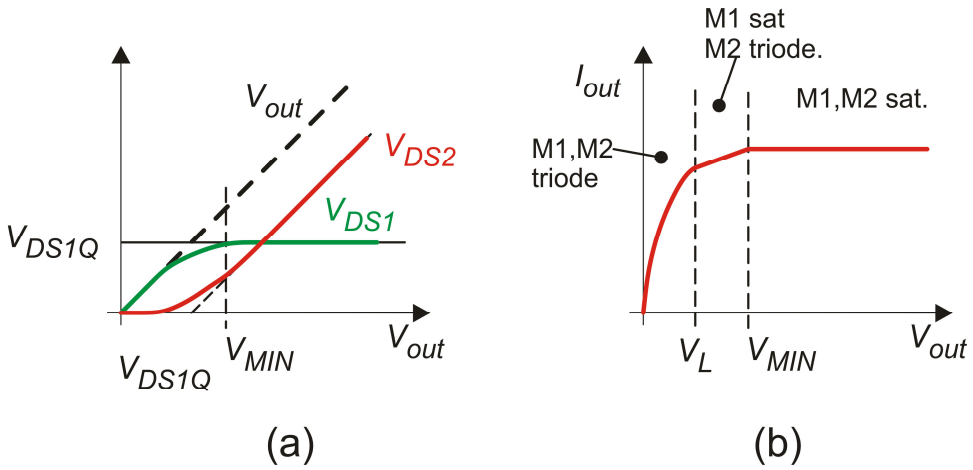

Fig. 1.3. (a) Dependence of M_1, M_2 V_{DS} on V_{out} in a cascode structure; (b) dependence of I_{out} on V_{out}.