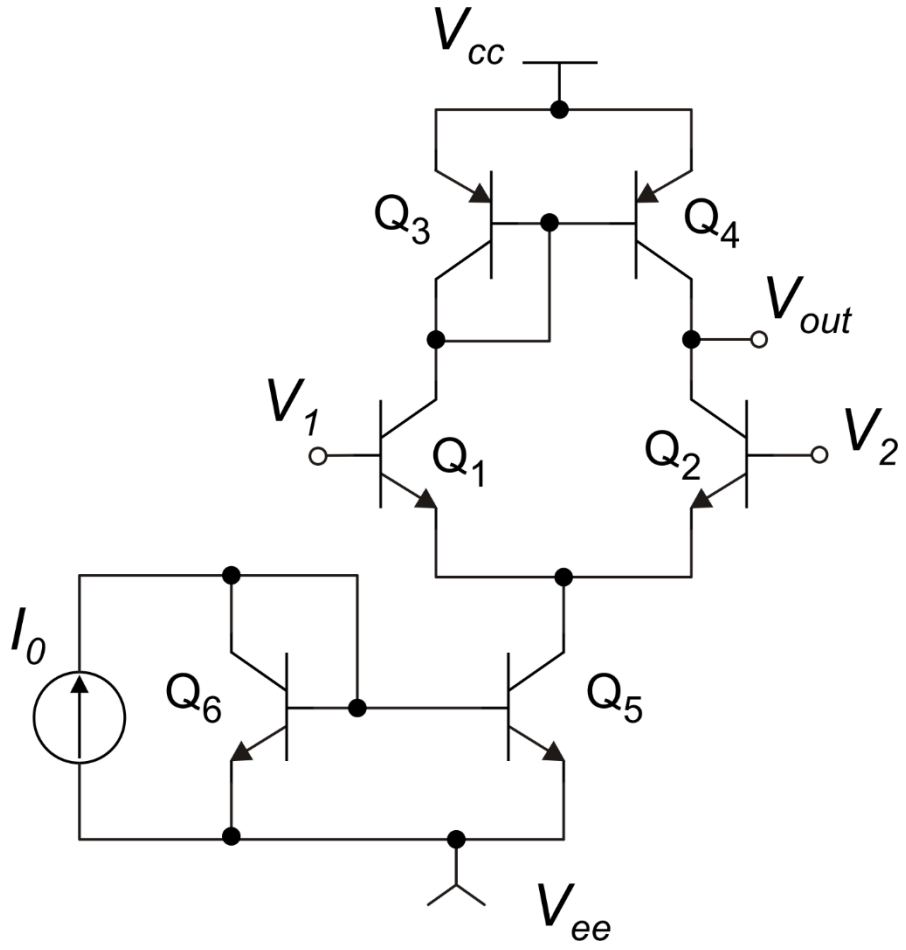
BJT differential amplifier with mirror load

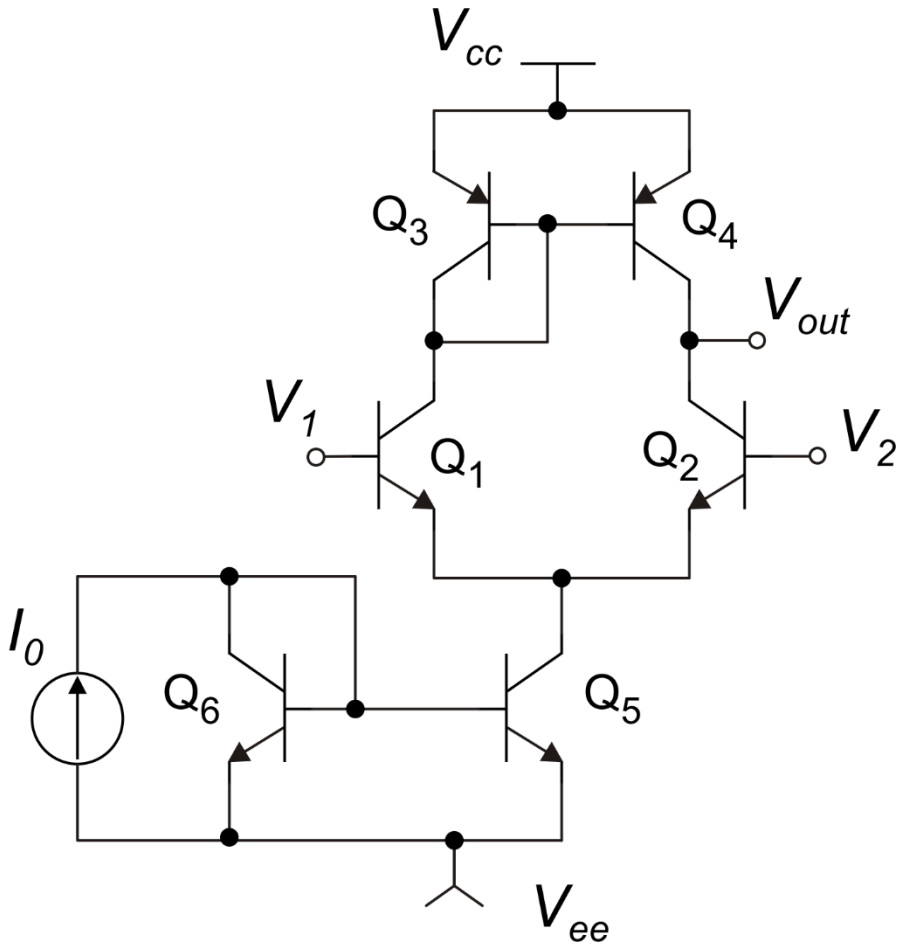


$$A_d = g_{m1} R_{out} = g_{m1} \left(r_{o2} \,//\, r_{04} \right)$$

$$g_{m1} = \frac{I_C}{V_T} \qquad r_{o2} \,//\, r_{o4} = \frac{1}{\frac{I_{C2}}{V_{A2}} + \frac{I_{C4}}{V_{A4}}}$$

$$A_d = \frac{1}{V_T} \frac{1}{\frac{1}{V_{A2}} + \frac{1}{V_{A4}}}$$

BJT differential amplifier with mirror load



$$V_{out-\max} = V_{cc} - V_{CESAT\,4}$$

$$V_{out-\min} = V_C - V_{BE\,2} + V_{CESAT\,2} \cong V_C - 0.5\ \text{V}$$

$$V_{C-\max} = V_{cc} - V_{BE\,3} - V_{CESAT\,1} + V_{BE1} \cong V_{cc} - V_{CESAT\,1}$$

$$V_{C-\min} = V_{ee} + V_{CESAT\,5} + V_{BE1} \cong V_{ee} + 0.8\,\text{V}$$

Gain estimation

$$A_d = \frac{1}{V_T}\,\frac{1}{\frac{1}{V_{A2}}+\frac{1}{V_{A4}}}$$

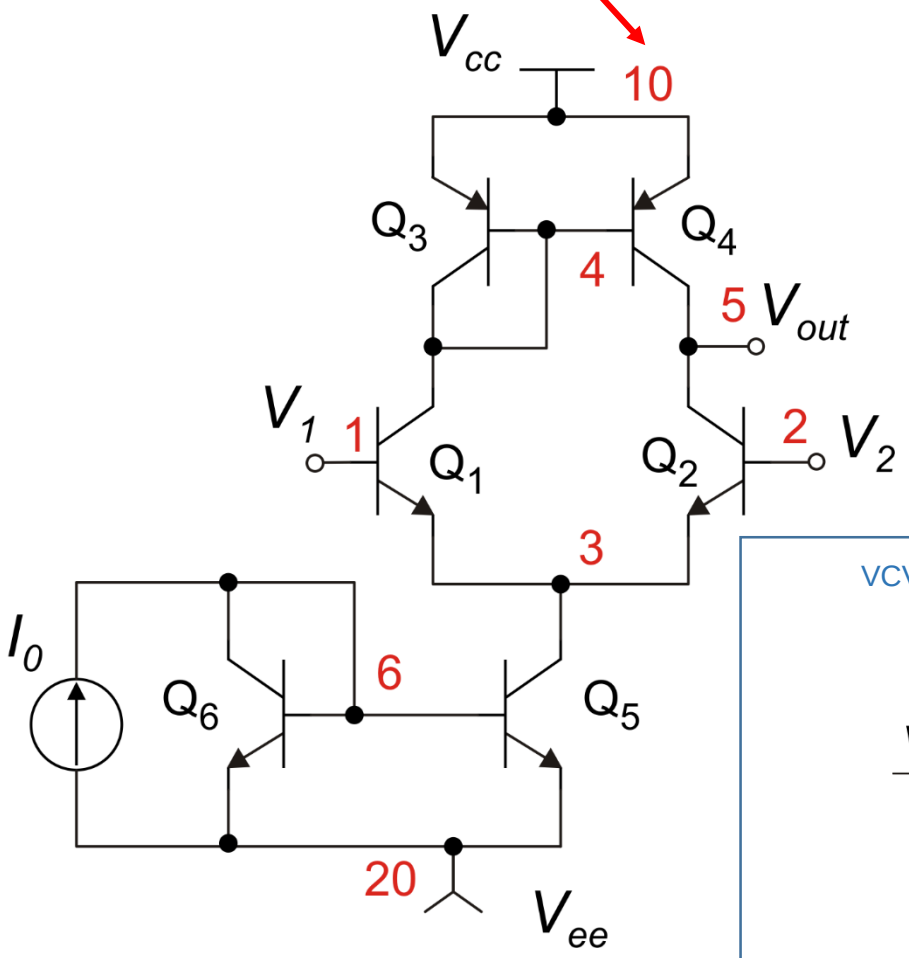
$$A_d = \frac{12.33}{V_T} \cong 490$$

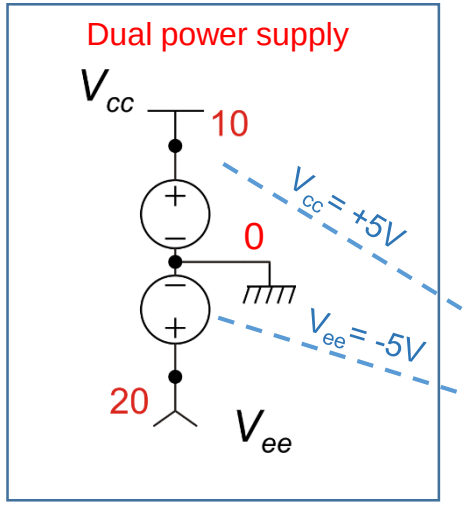
Device models : bipol.lib

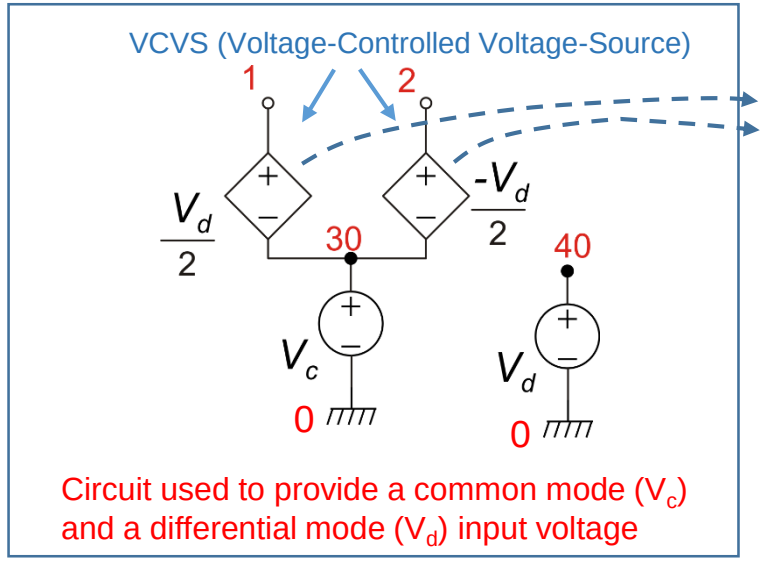
```
*Modello transistore S-T C21, libreria typical
.MODEL NBJT
+ NPN
+ IS=1.00E-018 BF=1.00E+002 BR=1.00E+000 NF=1.00E+000
+ NR=1.00E+000 TF=6.00E-012 TR=1.00E-008 XTF=1.00E+001
+ VTF=1.50E+000 ITF=2.80E-003 PTF=3.75E+001 VAF=4.50E+001
+ VAR=3.00E+000 IKF=3.70E-003 IKR=4.70E-004 ISE=3.40E-017
+ NE=2.00E+000 ISC=1.80E-017 NC=1.50E+000 RE=2.32E+001
+ RB=4.74E+002 IRB=0.00E+000 RBM=5.66E+001 RC=4.10E+002
+ CJE=5.33E-015 VJE=1.05E+000 MJE=1.60E-001 CJC=7.01E-015
+ VJC=8.60E-001 MJC=3.40E-001 XCJC=1.30E-001 CJS=7.26E-015
+ VJS=8.20E-001 MJS=3.20E-001 EG=1.17E+000 XTB=1.70E+000
+ XTI=3.00E+000 KF=0.00E+000 AF=1.00E+000 FC=5.00E-001

*Modello transistore S-T M41, libreria typical
.MODEL PBJT
 + PNP
 + IS=1.00E-017 BF=1.50E+001 BR=4.00E+000 NF=1.00E+000
 + NR=1.00E+000 TF=3.00E-009 TR=3.00E-008 XTF=2.00E+000
 + VTF=1.00E+000 ITF=4.00E-003 PTF=1.50E+001 VAF=1.70E+001
 + VAR=3.30E+001 IKF=4.30E-005 IKR=4.30E-005 ISE=3.00E-015
 + NE=1.70E+000 ISC=1.00E-014 NC=1.70E+000 RE=3.60E+001
 + RB=2.50E+002 IRB=0.00E+000 RBM=2.00E+001 RC=1.48E+002
 + CJE=8.80E-015 VJE=9.00E-001 MJE=2.00E-001 CJC=3.95E-014
 + VJC=9.00E-001 MJC=3.30E-001 XCJC=5.00E-001
 + EG=1.17E+000 XTB=1.70E+000
 + XTI=3.00E+000 KF=0.00E+000 AF=1.00E+000 FC=5.00E-001
*
```

Simulation circuit

Nodes of the circuit
(same as in the netlist)







Spice netlist and commands

```
Q1 4 1 3 20 NBJT
Q2 5 2 3 20 NBJT
Q3 4 4 10 20 PBJT
Q4 5 4 10 20 PBJT
Q5 3 6 20 20 NBJT
Q6 6 6 20 20 NBJT

VCC 10 0 DC 5
VEE 20 0 DC -5
I0 20 6 DC 10u

VC 30 0 DC 0
VD 40 0 DC 0 AC 1 sin(0,10m,1k,0,0,0)
E1 1 30 40 0 0.5
E2 2 30 40 0 -0.5

.DC VD -100m 100m 1m VC -3 4 1
*.AC DEC 10 1 1G
*.tran 10u 3m
.lib bipol.lib

.end
```

1 V stimulus used in AC (small signal frequency response) analysis

Amplitude

Frequency

Sinusoidal stimulus used in time-domain transient (TRAN) simulations

Simulation Instructions

Simply unzip the byt_amp.zip file into an empty folder. Make sure that the folder path is not too long end does not contain spaces.

Three LTSpice input files have been prepared. To trigger the simulation, simply double click on the file icon into the folder. The output plot can be generated by the "add_trace" command (menu "plot settings") and by selecting the V(5) trace. Instruction for their usage are briefly described below.

amp_diff_DC.cir: Simulates the DC output voltage dependence on the input differential voltage for various common mode voltages. Note the effect of the input common mode voltage on the output swing.

amp_diff_DC_gain.cir. As above but only for Vc=0. Add the derivative of the output voltage as a function of the input differential voltage, by adding the trace: D(V(5)). Note that the gain is between 450 and 500. Change the bias current (I0) from 10u to 1u and launch the simulation again. Note that the gain is not substantially changed. Repeat with I0=0.1u and 100u.

amp_diff_AC.cir: Performs an AC simulation with an input differential voltage (Vd) of 1 V and phase 0 degrees. Add the V(5) trace (output voltage) : the magnitude and phase response is shown. Note that an output voltage of more than 100 V simply means that the amplification is more than 100. The AC simulation is performed on the linearized circuit (small signal analysis) so that non-linear and saturation effects do not occur. Note that, for Io=10u, the upper bandwidth limit is around 1 MHz. Reducing the bias current to I0=1u shifts the upper band limit down to 100 kHz. This shows that the higher the current consumption, the faster the amplifier.

amp_diff_TRAN.cir: Performs a transient simulation with a sinusoidal input differential voltage. The amplitude of the input waveform is initially set to 10 mV, that, if the amplifier were really linear with no swing limitation, would result in an output voltage of 5 V amplitude (10 V peak to peak). This is not possible with the real output swing of the amplifier and distortion occurs (the output voltage is nearly a square wave). Reducing the input magnitude to 1 mV, result in a output with non-noticeable distortion. To change the sine magnitude, change the second argument of the sine function assigned to voltage source VD: