1 Wide swing cascode current mirrors.

The "six MOSFET" wide-swing cascode current mirror (low precision)

Conventional cascode mirrors suffer from two important drawbacks, namely (i) relatively high minimum output voltage (V_{min}=V_{GS}+V_{DSAT}) and (ii) quite high input voltage (V_{in}=2V_{GS}). The six MOSFET mirror shown in Fig. 1.1 ("six-MOSFET" cascode mirror) solves the problem of the output voltage range, since an additional voltage shifter (M6 biased by M5) is used to reduce M4 gate voltage, in turn making V_{DS2} smaller than in a standard cascode mirror. We recall here the general expression of the V_{MIN} of a cascode structure:

$$V_{MIN} = V_{DS2} + V_{DSAT4} \tag{1.1}$$

Setting V_{DS2}=V_{DSAT2}, V_{min} can be designed to be as small as 2V_{DSAT}. This condition is satisfied for the current mirror in Fig. 1.1 when the betas of the six MOSFETs are chosen as indicated by the red labels.

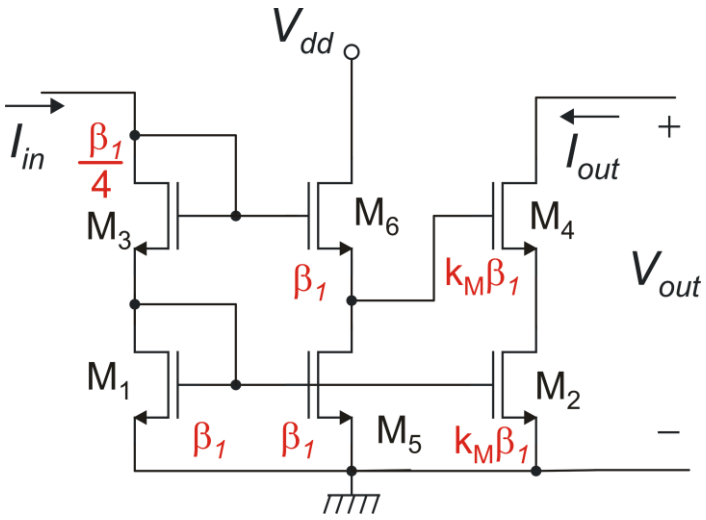

Fig.1.1. Low precision, wide swing cascode current mirror. Red labels close to the MOSFETs indicates the respective betas.

The current gain of the mirror is given by:

$$k_M = \frac{\beta_2}{\beta_1} \cong \frac{I_{D2}}{I_{D1}} = \frac{I_{D4}}{I_{D1}} = \frac{I_{out}}{I_{in}} \tag{1.2}$$

In addition:

$$I_{D6} = I_{D1} = I_{D3} \tag{1.3}$$

From Fig. 1.1, we find:

$$V_{DS2} = V_{GS1} + V_{GS3} - V_{GS6} - V_{GS4} \tag{1.4}$$

Clearly, the V_{GS} in (1.4) cannot be made all equal, otherwise V_{DS2} would be zero. With the device sizing shown in Fig. 1.1 (red labels), β_3 is made smaller, so that its V_{GS} is made larger than the other ones that appear in (1.4).

Expressing V_{GS} as the sum of V_t and V_{GS}-V_t, Eq. (1.4) becomes:

$$V_{DS2} = (V_{GS} - V_t)_1 + (V_{GS} - V_t)_3 - (V_{GS} - V_t)_6 - (V_{GS} - V_t)_4 + V_{t1} + V_{t3} - V_{t6} - V_{t4} \tag{1.5}$$

Neglecting the body effect for simplicity, we can consider that all threshold voltages are equal, so that only the overdrive voltages remain in (1.5). Using the strong inversion expressions for the V_{GS}–V_t, and taking into account (1.2) and (1.3), we find:

$$\begin{aligned} (V_{GS} - V_t)_1 &= \sqrt{\frac{2I_{D1}}{\beta_1}} = \sqrt{\frac{2I_{D6}}{\beta_6}} = (V_{GS} - V_t)_6 = \sqrt{\frac{2I_{D4}}{\beta 4}} = (V_{GS} - V_t)_4 \\ (V_{GS} - V_t)_3 &= \sqrt{\frac{2I_{D3}}{\beta_3}} = 2\sqrt{\frac{2I_{D1}}{\beta_1}} = 2(V_{GS} - V_t)_1 \end{aligned} \tag{1.6}$$

Using relationships (1.6), equation (1.5) becomes:

$$V_{DS2} = (V_{GS} - V_t)_1 = V_{DSAT1} = V_{DSAT2} \tag{1.7}$$

In this way, considering (1.1), we have reached the smallest V_{MIN} values ($2V_{DSAT}$) that can be obtained with a cascode structure. As a side-effect, we have:

$$V_{DS1} = V_{GS1} > V_{DS2} = V_{DSAT2} \tag{1.8}$$

As a result, I_{out} is systematically smaller than the ideal value, equal to $k_M I_{in}$. In addition, the input voltage V_{in} is still equal to $2V_{GS}$. To summarize, the six-MOSFET cascode mirror has the following characteristics:

- Lowest V_{MIN} (advantage);
- Low precision (drawback)
- High input voltage (drawback)

The high-precision, wide-swing cascode current mirror

The six-MOSFET cascode mirror is particularly useful when there is no need of precision and we just need a current source with a high output resistance and the widest output voltage range. However, cases where a high precision is mandatory occur very frequently in analog integrated circuits. The cascode current mirror shown in Fig. Fig.1.2 (a) combines the same small V_{IN} as the six-MOSFET mirror with high precision and an input voltage (V_{in}) as small as a single V_{GS}. This circuit requires an auxiliary voltage, V_k, to bias the gates of M_3 and M_4. We can start the analysis by writing V_{DS1} and V_{DS2}:

$$\begin{aligned} V_{DS1} &= V_k - V_{GS3} \\ V_{DS2} &= V_k - V_{GS4} \end{aligned} \tag{1.9}$$

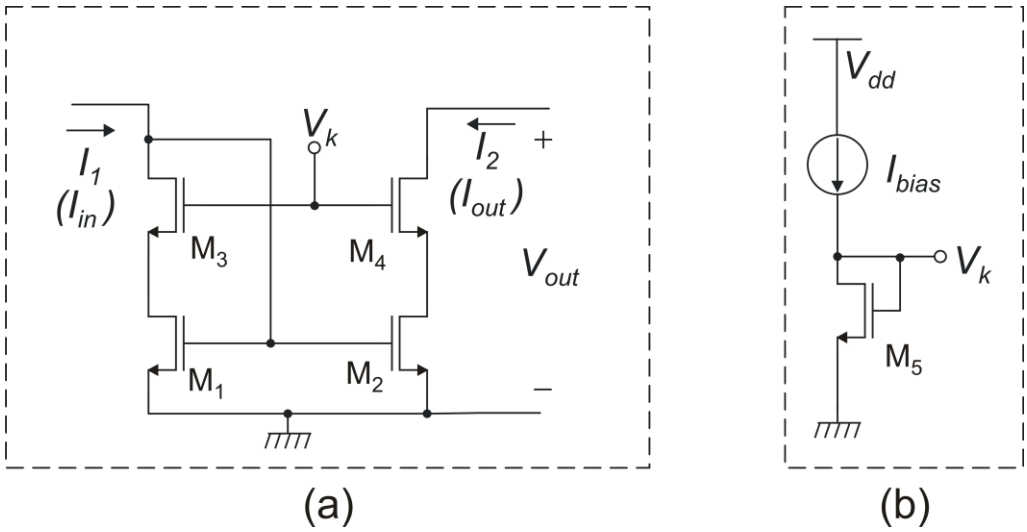

Fig.1.2. (a) High precision, wide swing cascode current mirror with low input voltage. (b) Generation of bias voltage V_K

Using the fundamental design rule of cascode current mirror,

$$\frac{\beta_4}{\beta_3} = \frac{\beta_2}{\beta_1} = k_M \tag{1.10}$$

we obtain $V_{GS3}=V_{GS4}$, as in a standard cascode, so that $V_{DS1}=V_{DS2}$. This relationship guarantees that the mirror is precise, in the sense that, in nominal conditions and for $V_{out}=V_{in}$ (symmetry condition), the actual current gain is equal to the ratio β_2/β_1. Voltage V_k must be chosen to keep M_1 and M_2 in saturation region. If this condition is satisfied, we obtain the typical high output resistance of cascode structures, so that even if symmetry is broken ($V_{out} \neq V_{in}$) the I_{out}/I_{in} ratio remains very close to k_M.

Voltage V_k sets $V_{DS1} = V_{DS2}$ voltage through (1.9). Writing V_{GS4} as the sum of V_{t4} and the overdrive voltage, we get:

$$V_{DS2} = V_k - (V_{GS} - V_t)_4 - V_{t4} \tag{1.11}$$

Note that the source of M4 is not connected to *gnd*. If the fabrication technology is a standard n-well CMOS process, then the body of all MOSFETs coincides with the *gnd* rail. Then, V_{BS4} is not zero and V_{t4} is affected by the body effect. Using a first order approximation, we can write:

$$V_{t4} \cong V_{t0} + (m_4 - 1)V_{SB4} = V_{t0} + (m_4 - 1)V_{DS2} \tag{1.12}$$

where V_{t0} is the threshold voltage for $V_{BS}=0$ and m_4 is the body effect coefficient of M4, equal to $(g_{m4}+g_{mB4})/g_{m4}$. Substituting (1.12) into (1.11), we find:

$$m_4 V_{DS2} = V_k - (V_{GS} - V_t)_4 - V_{t0} \tag{1.13}$$

Voltage V_k is generally be produced by the circuit shown in Fig.1.2 (b). Considering Eq.(1.13) we can write:

$$V_k = V_{GS5} = V_{t5} + \left(V_{GS} - V_t\right)_5 = m_4 V_{DS2} + \left(V_{GS} - V_t\right)_4 + V_{t0} \tag{1.14}$$

Note that the source of M5 is grounded, therefore V_{BS5}=0 and V_{t5} coincides with V_{t0}. Then, (1.14) becomes:

$$\left(V_{GS} - V_t\right)_5 = m_4 V_{DS2} + \left(V_{GS} - V_t\right)_4 \tag{1.15}$$

In order to obtain the minimum V_{MIN} value ($2V_{DSAT}$), we have to impose V_{DS2}=V_{DSAT2}, which in strong inversion result in V_{DS2}=$(V_{GS}-V_t)_2$. Then we have the simple design rule for M5:

$$\left(V_{GS} - V_t\right)_5 = m_4 \left(V_{GS} - V_t\right)_2 + \left(V_{GS} - V_t\right)_4 \tag{1.16}$$

Equation (1.16) states that.

- The V_{GS}-V_t of M5 should be designed to be the sum of M4 V_{GS}-V_t and M2 V_{GS}-V_t increased by a factor around 120 %-140%, depending on the value of m_4.

In the case that the technology allows M4 and M3 bodies to be connected to their sources (e.g. triple well technology), then equation (1.16) should be simplified by removing factor m4.

Another design constraint on V_k derives from the need of also keeping M_3 in saturation region. Note that V_{D3}=V_{GS1}. Therefore, we must guarantee that:

$$V_{D3} = V_{GS1} \geq V_k - V_{t3} \quad = \; V_k - V_{t4} \tag{1.17}$$

where V_{t3}=V_{t4} derive from the property V_{S3}=V_{S4}. Finding V_k from (1.9) and substituting it into (1.17) we obtain the condition:

$$V_{GS1} \geq V_{DS2} + \left(V_{GS} - V_t\right)_4 \tag{1.18}$$

If V_{DS2} is set to the minimum value V_{DSAT2}=V_{DSAT1}=$(V_{GS}$-$V_t)_1$, we can obtain the following simplified expression:

$$V_{t1} \geq \left(V_{GS} - V_t\right)_3 \tag{1.19}$$

With the typical value of the threshold voltages in CMOS processes (hundred millivolts), condition (1.19) can be easily satisfied, since $(V_{GS}$-$V_t)_3$ cab be set as low as 100 mV, while maintaining M3 in strong inversion.

Finally, we note that the input voltage, V_{in}, is simply equal to V_{GS1}, like in simple current mirrors.

To summarize:

- The wide-swing cascode current mirror shown in Fig.1.2 offers a low V_{MIN} (equal to $2V_{DSAT}$), relatively low input voltage (V_{in}=V_{GS}), and also a precise current gain.

- This mirror requires accurate design in order to maintain all MOSFETS in saturation region over the whole range of input currents.