# 1 Process errors

## 1.1 General definitions

Fabrication of an integrated circuit is subjected to errors that make the final product different from the designed device. This problem, which is clearly typical of all industrial processes, needs to be well characterized in order to estimate the actual deviation that can be expected to occur from the ideal case. Let us start from very common definitions. We will focus on a component (e.g. a resistor) integrated on a silicon chip. Of that component, will consider a particular quantity (e.g. its resistance) that we will generically indicate with "*A*". The value of *A* assigned to the given component in the design phase is indicated as "nominal" value ($A_N$). Due to process errors, components integrated in the fabricated chips will show a value of *A* that differs from the nominal value. In addition, different realizations of the same component will show different value of *A*. The best way to represent the variability of the fabricated values (also indicated as "process spread") is using a histogram.

To build a histogram, we need to consider a large number of different specimens of the same component. Let us indicate the number of different samples with "*n*". Among this set, the quantity A assumes a minimum and maximum value. We divide the interval between the minimum and maximum into a series of uniformly sized sub-interval, called "bins", of width $\Delta A$. For each bin, we count the number of samples whose quantity *A* falls into it. A graphical representation of a histogram is shown in Fig.1.1, where the quantity represented in the *y*-axis is the fractional number ($\Delta n/n$) of samples included in each bin.

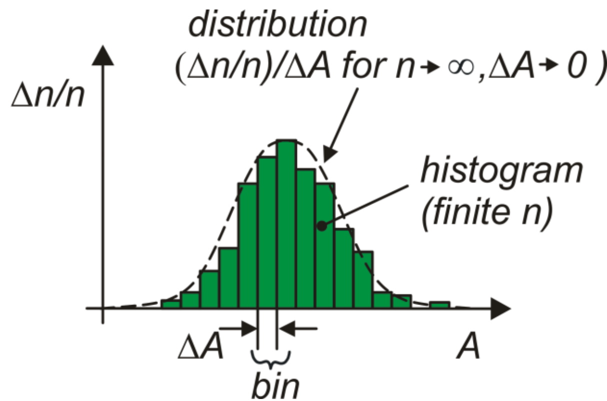


Fig.1.1. Example of histogram.

If we imagine to progressively increase the number of samples and, at the same time, increase the number of bins (reducing the width of each bin), the histogram tends to the ideal distribution that characterize the errors for the given fabrication process. To be more precise, the distribution is obtained by dividing the height of each bar in Fig. 1.1 ($\Delta n/n$) by the width of the bins ($\Delta A$). Since *A* is a continuous variable, the distribution coincides with the probability density function.

The elements of the distribution that are of interest for the production process are illustrated in Fig. 1.2. These elements are summarized below:

$A_N$: this is the nominal value, defined in the design phase.

$A_i$: The value of quantity $A$ for a generic i-th component.

$<A>$: the mean of the distribution.

$e_S$: The systematic error = $<A>-A_N$

$e_R$: Random error for the i-th component = $A_i-<A>$.

The mean of the process can be estimated by taking the mean of $A$ over a large set of components. The actual values of $A$ taken on different components tends to group around the mean value. Differences from the mean value constitute the random error. The difference of the mean with respect to the nominal value is the systematic error. In a correct design, the systematic error should be negligible with respect to random errors. The presence of a non-negligible systematic error can be due to design errors, inaccurate or faulty fabrication process or from inaccuracy of the models used to represent the component behavior. For example, an excess systematic error may derive from neglecting the contact resistance of integrated resistors. In this case, the resistance of the fabricated resistors will be on average larger than the value set by design (nominal value).

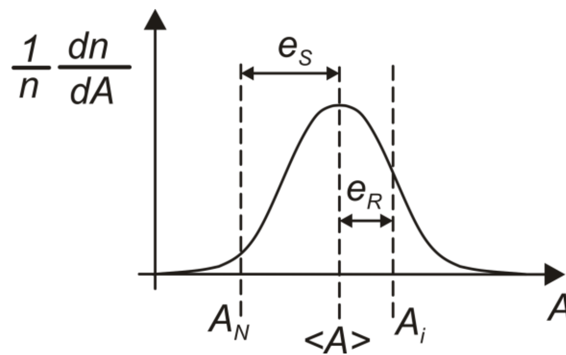


Fig. 1.2. Elements of the distribution.

The magnitude of random errors is well represented by the standard deviation (or standard error), which is the square root of the mean square value of the deviation from the mean. It is defined by:

$$\sigma_A = \sqrt{\left\langle \left(A - <A>\right)^2 \right\rangle} \tag{1.1}$$

If we have a finite set of data (finite sample N dada), the best estimate (unbiased estimate) of the standard deviation of the whole fabrication process is given by:

$$\sigma_A = \sqrt{\frac{\sum_{i=1}^{N} \left(A_i - \mu_{A,N}\right)^2}{N-1}} \tag{1.2}$$

where $\mu_{A,N}$ is the mean calculated over the finite sample of N data. The square of the standard deviation is the variance.

The knowledge of the standard deviation is particularly important when the type of distribution is given, since it allows determining the fraction of data that fall with a given interval around the mean. Note that in most cases of interest for a fabrication process, the distribution is Gaussian. This occurs because fabrication process involve a large number of phenomena that contribute to the total random error. Generally, these phenomena are independent, so that the final distribution tends to a Gaussian even if the single distributions are not Gaussian (central limit theorem). A Gaussian distribution is perfectly determined when its man and standard deviation are given. The fraction of data that falls within an interval centered around the mean is given in the table 1.1:

| Max deviation from the mean | $\pm \sigma$ | $\pm 2\sigma$ | $\pm 3\sigma$ | $\pm 4\sigma$ |
|---|---|---|---|---|
| Fraction of data within the interval | 68.3 % | 95.4 % | 99.7 % | 99.994 % |
| Fraction of data outside the interval | 31.7 % | 4.6 % | 0.3 % | 0.006 % |

Table 1.1: Fraction of data that fall inside or outside an interval around the mean for a Gaussian distribution as a function of the maximum deviation from the mean.

## 1.2 Fabrication errors in a microelectronic process: global and local errors.

Figure 1.3 depicts the different scales of an integrated circuit (IC) fabrication process. At the smallest level there is the chip. At this stage, if we place several identical copies of the same component (nominally identical components) the differences among them are very small. For example, if we design a chip with different copies (instances) of a 1000 Ω resistor, we have good chances to get components that differ from each other by less than a few Ohms. At the second level of the fabrication process, there is the wafer, which collects hundreds or even thousands of dies (chips). The uniformity of process geometrical or physical parameters over a large wafer is much worse than over a single chip. Therefore, if we consider the set of components fabricated on the chip of the whole wafer, differences between these components begin to get significantly larger. Differences gets larger and larger as we consider the successive scale levels, that is the batch of wafers fabricated in a single run and, finally different runs. Differences between components fabricated in different runs can be very large, reaching even ± 20 %. If we consider again a resistor that is designed to have a resistance of 1000 Ω, we can likely get resistors of 800 Ω and 1200 Ω in different runs.

It is useful to introduce two new quantities:

**$\langle A \rangle_{chip}$:** The mean performed on all components integrated on a given chip. This value will change from one chip to another. Even if we cannot place an infinite number of copies of the same component on the same chip, we can imagine being able to reproduce the fabrication of that chip perfectly just in terms of mean values of all parameters (doping levels, oxide thickness, etc.). By this expedient, it is

possible to justify the introduction of a mean, which is a property of a hypothetical process that led to the fabrication of that particular chip, and then refer to an infinite number of components.

**$<A>_{process}$** The mean performed over the totality of components fabricated by that process. Clearly, $<A>_{process}$ is also the mean of $<A>_{chip}$ calculated over all chips produced by that process.

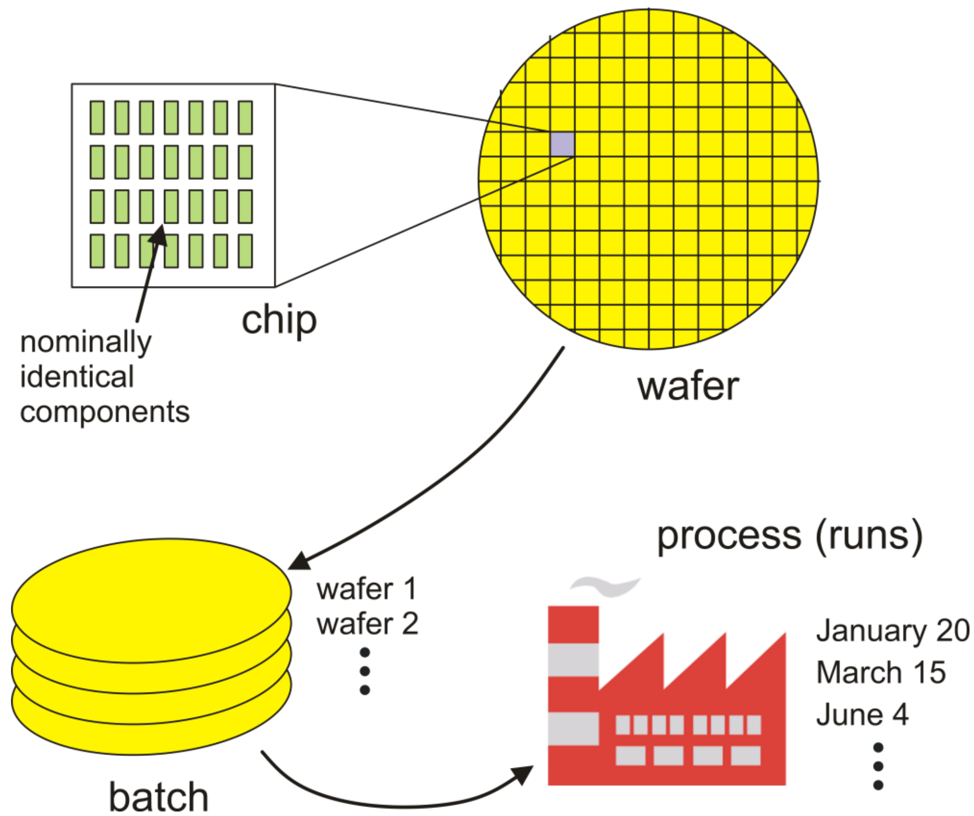


Fig. 1.3. Different scales of the fabrication process.

We can now divide the random errors into two different contributions:

-) **Local errors**, given by the difference between the value of the quantity of interest ($A$) assumed by a component with respect to the mean of the chip where it is located. Considering the discussion at the beginning of this paragraph, there is generally a good uniformity of parameters across a single chip, and then all components in that chip will exhibit values of $A$ very close to $<A>_{chip}$. In other word, local errors are generally very small. Symbolically, the local error for component i-th is given by:

$$e_{local} = A_i - \langle A \rangle_{chip} \tag{1.3}$$

where $<A>_{chip}$ refers to the chip where component i-th is placed .

**-) Global errors**: given by the difference of the mean of a given chip with respect to the mean of the process. This error can be very large, since process parameters can vary much depending on; (i) the

position of the chip in the wafer, (ii) the position of the wafer in the batch and, most importantly, (iii) the run the batch belongs to. (see Fig. 1.3). Symbolically, the global error for a given chip is given by:

$$e_{global} = \langle A \rangle_{chip} - \langle A \rangle_{process} \tag{1.4}$$

Figure 1.4 shows a graphical representation of the various error components. The random error is decomposed into a local and global error. The mean of single chips is distributed according to the global distribution shown at the bottom. The local distributions of two distinct chips ($chip_1$ and $chip_2$) are shown at the top of the figure. Decomposition of the random error is shown for a component belonging to $chip_1$.

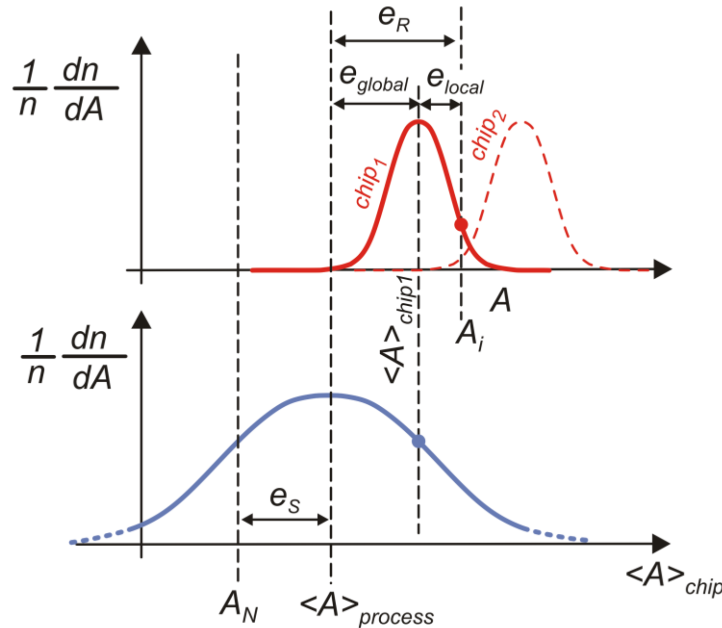


Fig. 1.4. Local (top) and global (bottom) errors. The width of local error distribution is comparatively much smaller than swon in the figure, where it has been artificially enlarged for visibility purpose.

Global and local errors are represented by distinct distributions, characterized by two distinct standard deviations, $\sigma_{global}$ and $\sigma_{local}$, respectively. Different chips are characterized by different local means ($<A>_{chip}$), but all chips have the same standard deviation. This mean that distribution from different chips are simply shifted along the A axis, as shown in Fig. 1.4, but maintain the same shape and width. For the considerations made about the magnitude of global and local errors, we have:

$$\sigma_{global} >> \sigma_{local} \tag{1.5}$$

## 1.3 Matching errors.

A matching error is defined as the difference assumed by quantity $A$ between two nominally identical components. In microelectronics, matching errors are considered only between components that are placed on the same chip. Therefore, matching errors are the consequence of local errors. If consider two component, identical by design, and indicate with $A_1$ and $A_2$ the value assumed by A on component 1 and component 2, respectively, then we can define the two quantities:

$$\begin{cases} \Delta A = A_1 - A_2 \\ \bar{A} = \dfrac{A_1 + A_2}{2} \end{cases} \tag{1.6}$$

Where $\Delta A$ is the matching error, while $\bar{A}$ is the midpoint value. Equations (1.6) can be solved to express $A_1$ and $A_2$ as a function of the matching error and midpoint value:

$$\begin{cases} A_1 = \bar{A} + \dfrac{\Delta A}{2} \\ A_2 = \bar{A} - \dfrac{\Delta A}{2} \end{cases} \tag{1.7}$$

## 1.4 The Pelgrom Model

Matching errors between identical components that are placed very close to each other into the same die are due to local non-uniformity (“granularity”) of the material properties. To understand this, let us consider doping: dopant atoms are randomly distributed over the substrate and the number of dopant atoms that are present inside a given component will obviously vary, depending on the component location. The same occurs, for example, for the gate oxide thickness: the gate oxide is not completely flat but is marked by random small-scale variations (surface roughness) that makes the average oxide thickness different from a device to another. Clearly, on large area devices, these short-length variations tend to have a smaller relative impact, since the device will include areas with both minimum and maximum levels of the physical quantities of interest, producing a sort of compensation.

For this mechanism, matching errors will be smaller in large area devices. This intuitive idea is well represented in a quantitative way by the Pelgrom model [1] that express the standard deviation of the MOSFETS parameters as a function of the device gate area (WL) in the following way:

$$\begin{cases} \sigma_{\Delta V_t} = \dfrac{C_{Vt}}{\sqrt{WL}} \\ \sigma_{\frac{\Delta\beta}{\beta}} = \dfrac{C_{\beta}}{\sqrt{WL}} \end{cases} \tag{1.8}$$

where $C_{Vt}$ and $C_{\beta}$ are constant parameters that are typical of the fabrication process. These matching parameters can be found in the process DRM (Design Rule Manual). This model is generally valid also for other kind of devices, such as resistors, capacitors and bipolar transistors. For example, the standard deviation of the relative matching error of integrated resistors can be expressed by:

$$\sigma_{\frac{\Delta R}{R}} = \frac{C_R}{\sqrt{WL}} \tag{1.9}$$

where $C_R$ is constant that depends on the process and on the type of resistor (polysilicon, high-resistivity polysilicon, diffusion etc.).

**References**

[1] M. J. M. Pelgrom, A. C. J. Duinmaijer, A.P.G. Welbers, “Matching Properties of MOS Transistors, IEEE J. Solid State Circuits, vol. 24, No. 5, pp. 1433-1440, October 1989.