1 Passive Components in Integrated Circuits.

1.1 Resistors

General considerations.

The generic layout of an integrated resistor is shown in Fig.1.1 (a). We have a resistive layer, which is properly shaped to obtain the required resistance. Contacts to an interconnect layer (metal 1 in the example) are placed at both end of the resistive shape, creating the two resistor terminals. The rectangular shape that is included between the contacts is the resistor section, indicated with resistor body.

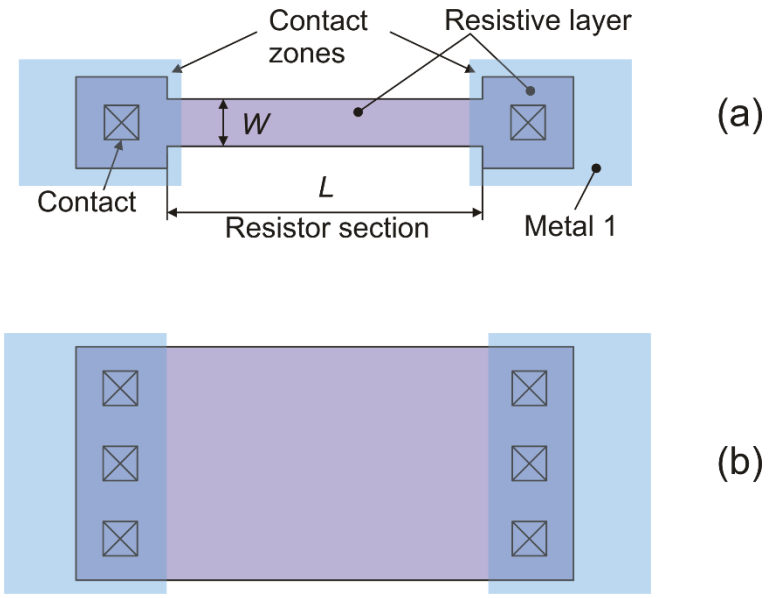

Fig.1.1. Generic resistor layouts.

The resistance of the resistor body is given by:

$$R = R_S \frac{L}{W} \quad with \quad R_S = \frac{\rho}{t} \tag{1.1}$$

where R_S is the so called sheet resistance, ρ and t are the resistivity and thickness of the resistive layer. In order to obtain relatively large resistances, generally the L/W ratio should be made large. To keep dimensions small, W is then set to the minimum value allowed by the design rules. Frequently, this width is not large enough to accommodate a contact. For this reason, the resistor shape is enlarged at both ends, as shown in Fig.1.1(a), introducing a sufficient overlap of the contact object on all sides. If W has to be made much larger than the minimum width (for example to fabricate resistances of low value or to make it withstand large currents) then there is no need to enlarge the resistor ends. For large widths, it is

possible to place more than one contact at both ends, in order to reduce the contact series resistance and increase the maximum current capability of the device.

A process may offer different kind of resistors, which are distinguished by the type of resistive layer. The criteria that are used to choose the best type of resistor are the following:

- **Sheet resistance (R_S)**. To obtain large resistance values, it is necessary to choose the resistor type with the larger R_S. For particularly low resistance values, layers with exceptionally low R_S (such as the metal layers) can be used.
- **Voltage dependence**. Some type of resistors exhibit a large deviation from the ideal V=I/R law. This non-ideality is expressed as a dependence of the resistance on the applied voltage V. A typical expression that is used to model this effect is:

$$R(V) = R(0)[1 + \alpha_{V1} V + \alpha_{V2} V^2] \tag{1.2}$$

  where R(0) is the resistance measured at very low applied voltage while α_{V1} and α_{V2} are empirical coefficients. For applications requiring high precisions, resistors should have negligible dependence on voltage.

- **Temperature dependence**. Temperature dependence is generally expressed with the following formula::

$$R(T) = R(T_0)[1 + \alpha_1 \cdot (T - T_0) + \alpha_2 \cdot (T - T_0)^2] \tag{1.3}$$

  where $R(T_0)$ is the resistance measured at the nominal temperature T_0 (typically 300 K), while α_1 and α_2 are the first order and second order temperature coefficient, respectively. In particular, coefficient α_1, also named TCR (Temperature Coefficient of Resistance) is given by:

$$a_1 = TCR = \frac{1}{R}\frac{dR}{dT} \tag{1.4}$$

- **Parasitic components**. Resistors, as all other integrated devices, are in close contact with the substrate. As a result, there will be parasitic capacitances between the resistor body and the substrate. In the case of diffused resistors, parasitic components include reverse biased junctions between the resistor body and the substrate. Parasitic components contribute to make the resistor behavior non-ideal.

Polysilicon resistors

The cross-section and layout of a polysilicon resistor is shown in Fig.1.2. The polysilicon layer is placed over the field oxide (FOX), providing effective isolation from the substrate. Since polysilicon is salicided by default in modern CMOS processes, if a unsalicided resistor is needed, then the resistor body should be protected from salicide generation by means of a proper layer (Si-Prot in Fig.1.2). Salicide is left on the contact areas in order to reduce the contact series resistance.

Depending on the process, several different types of polysilicon resistors can be available. Table 1.1 includes a few common cases, with the typical sheet resistances and TCRs.

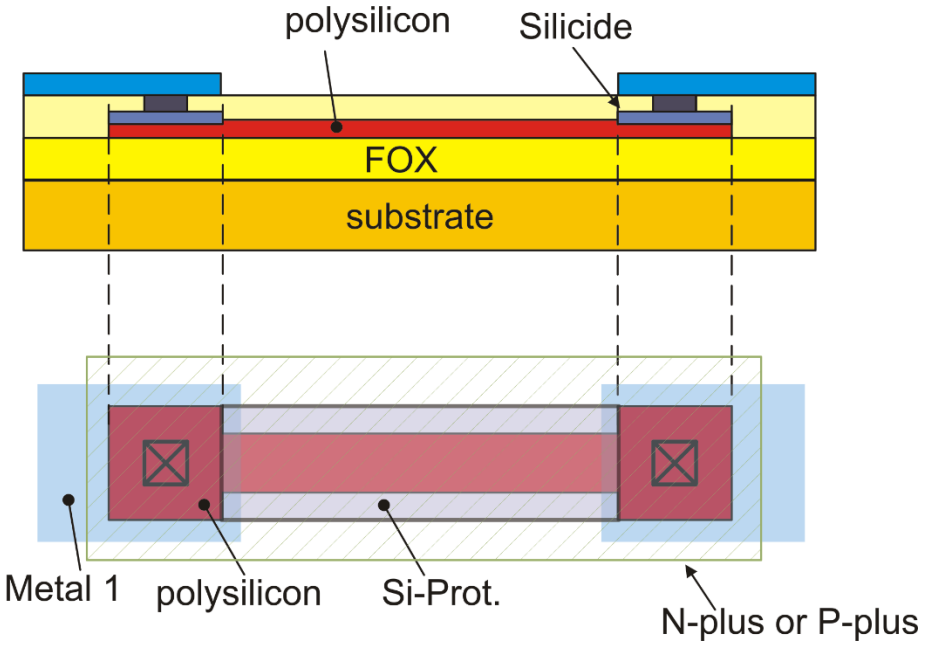

Fig.1.2. Cross-section and layout of a polysilicon resistor.

High-res polysilicon resistors are formed by lightly doped polysilicon. An additional layer (i.e. photomask) is generally required to indicate that the resistor body should not be highly doped as standard polysilicon. N-plus and p-plus polysilicon doping is generally performed with the same implant used to for source/drain doping. Finally, salicided polysilicon resistors, when available, are used when low resistance values are required. All type of polysilicon resistors are marked by very low dependence on voltage, i.e. their current vs voltage characteristics is highly linear.

Table 1.1. Commonly available polysilicon resistors in CMOS processes

Resistor Type	Sheet resistance	TCR	Non linearity (α_{V1})
n-plus polysilicon	30-150 Ω	100-500 ppm/°C	50 ppm / V
p-plus polysilicon	50-400 Ω	250-1000 ppm/°C	-50 ppm / V
high-res polysilicon	400-4000 Ω	–1000 ppm/°C, –3000 ppm/°C	100 ppm / V
Salicided polysilicon	5-10 Ω	2500-3500 ppm/C	-

Diffusion resistors

The resistive layer of a diffused resistor consists of a portion of the crystalline silicon whose doping is opposed to that of the surrounding substrate. In this way, a junction is created between the resistive layer and the substrate. This junction should be properly reverse-biased to provide isolation between the

substrate and the resistive layer. The cross-section and layout of an n-plus resistor implanted into the p-substrate is shown in Fig. 1.3. As in the case of polysilicon, the resistor body should be protected from salicide formation in order to obtain large R_S values. Other possible diffused resistors are p-plus diffusion in n-Well and n-Well diffusion in substrate.

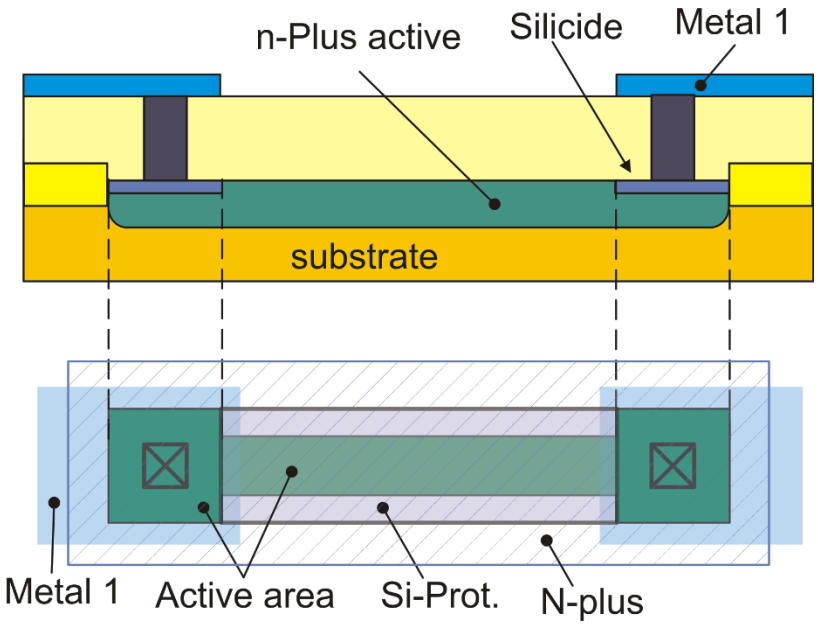

Fig.1.3. Diffused (implanted) resistor: n-plus implant in substrate.

Diffused resistors generally present a relatively large dependence on the applied voltage. The reason is illustrated in Fig.1.4:

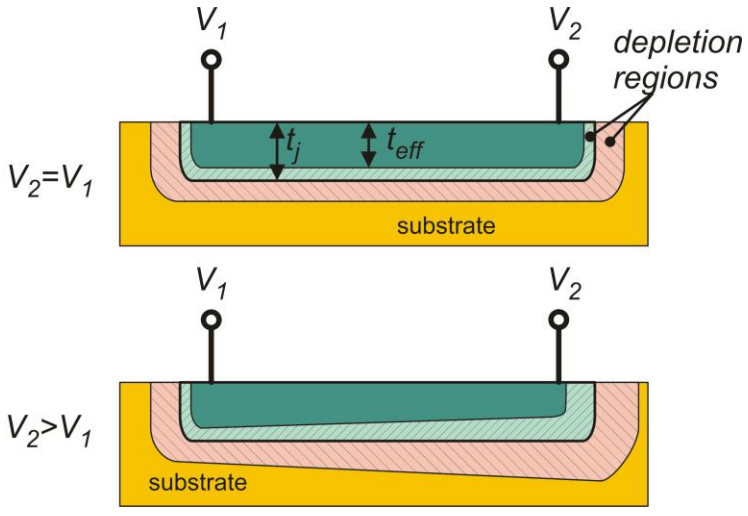

Fig.1.4. Depletion regions in a diffused resistor in the case of null applied voltage (top) and positive applied voltage (bottom).

The problem arises from the depletion regions that form at the boundary between the implant and the substrate. These regions extend also into the resistor body, reducing the effective thickness (t_{eff}) with respect to the thickness of the implant (t_j). The thickness reduction produces a resistance increase, due to expression (1.1). Since the deplation region thickness depends on the voltage difference between the substrate and the implant, the total resistance will also depend on voltage. Note that both the differential voltage across the terminals (V_2-V_1) and the common mode voltage (V_1+V_2)/2 affect the resistance. A change in the common mode voltage with null differential component (Fig.1.4, top) produces an uniform enlargement or reduction of the effective thickness. Application of a differential voltage (Fig.1.4, bottom) produces a restriction of the effective thickness that is maximum at the terminal with higher voltage (V_2 in Fig.1.4). As the applied voltage V2-V1 progressively increases, the effective thickness decreases, producing an increase of the resistance, i.e. a non-linearity in the current-voltage curve. For this reason diffused resistors should be avoided when high linearity have to be achieved in the presence of large applied voltages. Table 1.2 summarizes the characteristics of a few diffused resistor types.

Table 1.2. Parameters of diffused resistors in a CMOS process

Resistor Type	Sheet resistance	TCR	Non linearity (α_{V1})
n-plus on substrate	30-80 Ω	1000-1500 ppm/°C	400 ppm / V
p-plus on n-well	50-150 Ω	1000-1500 ppm/°C	400 ppm / V
n-Well on substrate	400-4000 Ω	2000 -3000 ppm/°C	3000 ppm / V

1.2 Capacitors

General considerations

Capacitances consists of two conductors separated by a thin electrically insulating layer. As for resistors, several parameters have to be taken into account when choosing a capacitor type among the available ones.

- **Capacitance per unit area**: this figure is extremely critical when large capacitors have to be integrated into the chip. Typical values ranges between 1 fF/μm^2 to 8 fF/μm^2.
- **Linearity**: this parameter is related to the dependence of capacitance on the applied voltage. A linear capacitance should be voltage independent. In some cases, the fact that a capacitance depends on voltage can be exploited to obtain tunable resonant circuits.
- **Temperature dependence.** Integrated capacitors exhibit a very low temperature dependence (a few tens of ppm/°C. Thus, this is seldom a critical point.
- **Parasitic components**: as for resistors, capacitors may be affected by parasitic components, typically capacitances to the substrate and parasitic diodes, when insulation is obtained by means of reverse-biased junctions.

Metal-Metal capacitors

Metal-metal capacitors can be divided into two different categories:

- MIM (Metal – Insulator –Metal) capacitors

- MOM (Metal – Oxide – Meta) or “flux” capacitors.

MIM capacitors are simply two stacked metal surfaces separated by a thin dielectric. The latter can be silicon dioxide, a different inorganic insulator or a polymeric insulator. The structure of a MIM capacitor is shown in Fig. 1.5. The capacitance is created between a metal layer and the successive, indicated with “metal (n-1)” and “metal n” in the figure. Due to planarization requirements, it is not convenient to use these two interconnect layers to build the two plates of the capacitor. Instead, an auxiliary metal layer, indicated with “metal (n-1) aux” in the figure is used. This metal layer forms a parallel plate capacitor with the metal (n-1). The two plates are separated by a thin dielectric layer, which is deposited on top of the metal (n-1). The upper plate of the capacitor, made of the auxiliary metal, is connected to the metaln layer by means of standard vias.

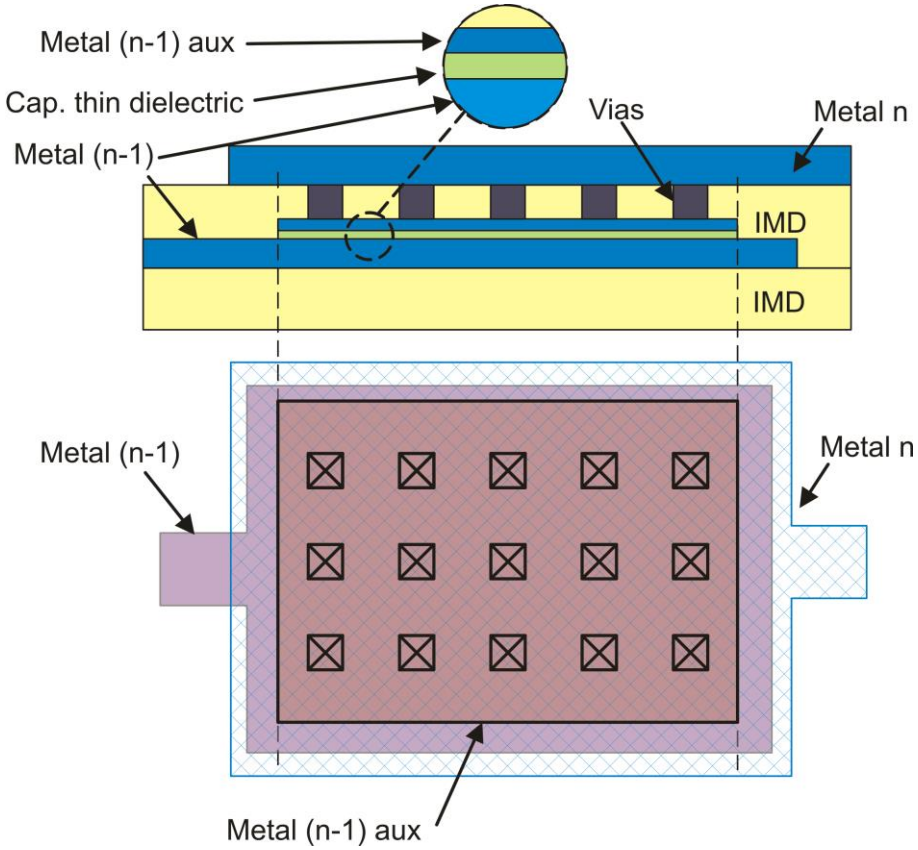

Fig.1.5. Cross-section and layout of a MIM capacitor.

The MIM capacitor layout, shown in Fig.1.5 (bottom) uses only an additional metal layer, the metal (n-1) aux layer, that define the shape of the corresponding metal plate and of the thin dielectric above it.

A MOM capacitor (flux capacitor) is formed by metal lines that are opposed laterally, instead of vertically as in the MIM device. The structure of a MOM capacitor is sketched in Fig.1.6: several parallel lines of a selected metal are alternatively connected to the two terminals of the capacitor, forming a fingered structure. The total capacitance is given by $C_{tot}=(N-1)C_1$, where N is the number of parallel lines and C_1 is the capacitance between two lines.

The advantage of the MOM capacitor is that it does not require additional process steps, because it can be obtained using only standard metal layers. Furthermore, MOM capacitors are generally capable of withstanding much higher voltages.

The main drawback is that, for the same used area, the capacitances that can be obtained are smaller than allowed by MIM capacitors. This problem can be overcome using multi-layer MOM capacitors, which involve several metal layers connected by means of vias, as shown in Fig. 1.7.

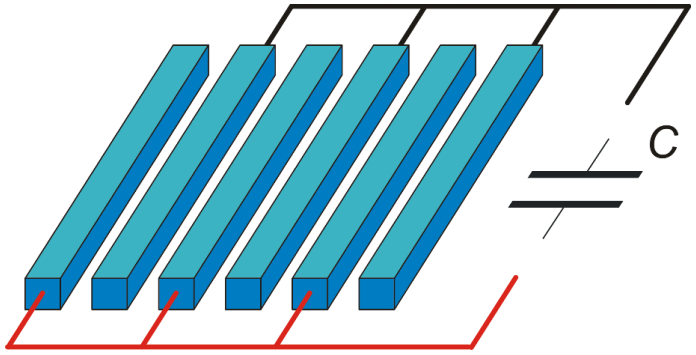

Fig. 1.6. MOM capacitor designed using a single metal layer.

With a MOM capacitor designed with several metal layers, it is possible to match the capacitance-per-unit area of the MIM capacitors. The price to pay is creation of a region that cannot be crossed by interconnections, since all metal layers are used by the capacitor.

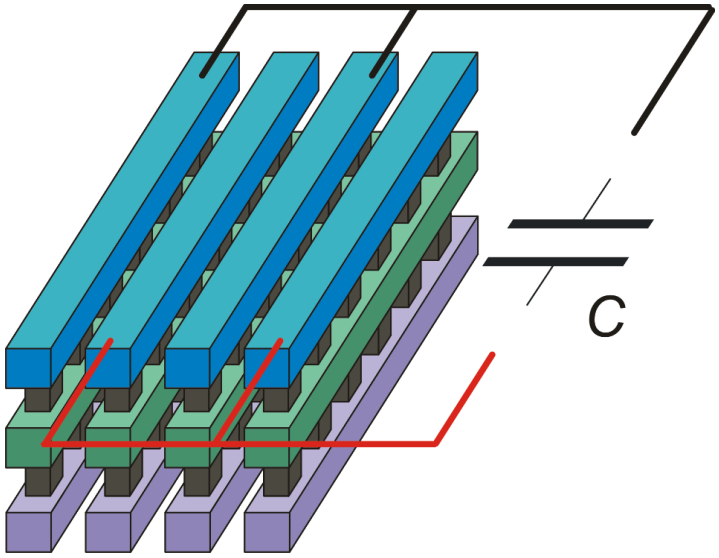

Fig.1.7. Multi-layer MOM capacitor.

On the other hand, the MIM capacitor uses only two of the standard interconnection layers. Frequently, the metal n is the upper metal layer and this allow to put the capacitor on top of active circuits, saving enough lower metal levels to provide basic interconnections.

Polysilicon capacitors

Another common capacitor type is the poly-poly capacitor. This device require two polysilicon levels. Such a feature is frequently available in IC fabrication processes, since it is required to fabricate the floating gates of EEPROMs. The two polysilicon levels are separated by a thin oxide layer, which can be grown by means of thermal oxidation just as the gate oxide. This allows tight control of the dielectric thickness, obtaining high capacitance-per-unit area values. The structure of a poly-poly capacitor is represented in Fig.1.8.

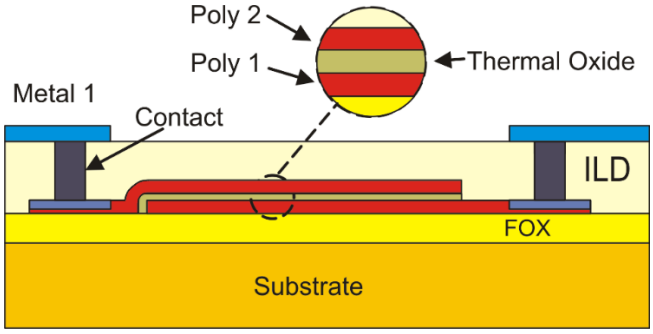

Fig.1.8. Cross-section of a poly-poly capacitor.

When two poly layers are not available, it is possible to create capacitance with a similar high capacitance density (cap. per unit area) using the single poly layer and an n+ diffusion created in the substrate. The structure is shown in Fig.1.9. The dielectric is just the gate oxide of the MOSFETs. The n+ diffusione (indicated with cap-implant in the figure) cannot be obtained using the n-plus layer of the n-MOSFET source and drains, since the n-plus is masked by the poly layer (see the CMOS process flow). Thus, a special diffusion (additional process step and photomask) is required to dope the active area before gate oxide growth and poly deposition.

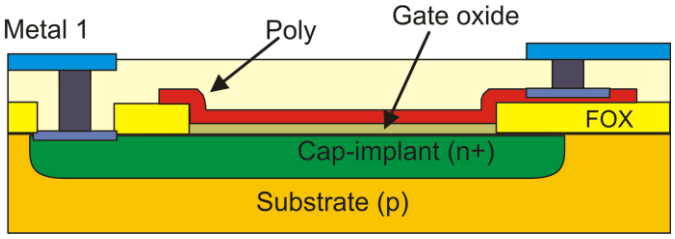

Fig.1.9. Poly-diffusion capacitor.

The main drawback of the poly-diffusion capacitor with respect to the poly-poly capacitors is the parasitic diode between the bottom plate (cap-implant) and the substrate. This diode introduce a leakage current (diode reverse saturation current) and a voltage dependent parasitic capacitance. The bottom plate should be connected only to nodes that are not sensitive to these problems. The top plate (polysilicon) is not affected by significant parasitic components, since it is insulated from the bottom plate by the gate oxide.

Junction capacitors.

These devices consists of a reverse-biased junction. A possible layout is shown in Fig.1.10. The bottom plate is an n-Well, while the top plate is a p+ diffusion. In order to keep the junction reverse biased, the polarity indicated in the figure should be respected. Junction capacitors are strongly nonlinear (voltage

dependent) and a large parasitic diode is present from the bottom-plate to the substrate. These devices are used for frequency compensation purposes when no other capacitor types are available or when the dependence on bias voltage is desirable, as in voltage-controlled capacitors (varactors or varicap diodes) for tuning of resonant circuit.

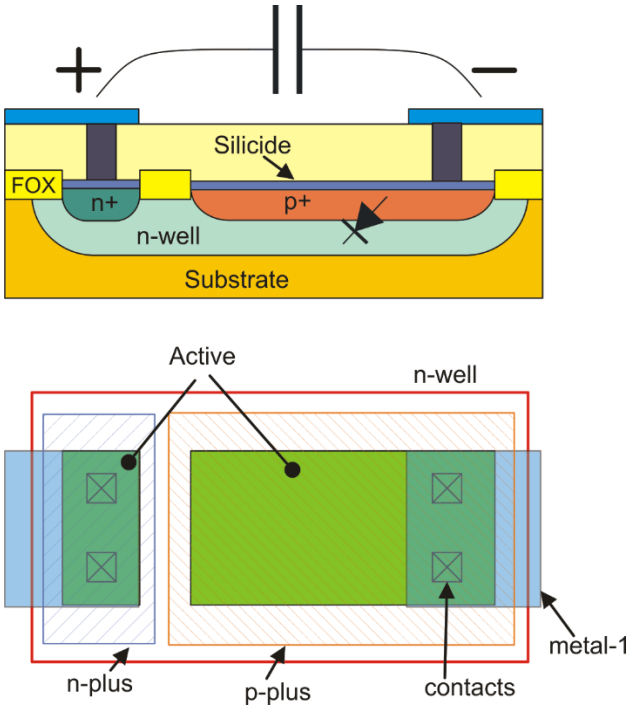

Fig.1.10. Junction capacitor

The properties of frequently used integrated capacitors are summarized in Table 1.3.

Table 1.3. Typical parameters of integrated capacitors

Capacitor Type	Capacitance per unit area	Linearity (voltage dependence)	Parasitic components
MIM	1 fF /μm^2	< 100 ppm/ V	Capacitance to substrate (bottom plate only)
MOM (fkux) 1 metal layer	0.1 fF /μm^2	< 100 ppm/ V	Capacitance to substrate (both terminals only)
MOM (flux) 6 metal layer	1 fF /μm^2	< 100 ppm/ V	Capacitance to substrate (both terminals only)
poly-poly	6 fF /μm^2	100 – 1000 ppm/V	Capacitance to substrate (bottom plate only)
poly-diffusion	6 fF /μm^2	100 – 1000 ppm/V	Diode to Substrate (bottom plate only)
junction	1 fF /μm^2	very –high (up to 30 % / V)	Diode to Substrate (bottom plate). Diode between terminals.

1.3 Integrated inductors

Inductors are the type of passive device that finds more difficulties to be integrated. The main problem is the small inductance values that can be obtained. In practice, due to the small available areas, only inductance values of a few nH can be obtained with integrated inductors. For an inductor to be useful, the magnitude of its impedance should be much greater than interconnect resistances. Since the magnitude of an inductor of inductance L at frequency f is given by $2\pi fL$, in order to have impedances of the order of a few ohm with L in the nano-Henry range, frequencies should be in the GHz range. As a result, integrated inductors can be used only for radio front-ends operating at very high frequencies. The layout of an integrated spiral inductor is shown in Fig.1.11. Notice that at least two metal levels are required. Another problem of integrated inductor is the close distance to the conductive substrate, which favors the development of induced currents. These currents dissipate power, reducing the quality factor of the integrated inductors.

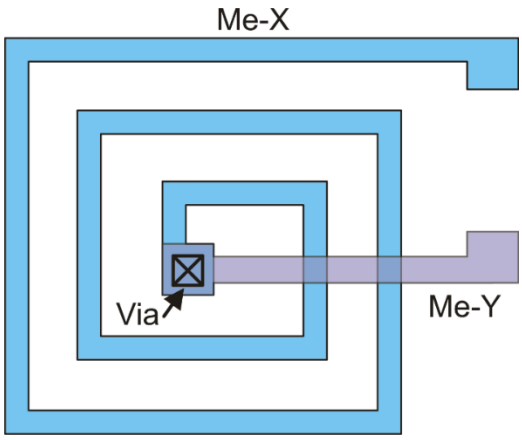

Fig. 1.11. Integrated inductor