1 Considerations on the cascode topology

A simple cascode architecture involving two n-MOSFETs is shown in Fig. 1.1.

Let us consider the effects of variations applied to V_{out}, when V_k and V_{in} are constant. In terms of variations:

$$v_{out} = v_{ds1} + v_{ds2} \tag{1.1}$$

Using the small signal equations of M_1 and M_2, we find:

$$i_{d1} = \frac{v_{ds1}}{r_{d1}} \tag{1.2}$$

$$i_{d2} = g_{m2} v_{gs2} + g_{mB2} v_{bs2} + \frac{v_{ds2}}{r_{d2}} \tag{1.3}$$

where g_{mb2} is M_2 body transconductance, given by:

$$g_{mB2} = (m-1)\cdot g_{m2} \tag{1.4}$$

where m is a coefficient generally varying in the range 1.2-1.3 (see chapter on MOSFET models).

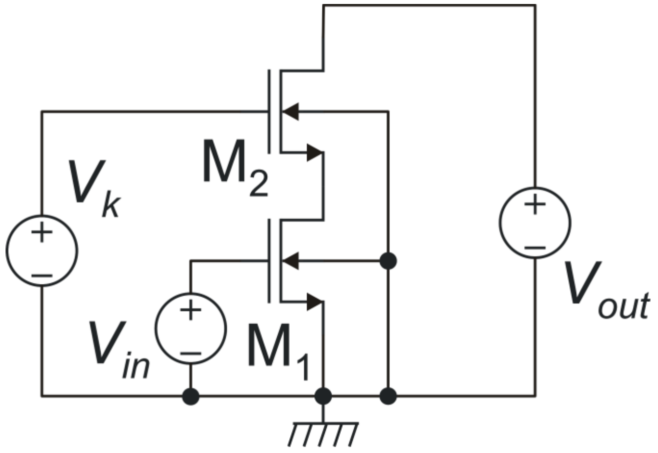

Fig. 1.1. Cascode topology with main voltages indicated.

Since:

$$i_{d2} = i_{d1} \quad v_{gs2} = v_{bs2} = -v_{ds1} \tag{1.5}$$

We find the following equations that ties v_{ds1} and v_{ds2}:

$$\frac{v_{ds1}}{r_{d1}} = -g_{m2}v_{ds1} - g_{mB2}v_{ds1} + \frac{v_{ds2}}{r_{d2}} \tag{1.6}$$

from which we find:

$$v_{ds1}\left(\frac{1}{r_{d1}} + g_{m2} + g_{mB2}\right) = \frac{v_{ds2}}{r_{d2}} \tag{1.7}$$

and finally:

$$v_{ds1} = \frac{v_{ds2}}{r_{d2}\left(g_{m2} + g_{mb2}\right) + \frac{r_{d2}}{r_{d1}}} \tag{1.8}$$

As far as M$_2$ is in saturation, $g_{m2}r_{d2}$>> 1, therefore the following approximation applies:

$$v_{ds1} \cong \frac{v_{ds2}}{r_{d2}\left(g_{m2} + g_{mb2}\right)} = \frac{v_{ds2}}{m \cdot g_{m2}r_{d2}} \quad \text{with} \quad m > 1 \tag{1.9}$$

Then, as v_{out} varies the effects on M$_1$ and M$_2$ are such that $v_{ds1} << v_{ds2}$. As a result, considering (1.1):

$$v_{out} \cong v_{ds2} \tag{1.10}$$

Equations (1.9) and (1.10) are well representative of the mechanisms that produces the typically high output resistance of cascode structures. In fact, M$_2$ “absorbs” the largest part of V_{out} variations and “protects” M1. More precisely, v_{out} variations are transmitted to M$_1$ through an attenuation of the order of $g_{m2}r_{d2}$. Therefore, as V_{out} varies, V$_{DS1}$ is practically kept constant. Since V_{GS1}=V_{in}=constant in this analysis and V_{BS1}=0, I_{D1} is controlled only bay V_{DS1}. If the latter is nearly constant, then also I_{out} (=I_{D1}) is nearly constant confirming the high output resistance. As V_{out} is progressively reduced, V_{DS2} diminishes at same pace. When eventuallyV_{DS2} gets lower than V_{DSAT2}, and M$_2$ gets into triode region, g$_{m2}$rd$_2$ starts getting progressively smaller and M$_2$ is no more effective in protecting M$_1$ from V_{out} variations. From this point on, also V_{DS1} start decreasing and the output current variations becomes more and more important, so that the output resistance enhancement produced by the cascode structure is disrupted.

The V_{out} value at which the output resistance starts increasing significantly is then given by:

$$\min\left(V_{out}\right) \equiv V_{MIN} = V_{DS1} + V_{DSAT2} \tag{1.11}$$

Note that:

$$V_{DS1} = V_K - V_{GS2} \tag{1.12}$$

V_{DS1} is determined by V_K and by V_{GS2}, which are both under control of the designer. Depending on the circuit used to produce V_k, V_{DS1} can be significantly higher than V_{DSAT1}.