1 Wide swing cascode with precise current gain.

Conventional cascode mirrors suffer from two important drawbacks, namely (i) relatively high minimum output voltage ($V_{min}=V_{GS}+V_{DSAT}$) and (ii) quite high input voltage ($V_{in}=2V_{GS}$). The six MOSFET mirror shown in Fig. 1.1 solves the problem of the output voltage range, since V_{min} can be designed to be as small as $2V_{DSAT}$. Unfortunately, its precision is poor, since M_2 and M_1 has different V_{DS}. Furthermore, the input voltage is still $2V_{GS}$.

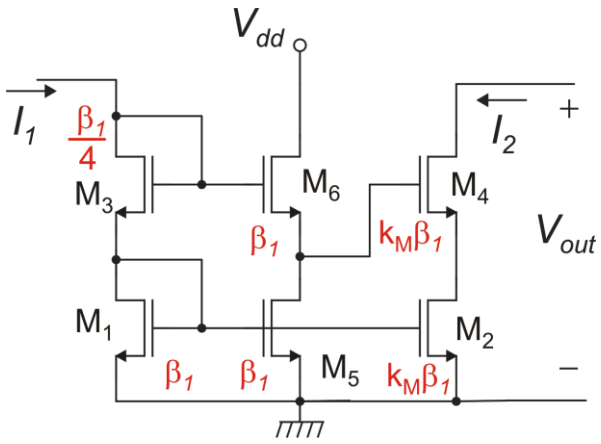

Fig.1.1. Low precision, wide swing cascode current mirror

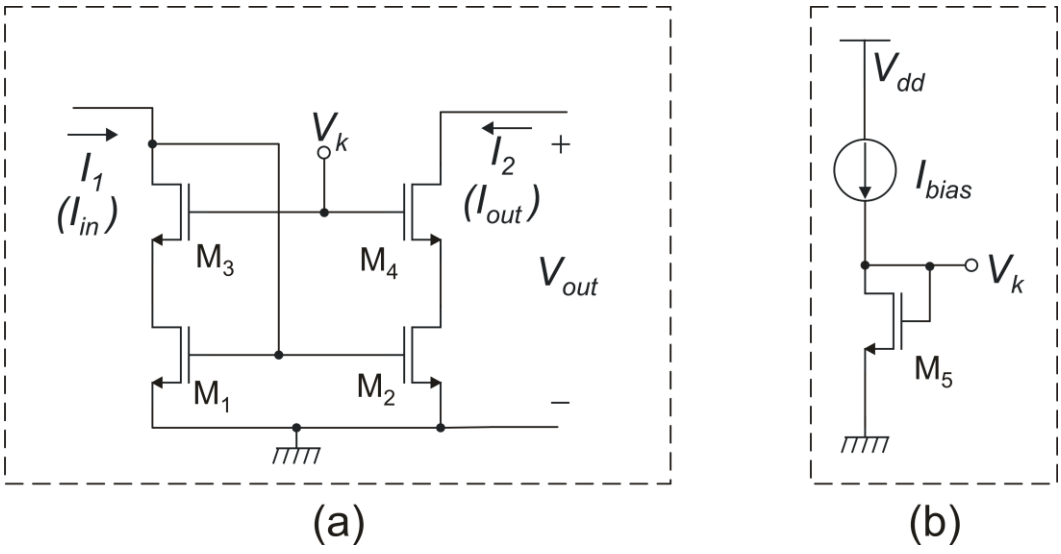

Fig.1.2. (a) High precision, wide swing cascode current mirror with low input voltage. (b) Generation of bias voltage V_K

The cascode mirror shown in Fig.1.2 (a) solves all these problems. It requires an auxiliary voltage, V_k, to bias the gates of M_3 and M_4. To study this circuit, we can start by writing V_{DS1} and V_{DS2}:

$$V_{DS1} = V_k - V_{GS3}$$
$$V_{DS2} = V_k - V_{GS4} \tag{1.1}$$

Choosing $\beta_4/\beta_3=\beta_2/\beta_1=k_M$, we obtain $V_{GS3}=V_{GS4}$, as in a conventional cascode, so that $V_{DS1}=V_{DS2}$. This relationship guarantees that the mirror is precise, in the sense that, in nominal conditions and for $V_{out}=V_{in}$ (symmetry condition), the actual current gain is equal to the ratio β_2/β_1. Voltage V_k must be chosen to keep M_1 and M_2 in saturation region. Therefore:

$$V_k \geq V_{DSAT2} + V_{GS4} \tag{1.2}$$

Voltage V_k can be properly chosen to make V_{DS1} and V_{DS2} close to the transition to triode region, which, in strong inversion means:

$$V_{DS2} \cong V_{DSAT2} = V_{GS2} - V_t \quad \Rightarrow \quad V_{MIN} \cong V_{DSAT2} + V_{DSAT4} \tag{1.3}$$

In this way, V_{MIN} is only equal to $2V_{DSAT}$, which is the minimum value that can be expected from a cascode structure. The condition on V_k becomes:

$$V_k = V_{DS2} + V_{GS4} = (V_{GS} - V_t)_2 + (V_{GS} - V_t)_4 + V_{t4} \tag{1.4}$$

Voltage V_k can be produced by the circuit shown in Fig.1.2 (b). Considering Eq.(1.4) we can write:

$$V_k = V_{GS5} = V_{t5} + (V_{GS} - V_t)_5 = (V_{GS} - V_t)_2 + (V_{GS} - V_t)_4 + V_{t4} \tag{1.5}$$

Note that the source of M_5 is grounded, while M_4 source is at potential V_{DS2}, which, being close to V_{DSAT2}, is of the order of a few hundred millivolts. Therefore, the body effect on V_{t4} is small and we can consider that $V_{t4} \cong V_{t5}$. Then:

$$(V_{GS} - V_t)_5 = (V_{GS} - V_t)_2 + (V_{GS} - V_t)_4 \tag{1.6}$$

Current I_{bias} and M_5 aspect ratio (W/L) should be properly designed to obtain equality (1.6).

Voltage V_k should also keep M_3 in saturation region. Note that $V_{D3}=V_{GS1}$. Therefore, we must guarantee that:

$$V_{D3} = V_{GS1} \geq V_k - V_{t3} \quad = \; V_k - V_{t4} \tag{1.7}$$

where $V_{t3}=V_{t4}$ derive from the property $V_{S3}=V_{S4}$. Substituting the expression of V_k from (1.5) we obtain the condition:

$$V_{GS1} \geq (V_{GS} - V_t)_1 + (V_{GS} - V_t)_3 \tag{1.8}$$

which can be further simplified in:

$$V_{t1} \geq (V_{GS} - V_t)_3 \tag{1.9}$$

With the typical value of the threshold voltages in CMOS processes (hundred millivolts), condition (1.9) can be easily satisfied by setting $(V_{GS}\text{-}V_t)_3$ = 100 mV, i.e. by biasing M3 at the boundary between strong and weak inversion.

Finally, we note that the input voltage is simply equal to V_{GS1}, like in simple current mirrors.

Final considerations.

- The wide-swing cascode current mirror shown in Fig.1.2 offers a low V_{MIN} (equal to $2V_{DSAT}$), relatively low input voltage (V_{in}=V_{GS}), and also a precise current gain.

- This mirror requires accurate design in order to satisfy (1.3) over the whole range of input currents.