Matching Properties of MOS Transistors

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Abstract—**The matching properties of the threshold voltage, substrate factor, and current factor of MOS transistors have been analyzed and measured. Improvements to the existing theory are given, as well as extensions for long-distance matching and rotation of devices. Matching parameters of several processes are compared. The matching results have been verified by measurements and calculations on several basic circuits.**

I. INTRODUCTION

MISMATCH IS THE process that causes time-independent random variations in physical quantities of identically designed devices. Mismatching is a limiting factor in general-purpose analog signal processing, but especially in multiplexed analog systems [1], digital-to-analog converters [2], reference sources, etc. In digital circuits matching can also be important, e.g., in the read and write circuits of digital memories and even in the voltage margins of static RAM cells. The impact of (mis)matching MOS transistors becomes more important because the dimensions of the devices are reduced and the available signal swing decreases.

Despite the widely recognized importance of matching, there are only a limited number of specialized open literature contributions in this field. Shyu *et al.* [3], [4] has analyzed the variation in capacitors and current sources in terms of *local* and *global* variations. Local variations are characterized by a short correlation distance: the concept of local variations is also part of the analysis of this paper. The effect of the global variations is a constant term in Shyu's mismatch description. In the following sections a more detailed description will be used, thereby introducing spacing dependence. The analysis of current mismatch in [4] is based on four physical causes: edge effects, implantation and surface-state charges, oxide effects, and mobility effects. The resulting measurements confirm the global trend in current matching, but matching is not further specified in parameter terms.

Lakshmikumar *et al.* [5] described MOS-transistor matching by means of threshold-voltage and current-factor standard deviations. The starting points were again the possible physical causes. Their analysis of the contributions to the current factor mismatch is not supported by the experiments in this paper. The limited variation in W/L ratios in his experiments cannot distinguish between alternative hypotheses.

This paper is a contribution to the discussion on matching and will include an analysis and measurements of the mismatch in threshold voltage, the current factor, and the substrate factor of the MOS transistor as a function of area, distance, and orientation. The starting point is not the wide range of possible mismatch causes, but a mathematical treatment of classes of mismatch behavior which covers all known area-related physical causes. Then the measurements are used to verify the theory and to derive the unknown constants in the theory. The origins of mismatch in several MOS parameters have been studied by means of additional experiments. The applicability of the results is demonstrated on several basic circuits.

II. ANALYSIS

Mismatch that can be observed between the parameters of a group of equally designed devices (MOS transistors in this paper) is the result of several random processes which occur during every fabrication phase of the devices. This definition excludes batch-to-batch or wafer-to-wafer variations of the absolute value of parameters and unwanted offsets caused by electrical, lithographic, or timing differences.

In general the value of a parameter P is composed of a fixed part and a randomly varying part, resulting in differing values of P at different coordinate pairs (x, y) on the wafer. If the variations are small, the average value of the parameter over any area is given by the integral of $P(x, y)$ over this area. The actual mismatch in parameter P between two identical areas at coordinates (x_1, y_1) and (x_2, y_2) is

$$\Delta P(x_{12}, y_{12}) = \frac{1}{\text{area}} \left\{ \iint_{\text{area}\,(x_1, y_1)} P(x', y')\, dx'\, dy' - \iint_{\text{area}\,(x_2, y_2)} P(x', y')\, dx'\, dy' \right\}. \quad (1)$$

This integral can be interpreted as the convolution of double box functions formed by the integral boundaries with the "mismatch source" function $P(x, y)$. By means of a two-dimensional Fourier transformation the geome-

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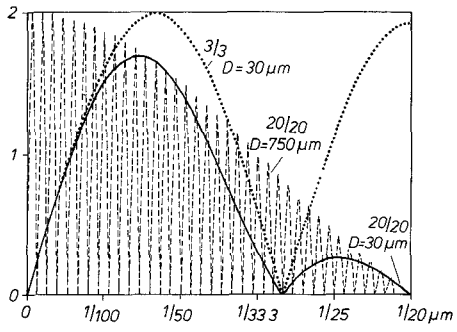


Fig. 1. Geometry functions $|\mathcal{G}(\omega_x, \omega_y)|$ as derived in (3) for a pair of 20/20 transistors spaced at 30 μm, a pair of 3/3 transistors at the same spacing, and a pair of 20/20 transistors spaced at 750 μm. The horizontal axis is $\omega_x/2\pi$ in $1/\mu$m.

try-dependent part is separated from the mismatch source:

$$\Delta\mathcal{P}(\omega_x, \omega_y) = \mathcal{G}(\omega_x, \omega_y)\mathcal{P}(\omega_x, \omega_y). \quad (2)$$

Now the mismatch generating process $\mathcal{P}(\omega_x, \omega_y)$ and the device geometry dependence $\mathcal{G}(\omega_x, \omega_y)$ can be regarded, respectively, as a source that generates spatial frequencies and as a spatial filter function. These two components are analyzed separately.

The geometry function for a pair of rectangular devices with area $W * L$ is found from straightforward Fourier analysis:

$$\mathcal{G}(\omega_x, \omega_y) = \frac{\sin(\omega_x L/2)}{\omega_x L/2} \frac{\sin(\omega_y W/2)}{\omega_x W/2} \{2\sin(\omega_x D_x/2)\}. \quad (3)$$

For convenience it has been assumed that both areas are at a spacing D_x along the x axis. Fig. 1 shows the absolute value of the geometry functions for three types of transistor pairs. The geometry functions have a zero value for $\omega_{x,y} = 0$, thereby eliminating the absolute value of the parameter from the calculations. The geometry functions for other geometries are found in the same way, e.g., a cross-coupled group of four transistors has a geometry function where the last term in brackets in (3) is replaced by $\{\cos(\omega_x D_x/2) - \cos(\omega_y D_y)/2\}$.

After this analysis of the geometry dependence, the specification of the random contribution to $P(x, y)$ or $\mathcal{P}(\omega_x, \omega_y)$ has to be formulated. Two classes of distinct physical mismatch causes are specified in this paper. Every mismatch-generating physical process which fulfils the mathematical properties of these classes results in a similar behavior at the level of mismatching transistor parameters.

The first class of the mismatch-generating process on a parameter P is spatial "white noise" or short-distance variations, with the following features:

- the total mismatch of parameter P is composed of many single events of the mismatch-generating process;
- the effects on the parameter are so small that the contributions to the parameter can be summed;
- the events have a correlation distance much smaller than the transistor dimensions.

Consequently the values of parameter ΔP are normally distributed with zero mean. A process with these properties can be modeled in the Fourier domain as a constant value for all spatial frequencies.

Many known processes which cause mismatching parameters fulfill in first order the above-mentioned mathematical constraints: distribution of ion-implanted, diffused, or substrate ions; local mobility fluctuations; oxide granularity; oxide charges; etc.

The assumption of a short correlation distance implies that no relation exists between matching and the spacing D between two transistors. Wafer maps show, however, a circular parameter-value distribution which originates from wafer fabrication and the oxidation process. This second class of mismatch is a deterministic process but, as the original placement of dies on a wafer is unknown after packaging, the effect of the circular value distribution on the mismatch can be modeled as an *additional* stochastic process with a long correlation distance. In the Fourier domain this effect is modeled as a fixed low-frequency contribution with a spatial frequency inversely proportional to the wafer diameter. The normal distribution is a reasonable approximation for the second class as well.

The representation of parameter fluctuations in the Fourier domain allows easy determination of the power contents, which in turn can be interpreted as the variance (σ^2) of the stochastic parameter:

$$\sigma^2(\Delta P) = \frac{1}{4\pi^2} \int_{\omega_y=-\infty}^{\omega_y=\infty} \int_{\omega_x=-\infty}^{\omega_x=\infty} |\mathcal{G}(\omega_x, \omega_y)|^2 \cdot |\mathcal{P}(\omega_x, \omega_y)|^2 \, d\omega_x \, d\omega_y. \quad (4)$$

The variance of parameter ΔP between two rectangular devices is then found by substitution of (3) and the above-described models for the long and short correlation distance variations in (4):

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2. \quad (5)$$

Here A_P is the area proportionality constant for parameter P, while S_P describes the variation of parameter P with the spacing. The proportionality constants can be measured and used to predict the mismatch variance of a circuit. For a group of four cross-coupled transistors is found in a similar way:

$$\sigma^2(\Delta P) \approx \frac{A_P^2}{2WL} + S_P^2 D_x^2 \frac{D_y^2}{\text{wafer diameter}^2}. \quad (6)$$

The effect of the doubled gate area and of the cancellation of the linear components in the gradient is obvious.

In the experiments reported in the following sections mostly rectangular devices have been used, so (5) describes the variance of the parameters. Secondly the constants in (5) are used in this paper for tracing the causes of parameter mismatch.

III. Matching of MOS Transistors

The matching properties of MOS transistors can be calculated by applying this theory to the parameters of the long-channel MOS model in the linear region:

$$I_D = \beta\left\{\frac{(V_{GS}-V_T-V_{DS}/2)V_{DS}}{1+\theta(V_{GS}-V_T)}\right\} \tag{7}$$

where $\beta = C_{ox}\mu W/L$ is the current factor, and the threshold voltage is composed of a fixed part V_{T0} (0 V substrate voltage) and a substrate-voltage-dependent part: $V_T = V_{T0} + K(\sqrt{|V_{SB}|+2\phi_F} - \sqrt{2\phi_F})$. Within this model V_{T0}, β, and K are used in the matching description; the values found for θ include the mobility reduction effect and the series resistances.

The mismatch causes that are known for V_{T0} and K (e.g., depletion charge, implantations, fixed oxide charge, oxide granularity) satisfy in first order the mathematical requirements demanded by the analysis. So the standard deviations of V_{T0} and K are characterized by (5) with constants A_{VT0}, S_{VT0}, A_K, and S_K:

$$\sigma^2(V_{T0}) = \frac{A_{VT0}^2}{WL} + S_{VT0}^2 D^2$$

$$\sigma^2(K) = \frac{A_K^2}{WL} + S_K^2 D^2. \tag{8}$$

The matching properties of the current factor are derived by examining the mutually independent components W, L, μ, and C_{ox}:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(C_{ox})}{C_{ox}^2} + \frac{\sigma^2(\mu_n)}{\mu_n^2}. \tag{9}$$

The mismatch-generating processes for the gate oxide and the mobility are treated in accordance with (5). The remaining variations in W and L originate from edge roughness and appear as additional terms in the current-factor variance. The analysis of edge roughness is a one-dimensional variant of the analysis in the previous section and leads to $\sigma^2(L) \propto 1/W$ and $\sigma^2(W) \propto 1/L$:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_W^2}{W^2L} + \frac{A_L^2}{WL^2} + \frac{A_\mu^2}{WL} + \frac{A_{Cox}^2}{WL} + S_\beta^2 D^2$$

$$\approx \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \tag{10}$$

where A_W, A_L, A_μ, A_{Cox}, and S_β are process-related constants. The relative mismatch in the current factor can be approximated by the inverse-area description as seen in the last part of (10) if W and L are large enough. The values of W and L for which the inverse-area proportionality still holds must be determined from the measurements.

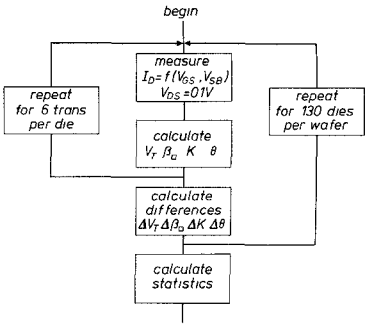


Fig. 2. Measurement procedure.

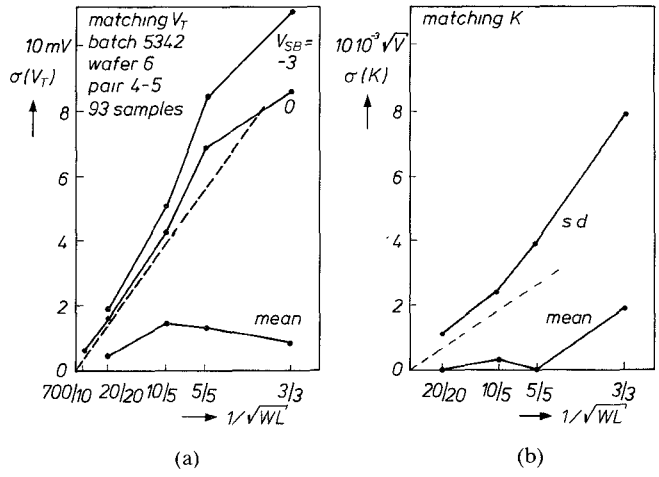
IV. The Measurement Setup

Test circuits have been processed on several batches in industrial n-well CMOS processes. The matching test circuits were part of multiproject chips with about 100 uniformly distributed dies per wafer. The processes are production approved and are used for manufacturing 5-V digital and analog custom designs. The test circuit contains a number of modules for n- and p-channel transistors with several W/L ratios (e.g. 2.4/1.6, 2.4/20, 3/3, 5/5, 20/5 and 20/20 for a 1.6-μm gate-length, 25-nm-gate-oxide process). Each module has six transistors of the same size: a reference device, devices at 30, 250, and 500-μm spacing whose current directions are in line with the reference transistor, one device in parallel and one device at 90° rotation, both at 30-μm distance. Separate modules have been used for special devices e.g. n- and p-channel transistors with $W/L = 700/10$, or cross-coupled pairs.

Several measurement procedures and measurement setups have been considered. The measurements reported in this paper have been made by extracting the parameters in the linear operating region, one transistor after the other. The validity of the data for the saturation region will be shown in Fig. 8.

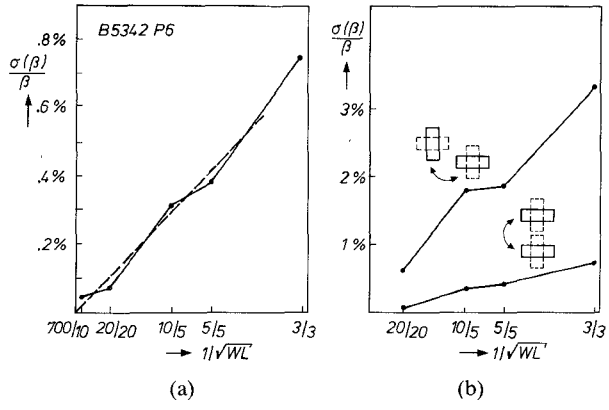
The measurement procedure runs on an automated wafer stepper and is shown in Fig. 2. Special precautions have been taken to eliminate as much disturbance as possible. As these investigations were spread over several years, tests were developed to calibrate the measurement setup itself. In one of these tests the prober is locked to a fixed die position and a complete wafer test cycle is performed: so the same die is measured about 100 times. The resulting parameter standard deviations indicate the obtainable accuracy of the measurement setup: $\sigma(V_T) = 0.15$ mV and $\sigma(\beta)/\beta = 1.5\times10^{-4}$.

A major problem in wafer measurements is the varying resistance in the measurement chain, e.g. prober contact to the bond pad, the aluminum wiring, and relay resistances. Especially at large W/L ratios and gate drive voltages of around 1 V, the equivalent resistance of the MOS transistor in the linear region can be less than 1 kΩ, requiring standard deviations of the series resistances of less than 0.1 Ω. This problem was circumvented by including the series resistance in the parameter extraction. The major effect of series resistance is observed in the mobility degra-



(a) (b)

Fig. 3. Standard deviation of (a) the threshold V_T and (b) the substrate factor K versus the inverse transistor area for an NMOS transistor pair.



(a) (b)

Fig. 4. Standard deviation of (a) the current factor β versus the inverse transistor area for an NMOS transistor pair and (b) a comparison of the standard deviation of β for parallel and rotated placement.

dation factor θ via $\theta := \theta + \beta R_S$; consequently θ is only used to monitor the measurement accuracy.

After correct determination of the parameters and their mutual differences yet another problem arises: a few values are far out of range. Although only a small number of devices suffer from these deviations, their influence can be considerable in a least-squares fit to the expected normal distribution. Therefore a more robust method has been proposed by Rey [6, pp. 126–130]. This method is a rank-linear estimator and is less sensitive for the extreme values of the deviations. Note that the estimation of the standard deviation of an ideal normal distribution by means of 100 samples leads to a relative error larger than 10 percent once out of six times.

V. Results

The experiments reported in this section have been performed in a 2.5-μm, 50-nm gate-oxide CMOS process. The process uses n-wells in $\langle 100 \rangle$ oriented, 5–15 $\Omega \cdot$cm p-type substrates. Fig. 3(a) and (b) shows the relation of the standard deviation[1] in the threshold voltage with 0- and 3-V substrate potentials and the relation of the standard deviation of the substrate factor K with area for a pair of n-channel transistors spaced at 30 μm. A reasonable fit with the predicted $1/\sqrt{WL}$ relation is found. The values for the proportionality constants A_{VT0} and A_K can be derived from the slopes of the curves. In Table I these values have been summarized for the n-channel and p-channel transistors in the 2.5-μm CMOS process. These data are reproducible to within 5 percent for wafers of the same batch; data from wafers processed at two factories over a period of three years vary from $A_{VT0} = 26$ to 34 mV$\cdot\mu$m. Some of the variation in the proportionality constants may be caused by differences in effective area from batch to batch, as in all figures the nominal gate oxides and nominal W and L values have been used.

The curves denoted "mean" show the absolute value of the mean of the measurements. It is clear that this component can be neglected.

In Fig. 3(b) a dashed line indicates the expected A_K for a uniformly doped substrate (1.5×10^{15} cm^{-3}). Although the mismatch of the substrate factor is slightly higher due to additional doping by the threshold adjustment implantation, the substrate doping is most likely the dominant contribution to the substrate factor mismatch.

If it is assumed that the variation of substrate charge does not change in depth, then the contribution of the substrate charge variation in the threshold mismatch can be estimated. The correlation between the variations in substrate factor and the variations in threshold at zero substrate potential is low, and the proportional part of the substrate factor in the threshold ($K\sqrt{2\phi_F}$) will only explain 30 percent of the threshold mismatch variance at 0-V substrate potential. It must be concluded that the substrate charge variation is a major but not a dominant contributor to threshold mismatch.

Fig. 4(a) shows the standard deviation of the relative current factor mismatch as a function of $1/\sqrt{WL}$. Again the measurements confirm the linear relation which holds for the large 700/10 transistor as well as for the nominal 3/3 device. The linear relation with the inverse area has turned out to be the best fit in all experiments (see, e.g., Fig. 6). The data from [5, figs. 3 and 4] fit also to the linear relationship as only W/L ratios of 2 and 4 have been used. From these experiments edge roughness seems not to be a major mismatch factor, leaving mobility and gate oxide as possible mismatch causes.

Fig. 4(b) compares the effect of rotated transistor placement with parallel placement (copied from Fig. 4(a)) on the current factor. The threshold and substrate-factor mismatch is identical for rotated and parallel placement; only the current factor is affected. The proportionality constant A_β for a parallel pair reproduces very well over several

[1] In the theoretical description, the symbol "σ" is used for the standard deviation. The same symbol will be used to indicate the estimations of the standard deviations in the measurements, although this estimator is in fact a stochastic variable.

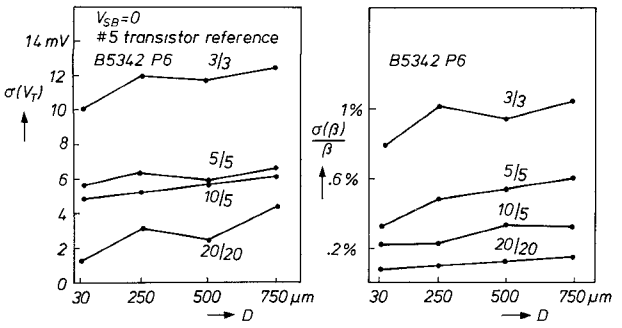


Fig. 5. Standard deviation of (a) V_T and (b) β versus the distance of the devices for an NMOS transistor pair.

TABLE I
MATCHING DATA FOR NMOS AND PMOS TRANSISTOR PAIRS IN A 50-nm GATE OXIDE, 2.5-μm n-WELL PROCESS

parameter	n-channel s.d.	p-channel s.d.	unit
A_{VT0}	30	35	mVμm
A_β	2.3	3.2	%μm
A_K	16×10^{-3}	12×10^{-3}	$V^{0.5}\mu$m
S_{VT0}	4	4	μV/μm
S_β	2	2	$10^{-6}/\mu$m
S_K	4	4	$10^{-6}V^{0.5}/\mu$m

batches: 2.1 to 2.5 percent·μm. The mismatch of rotated pairs varies considerably with wafer and batch. It is unlikely that the variance in transistor dimensions or gate oxide causes the effect observed in Fig. 4(b). Local mobility variations can be a possible explanation for the rotation-dependent mismatch.

The effect of an increased distance between the matching devices is observed in Fig. 5(a) and (b). The relative effect on the mismatch due to the distance is only significant for large-area devices with a considerable spacing. Correlation of the threshold-voltage variations with the current-factor variations shows that there is no significant mutual component for closely spaced transistor pairs: gate-oxide granularity is consequently not an important mismatch cause that affects both threshold voltage and current factor. The correlation for large-area devices goes to -0.35 for maximum spacings, probably due to the increased importance of the long correlation distance circular gradients, which are caused by oxide gradients or wafer doping gradients.

From Fig. 5(a) and (b) the proportionality constants S_{VT0} and S_β can be extracted. Table I compares the data for n-channel and p-channel devices. The most notable difference is in A_β, which again is attributed to differences in mobility behavior.

Several other experiments have been performed showing no significant effects on the matching properties of the transistor parameters: parallel or in-line placement, heating the wafers to 100°C (see also Fig. 9), wafers with or without scratch protection, and varying the threshold implantation doses.

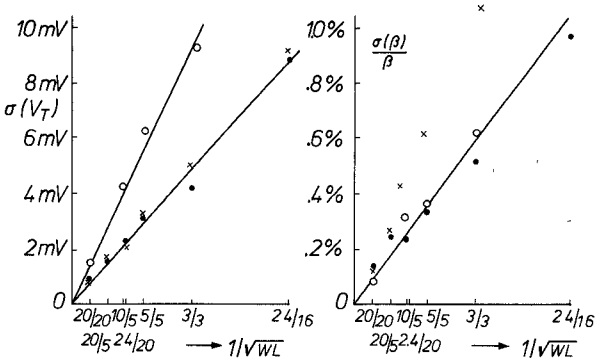


Fig. 6. Standard deviation of (a) V_T and (b) β versus the square root of the inverse area of an NMOS transistor pair for a 25-nm gate-oxide process (dots) and a 50-nm gate-oxide process (circles). Crosses are measurements on devices processed in a 25-nm process with direct wafer writing. The cross for the 2.4/1.6 device is at 2.2 percent.

VI. MATCHING IN DIFFERENT PROCESSES

During this investigation several batches have been processed in other CMOS processes. The main differences are the nominal gate oxides (50, 35, and 25 nm) and the minimum gate length (2.5, 2, and 1.6 μm). For obtaining smaller feature sizes several generally used measures were taken e.g., LDD transistors, anti-punch-through, and interconnect extensions. The results of two 25-nm gate-oxide batches are compared to the results of a 50-nm gate-oxide batch in Fig. 6. It is clear that the threshold mismatch nearly halves with thinner gate oxides, whereas the current-factor mismatch remains constant.

The measurements indicated with circles were performed on devices processed with mask lithography (5× reticle). The crosses indicate measurements on devices that were fabricated with direct-wafer writing (DWW). There is no effect on the threshold matching, but the current-factor matching strongly deviates for smaller geometries. This nonlinear curvature is the only observation where the larger edge roughness (caused by DWW) may have some influence (see first part of (10)).

Fig. 7 summarizes the proportionality constants that have been found in the course of this investigation (dots) and the proportionality constants calculated from data measured and published by others (e.g., [5]). The data are presented as a function of the gate oxide; however this is certainly not the only variable between the cited processes. Yet a linear relation is suggested in the threshold proportionality factor, which can be explained by assuming that a similar charge quantity causes the mismatch in all processes. If a Poisson process is assumed then this charge quantity must be of the order of 3×10^{11} to 10^{12} cm^{-2}. The experiments reported in the previous sections indicate that the substrate doping is part of this charge with a minor role for implanted charge. The dominant contribution to the mismatch charge is still the subject of investigation. Table II reflects the present opinion on the causes of mismatch.

The proportionality constant for the current factor has

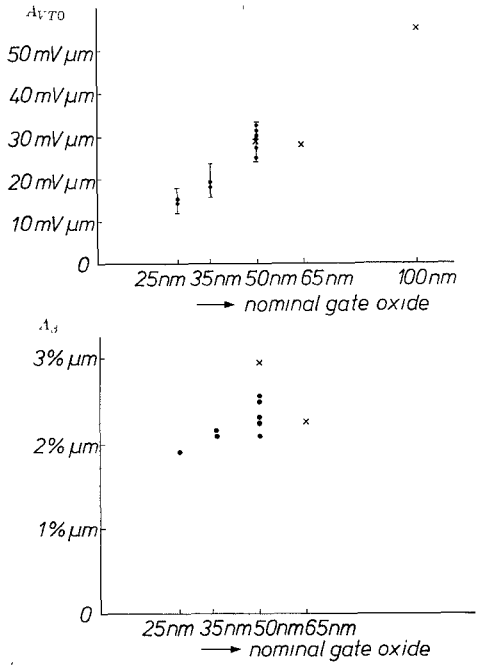


Fig. 7. Proportionality constants for the threshold mismatch and the current factor as a function of the nominal gate oxide of the process. Dots are measurements by the authors; crosses indicate other sources, e.g., [5]. Each point corresponds to the data of several wafers of one batch.

TABLE II
SUMMARY OF MISMATCH CAUSES
A major cause is +, a dominant cause is + + +, question marks indicate doubts

	threshold voltage V_{T0}	current factor β	substrate factor K
Short distance variations			
Gate oxide		?	
Substrate doping	+		+++
Implantations	+?		
Fixed oxide charge	++?		
Edge roughness		only in DWW	
Mobility		+++	
Lithography		?	
Long distance gradients			
Gate oxide	+	+	+
Substrate dope	+		+

no clear relation to the process parameters. This observation, combined with the linear relation with the inverse area found for the current factor mismatch, the rotation effect, and the increased PMOS mismatch, seems to reduce the importance of lithography, edge roughness, or oxide granularity as the dominant current-factor mismatch cause. Local mobility variations are a possible cause.

The proportionality factor of the substrate factor (not shown) is as expected linear with the oxide thickness for comparable substrate dopings.

VII. Matching in Circuits

The above results can be applied to many areas of analog integrated circuit design. In this paper these results are applied to a current source and to a bandgap reference circuit. The first circuit consists of two 20/20 transistors in a 25-nm gate-oxide process connected as parallel current sources to a 5-V supply (see Fig. 8). The measured standard deviation of the currents is plotted as a function of the gate-to-source voltage (dots). Moreover the standard deviation can be calculated using the mismatch data and

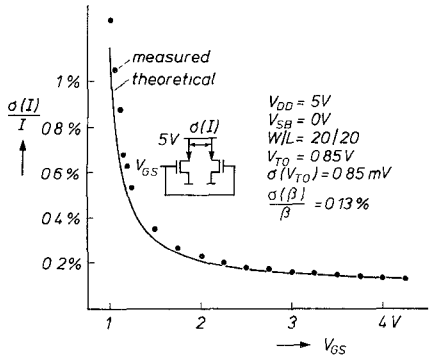


Fig. 8. Standard deviation of the current in an NMOS transistor pair connected to 5-V drain potential. Dots are measurement points; the solid curve has been calculated from extracted mismatch data.

$$\frac{\sigma^2(I_d)}{I_d^2} = \frac{4\sigma^2(V_{T0})}{(V_{GS}-V_{T0})^2} + \frac{\sigma^2(\beta)}{\beta^2}. \tag{11}$$

This figure shows that the measured mismatch is well predicted by the model although the parameter extraction has been done in the linear region of MOS operation. It is clear that the best matching currents are obtained at high gate voltages. At gate voltage close to weak inversion the relative current mismatch will not "explode," but stabilize at a level given by $q\sigma(V_{T0})/mkT \approx 4$ percent. From (11) the gate–source potential can be calculated for which the threshold and current-factor mismatch equally contribute to the relative current mismatch: $V_{GS} = V_{T0} + 2A_{VT0}/A_\beta$. This value ($V_{T0} + 1.5$ V) is independent of the W/L ratio and tends to decrease linearly with the gate-oxide thickness.

If the values of Fig. 8 are multiplied by half of the effective drive voltage, the corresponding standard deviation in the gate-to-source potential is found. This situation occurs, e.g., at the input of an amplifier. Now the minimum standard deviation in V_{GS} is obtained for low V_{GS} values. A more complicated example for current-source mismatch in a current-routing digital-to-analog converter is given in [2].

Fig. 9 shows a set of output curves of a standard bandgap circuit of 70 dies on one wafer. The circuit uses parasitic vertical p-n-p transistors in an n-well 50-nm-gate-oxide CMOS process, p-type diffusions as resistors, and a CMOS op amp. Obviously the expected second-order temperature behavior is present, but there is a spread in absolute output voltage with $\sigma(V_{bg}) = 19$ mV. This mismatch is due to variations in the three components of the circuit: the p-n-p transistors, the resistors, and the op amp. The absolute value of the base–emitter potential of the bipolar devices has been measured; it contributes directly to the absolute value of the output due to the processing accuracy (6 mV). The mismatch component (0.14 mV) between both base–emitter potentials is amplified by the

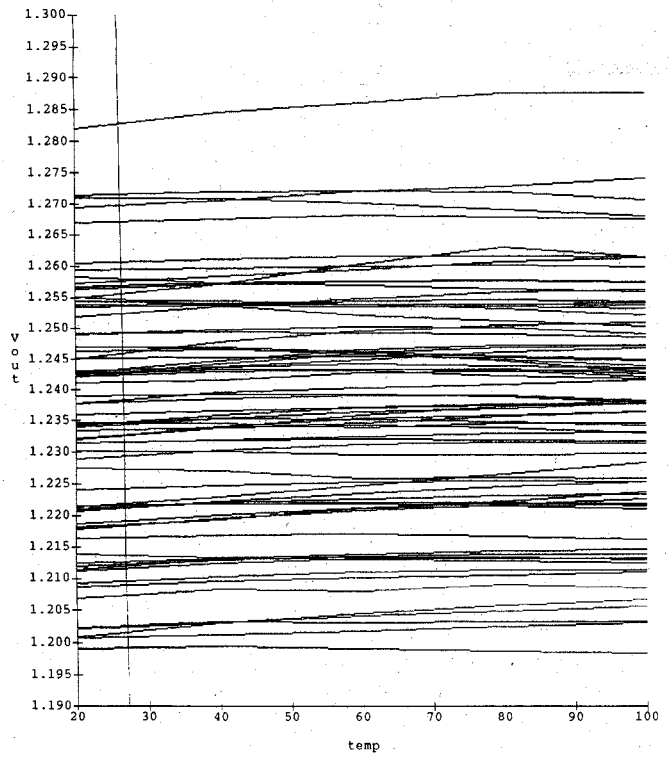


Fig. 9. Typical output curves of 70 bandgap circuits measured on one wafer for a temperature range of 20–100°C.

resistor ratio to give 1.5 mV. The resistors cause an output standard deviation due to their mutual ratio mismatch within one circuit (0.3 mV) and due to the variation of the absolute resistance value over the wafer (0.7 mV). The op amp is the main cause of output variation with 18 mV, which corresponds to 1.6-mV standard deviation at the input.

Using the mismatch data from Figs. 3 and 4 on the folded cascode input stage of the op amp yields a standard deviation of the input voltage of 1.7 mV, which is composed of a 1.6-mV threshold related mismatch and a 0.35-mV current-factor related mismatch, which numerically explains the variation in the bandgap voltage.

With Fig. 3 a trade-off can be made between op-amp area and accuracy: an output-voltage variance of, e.g., 9 mV can be obtained in this circuit configuration if the op-amp mismatch is reduced to 0.6 mV, requiring nine times as much gate area for the input stage, resulting in 0.1-mm^2 active gate area.

Finally a remark must be made with respect to the "offset-cancellation" or "auto-zero" technique, e.g., [7]. This technique aims at eliminating the offsets in comparators or op amps by means of switches and capacitance(s). One switch sets the op amp in unity gain while a second switch allows the input capacitance to be charged to the input offset. The threshold-dependent gate charge contains mismatch contributions of the switching MOS and will again give rise to mismatch voltages. The available time and the ratio of the gate capacitance of the critical switch and the storage capacitance determine the resulting mismatch.

VIII. Conclusions

The variance of the threshold voltage, the current factor, and the substrate factor are inversely proportional to the transistor area. The mismatch in threshold voltage dominates the transistor performance for normal gate–source potentials. Charge components are believed to contribute to the mismatch in threshold voltage and mobility variations influence the current-factor variance. The spacing between transistors can be ignored for transistor areas less than 100 μm^2. It is shown that thinner gate oxides decrease the threshold and substrate-factor mismatch while the relative current-factor mismatch remains almost constant. Comparing data of several production facilities indicates that matching is not strongly varying for these facilities.

Several examples show that mismatch data can predict the performance of circuits.

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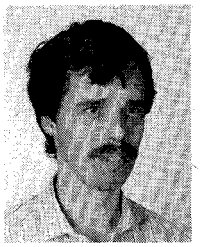

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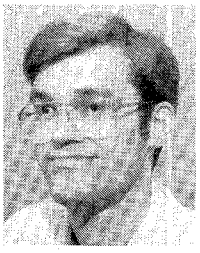

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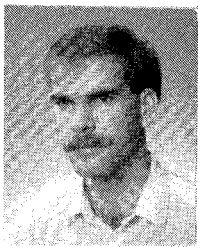

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