MOSFET Modeling for Analog Circuit CAD: Problems and Prospects

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Abstract—**The requirements for good MOSFET modeling are discussed, as they apply to usage in analog and mixed analog–digital design. A set of benchmark tests that can be easily performed by the reader are given, and it is argued that most CAD models today cannot pass all the tests, even for simple, long-channel devices at room temperature. A number of other problems are discussed, and in certain cases specific cures are suggested. The issue of parameter extraction is addressed. Finally, the context of model development and usage is considered, and it is argued that some of the factors responsible for the problems encountered in the modeling effort are of a nontechnical nature.**

I. Introduction

THE modeling of MOS transistors for computer-aided design has been driven by the needs of digital circuit designers for many years. Popular "yardsticks" for judging device models, such as the mean-square error criterion for the current, pass several models with high marks, and may indeed be adequate for models intended for digital circuit design. Yet, when these same models are used for analog work, the outcome is very different: analog circuit parameters, as predicted through the use of such models, can be severely in error. This paper discusses why this happens, suggests ways to clearly demonstrate the magnitude of the problem, and in certain cases recommends cures.

A. Context of Today's Modeling Needs

Three unquestionable technological trends set the stage for today's device modeling for analog work:

1) The trend towards mixed analog–digital chips, not only for direct interfacing to the physical world, but also for aiding digital systems to increase their performance. The recent disk-drive chips (see, for example, [1], [2]) and even analog-assisted microprocessor chips (see, for example, [3]), are manifestations of this trend. It is predicted that in a few years, most chips will contain at least some analog circuits in them.

2) The trend towards low-voltage operation, both for reasons of compatibility with digital technology, and to meet the needs of battery-operated equipment.

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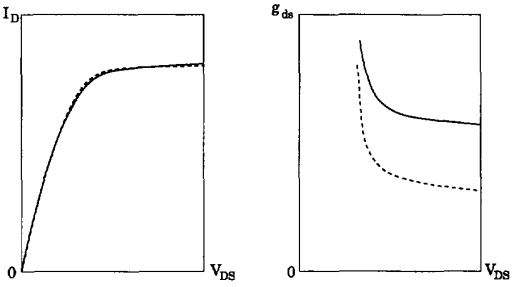

(a) (b)

Fig. 1. (a) I_D–V_{DS} characteristics as they may result from measurement (solid line) and simulation (broken line); excellent agreement is observed. (b) The output conductance resulting from taking the slopes in (a); the agreement is very poor. [4]

3) The trend towards higher speeds, which continues unabated in the analog world in view of the need for a variety of equipment such as high-speed disk drives and wireless communication systems.

Today, designing a high-speed analog circuit with a low-voltage power supply is a big challenge: most MOSFET models in existence cannot handle low-voltage or high-speed operation adequately, let alone a combination of both.

B. The Special Nature of Analog Modeling Needs

Success in analog modeling often relies on the details that, to the digital circuit designer and his/her modeling support team, seem irrelevant. As an example, consider Fig. 1(a) [4]. It would seem that the model (broken line) is an adequate representation of the experiment (solid line). Yet, consider the drain–source small-signal conductance g_{ds}, given by the slope of the I_D–V_{DS} characteristics: for the case of Fig. 1(a), that slope is given in Fig. 1(b), and a very large discrepancy becomes obvious. To argue about the seriousness of this problem, one need only recall that amplifier voltage can be inversely proportional to sums of g_{ds} quantities.

As a separate example, consider the situation in Fig. 2, where two different models have been fitted to I_D–V_{DS} measurements, both with "excellent accuracy." For a sinusoidal V_{DS} variation, though, totally different shapes in I_D variation are predicted, leading to totally different distortion predictions by the two models.

From such examples, it becomes obvious that, if somebody claims a model to give good drain current fit to measurements, all we can conclude is that, maybe, the model can predict

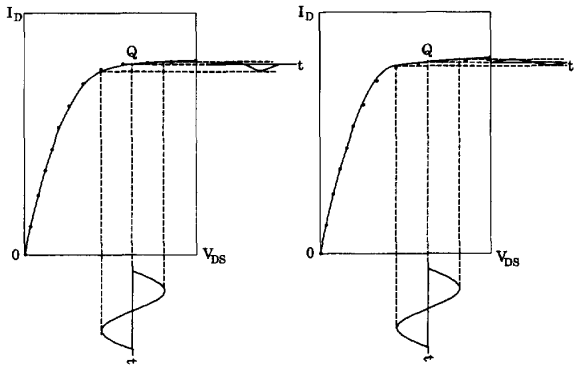

Fig. 2. Illustration of how two different models, both fitting measured *I–V* data (dots) with excellent accuracy, can predict totally different drain current distortion for a sinusoidal drain–source voltage variation.

satisfactorily the bias point of an analog circuit. Since the design of such a circuit involves much more than just bias point evaluation, many more requirements would need to be met by the model before we could call it adequate for analog work. This leads us to the following section.

II. Requirements for Good " Analog" Models

A MOSFET model for analog circuit design should ideally satisfy the following criteria:

1) The model should, of course, meet common requirements for digital work, such as reasonable *I–V* characteristic accuracy, shift register speed prediction, charge conservation, etc.

2) It should give accurate values for all small-signal quantities such as g_m, g_{mb}, g_{ds}, and capacitances. In particular, all of these parameters should be *continuous* with respect to *any* terminal voltage.

3) It should give good results even when the device operates nonquasi-statically, or at least it should degrade gracefully for such operation, as frequency is increased.

4) It should give accurate predictions for both white and 1/*f* noise, including in the triode region.

5) It should meet requirements 1)–4) above over large bias ranges, including $V_{SB} \neq 0$, and encompassing the weak, moderate, and strong inversion regions.

6) It should do all of the above over the temperature range of interest.

7) It should do all of the above for any combination of channel width and length values, from the minimum specified upwards.

8) The user should only have to specify the geometrical dimensions for each device, and *one* set of model parameters valid for *all* devices of the same type and independent of dimensions.

9) The model should provide a flag every time it is attempted to use it outside its limits of validity. For example, if the model is quasi-static and one attempts to use it, say, around the unity-gain frequency of the device, a warning should be given to the user that the result may be inaccurate.

10) The model should have as few parameters as possible (but just enough), and those parameters should be linked as strongly as possible to ones related to the device structure and fabrication processing (e.g., oxide thickness, substrate doping, junction depth). This would allow meaningful worst-case simulations and predictions. Empirical parameters without physical meaning should be avoided as much as possible. This requirement strongly points to the direction of a *physics-based model.*

11) The model should be linked to an efficient parameter extraction method; one could even go so far as to say that parameter extraction should be constantly kept in mind during model development from the beginning. The number of required test devices and tests for parameter extraction should be as small as possible.

12) The model should ideally provide links to device and reliability simulators.

Phenomena that would need to be addressed by the developer of a model meeting the above criteria include weak and moderate inversion, nonquasi-static effects, nonuniform substrate effects (e.g., the dependence of the effective body coefficient on body bias), noise, channel length modulation, drain-induced barrier lowering, substrate currents and their manifestation in the body effect and noise, parameter dependence on geometry, velocity saturation, mobility dependence on gate, body, and drain potentials, source resistance (including its voltage dependence), LDD structure-related effects, and others, all with their temperature dependence. Many of these effects have been extensively studied, but some have not been adequately incorporated in CAD models. This paper is not a proper place to provide a guide to the hundreds of papers discussing phenomena in MOS transistors. The reader is referred to several books [4]–[6], where an extensive bibliography is provided.

How close are popular models to meeting the criteria listed above? Unfortunately, not too close. Indeed, the performance of most of them is sad *even* for simple, long-channel devices at room temperature. We hope to prove this with the help of the following sections.

III. A Set of Benchmark Tests

Rather than trying to convince the reader about the sad state of affairs when it comes to MOSFET modeling for analog work, we propose that the reader him/herself run a few tests that speak for themselves. We have found these very useful over the years, as a necessary (but not sufficient) set of tests a model should pass before we can begin to trust it for analog work. Ideally, the tests should be *quantitative* comparisons to measured data; however, even if such data are not available, one can get very useful indications by running just the simulations indicated since they will at least show whether the model being tested gives a correct *qualitative* behavior. Some examples of how well popular models fare when put to these tests will be given along the way, but we will avoid giving numerical comparisons, as we do not want to limit our comments to specific models with specific parameter

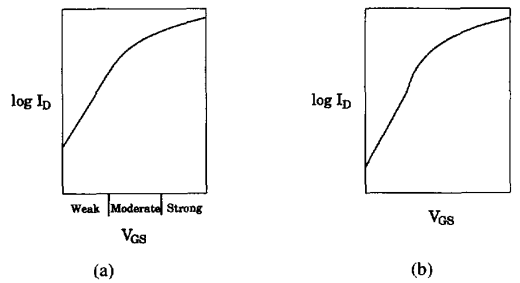

Fig. 3. Log I_D versus V_{GS} for fixed V_{DS} and V_{SB}. (a) A qualitatively correct curve. (b) A curve using the level 2 Spice model.

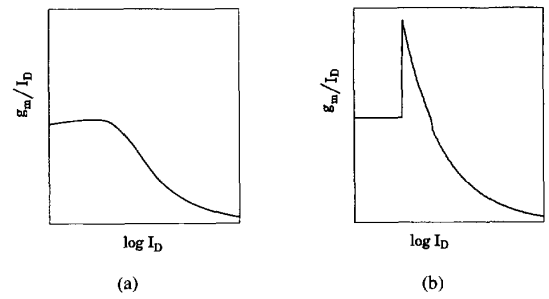

Fig. 4. g_m/I_D versus $\log(I_D)$. (a) A qualitatively correct curve. (b) A curve using the level 2 Spice model.

values. All tests are to be done using nonminimum geometries (long and wide channels) at room temperature.

Benchmark Test 0: Strong Inversion Current

This test concerns basic *I–V* characteristics accuracy; if this test fails, the model may be unsuitable even for digital circuit work. In strong inversion, and with $V_{SB} = 0$, plot I_D versus V_{DS}, with V_{GS} as a parameter, for two devices: one with a small, and one with a large value of the body effect coefficient (γ), but with the same mobility-oxide capacitance product. Contrary to what is predicted by simple models often used for hand analysis, for the *same* V_{GS}–V_T values, the two devices should behave significantly different [4]. Notably, the device with the large γ should exhibit lower $V_{DS,SAT}$ values and lower saturation current. For example, for $\gamma = 0.5\,\mathrm{V}^{1/2}$, the above quantities can be about 20% lower than for a small-γ device. This is a consequence of the fact that the body effect causes the bulk charge to vary significantly along the channel [4]. This effect is neglected in the Spice level 1 model, but it is also inadequately handled in the Bsim3 model version [7] released in early 1993. This problem was brought up with the developers of the Bsim3 model, who indicated to these authors that they may correct it in future versions [8].

Benchmark Test 1: Weak Inversion Current

For a V_{DS} value in the saturation region, plot I_D versus V_{GS}, with I_D on a *logarithmic* scale and including V_{GS} values well below threshold. The shape should be as illustrated in Fig. 3(a). Most popular models will fail this test at least in the moderate inversion region, as shown for the Spice level 2 (or 3) model in Fig. 3(b). Due to the advent of low supply voltages, the moderate inversion region has become very important; e.g., op amp input stages often operate advantageously in this region. This is a distinct region of operation, with properties distinct from those of strong or weak inversion, and can extend over several tenths of 1 V; more details can be found in [4]. A MOSFET which does not exhibit the moderate inversion region has yet to be invented; thus, we should acknowledge the presence of this region as a fact of life and take it seriously. The moderate inversion region should not be considered just a "transition" region through which one can fit an approximate curve.

Benchmark Test 2: Transconductance-to-Current Ratio

Plot the transconductance-to-current ratio g_m/I_D (an important quantity for analog design) versus V_{GS} or versus $\log(I_D)$ (same ranges as for benchmark test 1). This is easy to do with simulators that allow numerical operations (e.g., with PSpice, one can get I_D versus V_{GS} and then ask for a plot of $(dI_D/dV_{GS}/I_D)$; otherwise, the test can be tedious but *will still be worth running*, at least for V_{GS} values around kinks such as the one in Fig. 3(b). Measurements give a shape as in Fig. 4(a).[1] Spice level 2 or 3 can give results as in Fig. 4(b). A large error occurs in the moderate inversion region. This problem is caused by the lack of properly modeling the moderate inversion current, and is of course accentuated by the derivative operation inherent in evaluating g_m. Errors of 100% in the value of the latter are not rare in this region. With lower power supply voltages, the seriousness of this problem increases.

Benchmark Test 3: Drain–Source Conductance

Plot g_{ds} $(= dI_D/dV_{DS}$ versus V_{DS} for a fixed V_{GS} value (or, better yet, obtain a family of such curves). The expected shape is as in Fig. 5(a), but some models (e.g., the Spice level 2 model) can give a result as in Fig. 5(b), depending on model parameter values. The reason is an unnatural transition from triode to saturation, shown in Fig. 5(c) (see also Section VI). Other models, such as level 3 or Bsim1 and 2, do not produce such an abrupt change, but *still* predict g_{ds} inaccurately in the transition from nonsaturation to saturation. Another problem present in some models involves the expression used internally for g_{ds}. If the values of g_{ds} as a small-signal parameter are requested for several V_{DS} values (e.g., by asking for an operating point analysis at each such value), and plots of g_{ds} versus V_{DS} are generated, a discontinuity or a sudden slope change can be observed at $V_{DS} = 0$. This is not in agreement with experiment, and contradicts the behavior of dI_D/dV_{DS} obtained by differentiation on I_D–V_{DS} data obtained using

[1] The quantity g_m/I_D peaks in weak inversion, but does not become exactly constant in it. This is due to minute deviations from exponential behavior for the current (too minute to be noticeable in plots like the one of Fig. 3(a)), which are predicted by detailed charge-sheet models [9], [4]. However, predicting a constant g_m/I_D in weak inversion would be acceptable for most purposes (except, of course, at such low current values that junction leakage becomes noticeable).

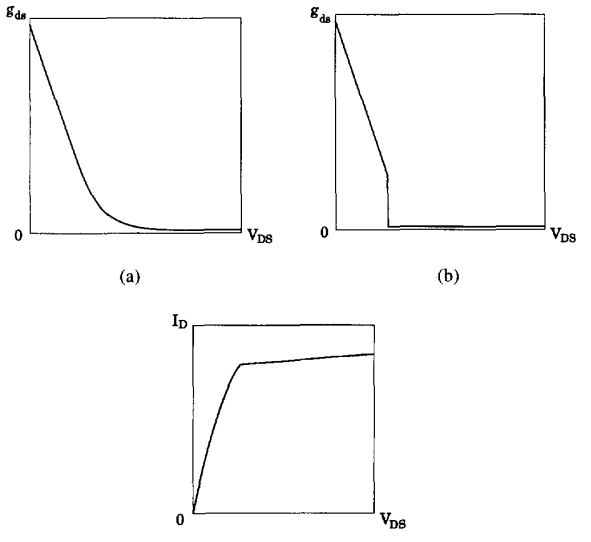

Fig. 5. (a) g_{ds} versus V_{DS} for fixed V_{GS} and V_{SB}; A qualitatively correct curve. (b) A corresponding plot using the level 2 Spice model. (c) I_D versus V_{DS} for fixed V_{GS} and V_{SB} using the level 2 Spice model.

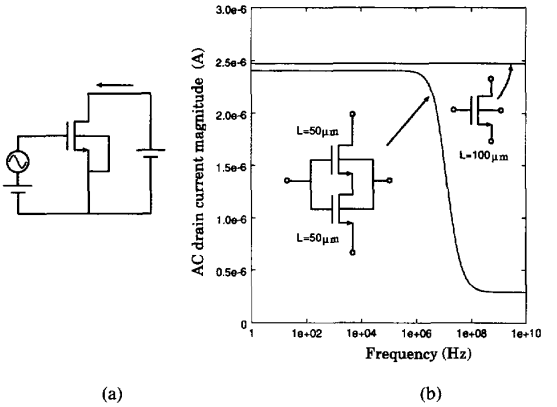

Fig. 6. (a) Circuit for obtaining ac response. (b) ac drain current magnitude versus frequency for a 100-μ m-long MOSFET and an equivalent combination of two 50-μm-long devices using the Spice level 2 model.

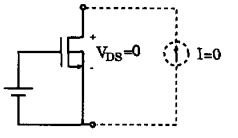

Fig. 7. Circuit for simulating thermal noise in triode region.

the same model, which show that nothing special should be happening at $V_{DS} = 0$.

Benchmark Test 4: High-Frequency Transadmittance

Take the simplest possible model (*remove* all parameters having to do with parasitics, such as junction and overlap capacitances, series resistors, etc.). In the device statement, do *not* specify source or drain areas and perimeters. We suggest the above simplifications to make clear what the following problem is due to. Bias a 100-μm-long MOSFET in strong inversion saturation, where the intrinsic gate-drain capacitance is zero. Use an ac source in series with the gate bias as shown in Fig. 6(a), and obtain a frequency response for the ac drain current magnitude. Now, break the device into two 50-μm-long devices, with their channels in series and with common gate and common substrate, and bias the combination as before. The combination should be equivalent to the single 100 μm device (remember, no junction area is supposed to exist at the intermediate point). Obtain the frequency response again. It should be the same as before. However, using any of the common Spice models, we get the behavior shown in Fig. 6(b). The behavior is totally different at high frequencies. This is the result of the fact that the models used are quasi-static; the behavior predicted for the 100 μm single device is, of course, totally unreasonable.[2] The two-device combination does a better job at approximating reality since it is a two-element lumped approximation to what is actually a distributed channel effect [4]. (In fact, such combinations (with two or more elements) can be used in lack of nonquasi-static models, for high-frequency small-signal work [4]; one should be careful, though, not to activate artificial short-channel effects in the subtransistors.) We note that nonquasi-static behavior has been experimentally demonstrated, even in short-channel devices [10].

Benchmark Test 5: Thermal Noise

Bias a device with a fixed V_{GS} in strong inversion and at $V_{DS} = 0$ (by placing a zero-value dc current source between drain and source, as shown in Fig. 7). Run a noise simulation for a frequency low enough so that the result is not affected by capacitances. Biased as indicated, the channel is equivalent to a resistor of value $R = 1/g_{ds}$, and should show a thermal noise voltage with power spectral density of $4kTR$ (e.g., 1.66×10^{-16} V^2/Hz for a g_{ds} of 10^{-4} A/V). The level 2, level 3, and Bsim models we tried give, depending on implementation, a value that is either a couple of orders of magnitude too low or is even identically zero. The consequences are obvious for the design of circuits using MOSFET's as resistors (most seriously, certain types of continuous-time filters and transconductors).

Benchmark Test 6: 1/f Noise

Bias a device in strong inversion saturation, and run a noise simulation at frequencies where $1/f$ noise should be dominant. The noise current can be converted to a voltage across a 1 Ω resistor, placed in series with the drain (or, even better, a "noiseless resistor" implemented using a self-dependent voltage-controlled current source). Now, increase the channel area ten times: does the power spectral density of the equivalent input noise voltage (in V^2/Hz) decrease 10 times, as observed in practice? Also, change V_{GS}; in

[2] In fact, the use of transcapacitors in some models can produce even worse errors, predicting that the ac current magnitude goes *up* with frequency. This is wrong, and contradicts both measurements and non-quasi-static models [4].

most devices, the equivalent input noise voltage should be insensitive to this change.

Most models in use will fail some or all of the above tests. And, of course, even if they pass some of them qualitatively, they still would have to pass them quantitatively, in comparison to measurements. Readers may want to take the results of the above tests to the model support team at their institution or their foundry.

IV. Other Problems

The above benchmark tests cover only some of the major problems which currently seem to be present in most popular CAD models. Other problem areas include capacitances and noise in the moderate inversion region; transient response under nonquasi-static conditions; the influence of the body effect along the channel on thermal noise; noise at frequencies where nonquasi-static effects are observed; effective mobility dependence on V_{SB}; etc. Most of these problems are discussed in [4], where extensive references to the literature are given. The problems mentioned as a rule get worse for devices with short and/or narrow channels, and for implanted (i.e., real!) devices. Also, particular models (and particular implementations of models in specific simulators) may have additional problems. For example, the Berkeley Spice 2G6 level 2 model can give C_{gd} values very different from C_{gs} for a symmetrical device biased in strong inversion symmetrically with $V_D = V_S$ if $V_{SB} \neq 0$. This problem does not appear in certain other implementations of the level 2 model. Many circuit designers have formed a list of problems particular to the models/simulators they use.

V. Parameter Extraction

Even if a model could, in principle, do a decent job over certain bias ranges, it often is not given the opportunity to do so due to poor parameter extraction. As an example, we took the parameters provided by a well-known foundry service for models level 2 and Bsim for the *same* fabrication process (obtained from measurements on the *same* devices). I_D–V_{DS} curves in strong inversion (where the parameters were apparently extracted) gave relatively good agreement of one model with the other. However, a plot of g_m/I_D using the two models gave the results in Fig. 8. The figure speaks for itself (note that no comparison of accuracy of the two models in weak inversion is implied here since the foundry simply did not attempt to match the models to data in that region). Other "results" using the same parameters from the same foundry: a six-order-of-magnitude difference in $1/f$ noise predictions between level 2 and Bsim, a factor of 3 discrepancy in the saturation g_{ds}, etc. Such problems are due to extraction having only the digital designer in mind.

Parameter extraction for general analog circuit design *must* include weak and moderate inversion, and it *must* include small-signal parameters, especially g_{ds}. Such parameters must be measured, and the error in predicting them must be included in the optimization criterion [4]. Ideally, capacitances and noise should also be included in the process. It is sad that, to this day, universities and sometimes even companies have

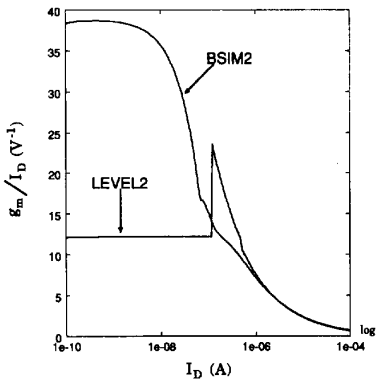

Fig. 8. g_m/I_D versus $\log(I_D)$ using the Spice level 2 and Bsim models with parameters as provided by a foundry service for the same fabrication process.

to design analog circuits using parameters obtained with the quality illustrated in Fig. 8.

Another issue with parameter extraction is the fact that it is often abused to make up for model deficiencies. For example, if a model equation predicts wrong drain current values when physically correct values are used for its parameters, the parameter extraction routine may assign totally artificial values to the latter, so that more accurate current values can be produced. This approach can be troublesome since the artificial parameter values used may cause very wrong predictions of other quantities, such as noise or capacitances, which were not considered during the parameter extraction process.

VI. Discussion

Experienced designers know about modeling problems, and they tend to design their circuits conservatively to avoid trouble. Novice designers or students, on the other hand, can be serious misled. For example, when designing op amps using the level 2 or 3 Spice models, they often discover that, as they increase the bias currents, the gain suddenly shoots up, say by a factor of 2. Sometimes they can even think they discovered a new phenomenon, and try to bias their circuit at that "magical" current value. Of course, the truth is that they just happened to hit the peak in Fig. 4(b), and that in reality, the extra gain is a mirage caused by poor modeling. [Imagine, by the way, what happens if they, in addition, happen to cross the kink in Fig. 5(b)!] Some people learn the truth the hard way when, after several months, their chips come back and they do not work.

Some of the problems discussed have a trivial cure. Their cause may simply be that somebody goofed and used the wrong formula. For example, the saturation thermal noise formula has been mistakenly used also for the triode region in most Spice models, causing the problem revealed by benchmark test 5 above. Such problems can be corrected by opening the code and replacing the wrong formula with the correct one. Other problems can be corrected by "twisting" the parameter extraction process; we have been told, for example, that in this way, one can eliminate the slope discontinuity in Fig. 5(c) (see, however, Section V). For other problems, the cure is not so simple; to avoid them, what is needed is a model developed from scratch, by teams who truly understand

device operation *and* appreciate the analog designer's needs at the same time. Here, in fact, lies one of the root causes of the problems with modeling: such teams are very hard to come by. The physicists, who could in principle develop a good model, usually attack "esoteric" problems of interest to them, and are not interested in putting together an entire model which correctly incorporates "mundane" effects. The circuit designers know what is needed, but lack the necessary physics background. With a lack of people who understand both areas, a solution might be to form an interdisciplinary team, consisting of device physicists and an analog circuit designer.

Another difficulty is the entrenchment of established approaches and routines. Suppose a good model, with none of the problems discussed above, were developed. It would be a very difficult job to try and get it accepted by the community. It would have to be implemented correctly in several versions of Spice, appropriate parameter extraction systems would have to be developed, the foundries would have to be convinced to provide parameters for the new model, etc.

All of these difficulties, however, would have been surmounted if the community planned a little longer term. Unfortunately, many companies "cannot afford" to increase their modeling effort since the latter will not pay off in the next quarter. Has anybody calculated, though, how much such companies have lost in revenues over the years because their chips did not work the first time due to erroneous modeling during design? Or because the chips had to be designed conservatively to bypass modeling difficulties, and thus did not achieve the performance the actual devices are capable of?

Of course, not everything is bleak. Several models which address at least some of the issues discussed here have recently been described (see, for example, [4]–[7], [11]–[13]). Promising work is also being conducted at EPFL and CSEM in Switzerland [14]–[16] by a team which includes analog designers. Rather than starting from modeling I–V characteristics and then differentiating to obtain small-signal parameters (with all the ensuing problems discussed above), they start by carefully modeling the small-signal parameters and then obtain the I–V characteristics by integration [17]. Single expressions valid in all regions of operation, including moderate inversion, are used. Thus, several of the problems that plague popular models are eliminated. The model is still under development, but a first version of it can be found in popular commercial simulators. Small-signal parameters have also been used as a start in a recently described table lookup model [18] which economizes on the large storage requirements associated with such models [19]. It is not possible for us, though, to judge the recent work mentioned in this paragraph. To really judge a model, one must "live with it" for some time, and we have not had a chance to do so for the above models.

The authors invite correspondence from model users as to the difficulties they are facing. Any report on a modeling problem, bug, inconvenience, etc. (giving specifics of the model and simulator used), as well as any ideas for improvement would be welcome. Respondents should specify whether their feedback can be reported in the open literature, and whether they object to being quoted.

VII. Conclusion

The MOSFET models available for analog work suffer from serious problems. Analog circuit designers have been complaining about this situation for a long time, but to deaf ears. For example, many of the problems discussed had been identified in an IEDM paper over ten years ago, and published in a journal [20], with cures suggested there and in a book [4]. Yet, even problems trivial to correct (e.g., noise in the triode region) have not been corrected in popular simulators. Fortunately, though, there is now cause for optimism. We have finally entered the era of mixed analog–digital chips in which, if the analog part is in trouble, the performance of the chip as a whole will suffer. Thus, the fates of analog and digital circuits have finally been connected. This presents a golden opportunity for the analog circuit designers to voice their complaints, and be heard this time.

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