1. Rules for the execution of the projects

- Projects are optional. Their aim is to improve the students' knowledge of the basic full-custom design flow. The final score of the exam is not affected by the choice of carrying out a project.
- Projects can be carried out by groups of up to 5 students. Project can be assigned to single student. The complexity of the project increases with the number of students of the group.
- Projects can be assigned in any period of the year.
- Verification of the projects consists of two phases: (1) the student are received by the teacher once they have finished the schematic design flow and performed the required simulation. If the result is satisfactory, the teacher authorizes them to complete the design with the layout drawing. (2) Once the layout is completed and the verification steps (DRC, LVS) are passed, the students send a short report to the teacher by e-mail (pdf format).
- The report should include:
  -) A brief description of the task and of the criteria used for the design (two pages max).
  -) A snapshot of the schematic view, taken from LTSpice schematic editor;
  -) All the required simulation results (plots) in graphical format;
  -) A snapshot of the layout
  -) A copy of the lvs report;
- All figures in the report should be provided of a small caption, indicating the content of the figure.

2. Brief introduction to the CAD environment.

2.1 Schematic view design: LTSpice.

2.1.1 Starting a new design.

The schematic project should be saved into a directory (schematic home directory), which will be called from here on sch-home. The sch-home should mandatorily include the following files:

PSM025.mos
N_PSM025.asy
P_PSM025.asy

To start a new schematic view, launch LTSpice from the corresponding icon in the Windows start-menu and choose file->new schematic. After that, before introducing any component, save the file into the sch-home directory. In this way, all the components included into the sch-home dir will be accessible.

2.1.2. Component libraries.

The components that can be instantiated into the schematic are divided into two cathegories:

(a) Process components.

(b) Standard Spice components

Process components are the only ones that can be used to design the cell and the only ones that can be placed into the layout. They are present into the sch-home dir. The Standard components are necessary to test the cell (provide power supply, bias currents, input signals and possible loads).

They are placed in a fixed LTSpice directory and are accessed through the dialog windows that opens when a new component is inlcuded into the schematic view. To introduce components (instance operation), choose: edit->component (shortcut F2).
The following dialog windows pops up:

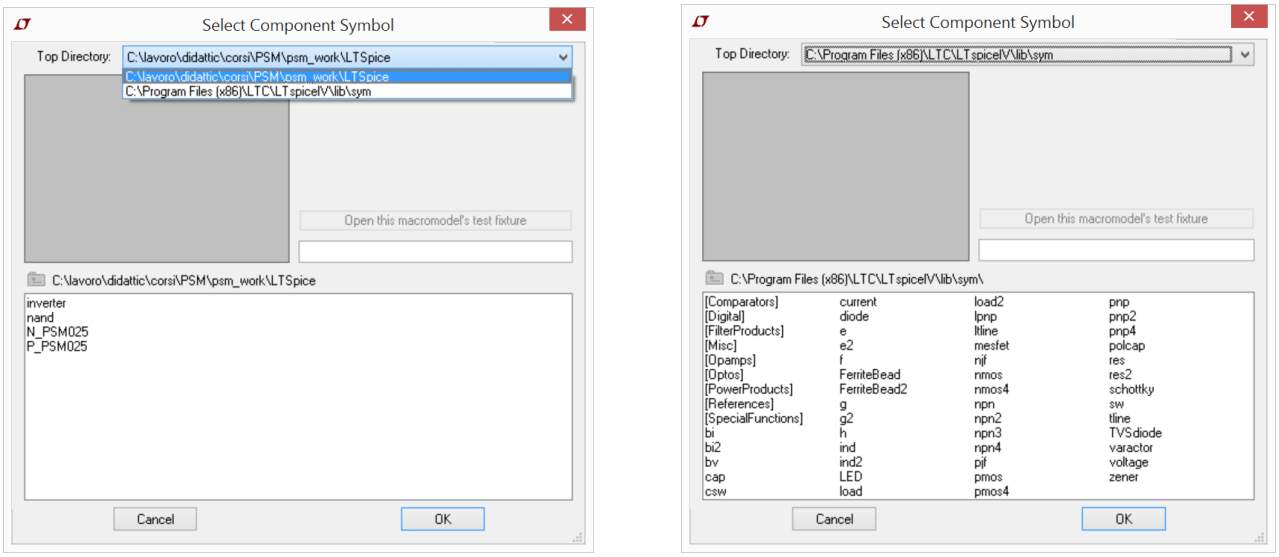

Fig. 1. Dialog windows for component instance in the case of process components (local sch-home dir) and Standard components (LTSpice library). Library selection is operated through the "Top Directory" field.

The components available in the PSM025 process are:

Component name	Description
N_PSM025	n-channel MOSFET
P_PSM025	p-channel MOSFET

Tab. 1. Process components.

Although integrated mosfets are symmetrical, it is important to remember that the source and drain are distinguished in the device symbols, according to the rule shown in next figure:

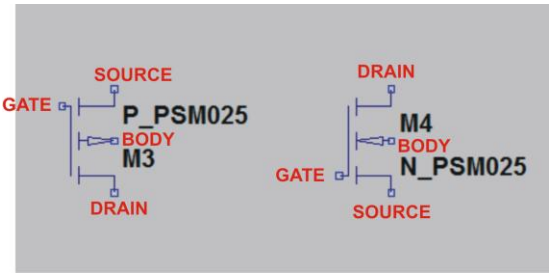

Fig. 2 Mosfet symbols, showing the convention used for the terminals.

If the drain and source terminals are swapped, the circuit behavior and the simulation results do not change. Unfortunately, when the simulator shows the mosfet voltages (Vgs, Vds etc) in an operating point analysis, it follows the rule of fig.2. Thus, be sure to place the mosfets correctly with the source and drain in the right positions.

The standard components that can be used in the project, are:

Component name	Description
voltage	Independent Voltage Source
current	Independent Current Source
e	Voltage Dependent Voltage Source
res	Resistor
cap	Capacitor

Tab. 2. Allowed standard spice components to be used for providing power supply, bias, stimuli and load to the cells.

All other standard spice components should be avoided.

Mosfets (process components) have to be properly sized, assigning the length (L) and width (W). To do so, right-click on the component and the following dialog window will pop-up.

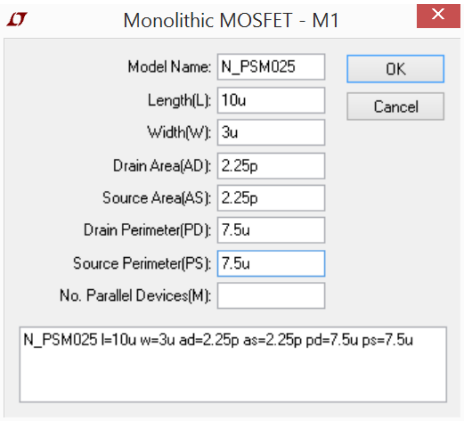

Fig. 3. Example of mosfet parameter dialog window with filled fields.

For static simulations (OP, DC sweep), set only the length and width. In this way, parasitic capacitors are not set, but the simulation is not affected (in dc analysis, capacitors are open circuits). For transient and AC simulations, fill the area and perimeter fields with the following rule:

$$AD = AS = W \cdot L_C$$

$$PD = PS = 2W + 2L_C$$

where L_C is the minimum drain/source diffusion length allowing placements of metal/diffusion contacts. Considering the educational PSM025 design rules, L_C=0.75 μm. If W and L are expressed in micron (using the suffix "u" for the 10^{-6} multiplier), perimeters are in μm (suffix "u") and areas in μm^2 (suffix "p").

2.1.3 Frequent command for network creation

Most LTSpice commands can be accessed by the upper toolbar. Passing with the mouse over an icon, cause a simple explanation text message to be displayed.

Zooming in and out is obtained by the mouse wheel.

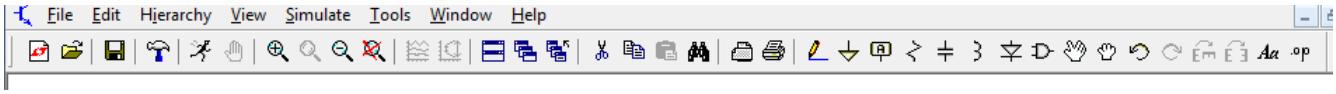

Fig. 4. Upper toolbar.

Frequent command and their keyboard shortcuts are the following:

Component (F2): used to insert components (creating an instance for each one), see previous paragraph for a detailed description.

Wire (F3) : enter the wire drawing mode, used to make connections with the components nodes. To connect two nodes: (i) select the wire command (ii) go over the first node with the mouse, (iii) left click with the mouse, (iv) drag the mouse without holding down any key, (v) left click to introduce vertices, (vi) reach the second node to be connected.

Label net (F4): opens the following dialog window that allows creation of labels and terminals.

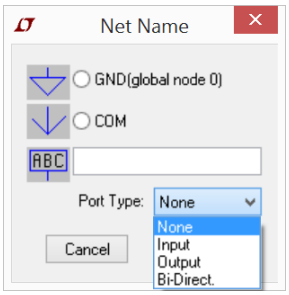

Fig. 5. Label/terminal pop-up window.

A pure label can be used to assign a name to a node, to easily recognize it. Labels can be used to connect two nodes without drawing a wire across them. To insert a simple label, choose a port type “none” and give a name to the label in the field identified by “ABC” (see Fig.5).
Terminals (pins) allow connection of cell to other cells, when it is instantiated into another schematic view, at a higher hierarchical level. When inserting a pin, choose the most appropriate type among Input, Output and BiDiderct. If not sure, choose BiDirect.
The same command can be used to introduce global nodes. Be sure to insert at least one GND symbol in your design. Gnd can be placed with the Label command or with its dedicated command in the upper toolbar.

Delete (F5) Enter the “delete” mode. Every component selected in this mode is deleted.
Duplicate (F6) every component selected (left mouse click) is duplicated.
Move (F7) every component selected (left mouse click) is moved.
Drag (F8) similar to “move” but the component is moved without interrupting the connections.

To move, drag, duplicate or delete a component, execute the following steps:

(a) start by selecting the command corresponding to the desired operation;

(b) select the component (or components) to which the command has to be applied. To select a single component, go over it with the mouse and then left click. To select a part of the circuit, drag the mouse across the area to be selected while holding down the left button (as in typical graphical program).

Important: once a command has been selected, it remains active until the key "esc" is pressed.

2.1.4 Component rotation and mirroring.

LTSpice uses a particular convention: components can be rotated and mirrored only after that they are "activated" by selecting the "move" or "drag" command. To rotate or mirroring a component, press F7 (to move) or F8 (to drag), select the component as for a simple move, then press:

Ctrl-r for rotation (by 90° steps)
Ctrl-e for mirroring (along the horizontal direction).

2.1.5 Symbol creation

In order to use the cell that is being created as a building block for more complex circuits, it is necessary to create a symbol view, by which the cell is instantiated into higher hierarchical levels and connected to other blocks. To create a symbol it is necessary to perform the following steps:

(a) Place terminals (input, output, bidirect) in the schematic view, for any node that should be accessible by other blocks. Use a bidirect for the Vdd, while GND does not need to be connected to a terminal since it is a global net by default.
(b) Open the symbol sheet by the menu command: Hierarchy->Open this Sheet's Symbol

The following window pops up:

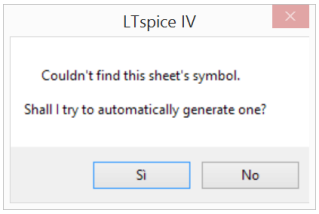

Fig. 6. Automatic symbol creation pop-up window.

Press yes to command the creation of a symbol, that is automatically linked to the schematic view. The default shape of the symbol is a box with all the terminals that were defined in the schematic view placed on the box perimeter. It is possible to change the terminal position, and/or the symbol appearance. To draw geometrical figures (with decorative purpose only) use the items of the "Draw" menu entry.

Save the symbol in the sch-home directory, so that it is accessible in the process library.

2.1.6 Simulation

To simulate the cell, voltage and current sources have to be added to provide power and biasing to the circuit. It is a good practice to separate these elements that, obviously, cannot be integrated, from the real process components. To do that:

(a) introduce terminals to the cell being created, using terminals also for the bias and power supply nodes
(b) introduce a “spice directive” (Edit->Spice directive) into the cell, with the following content:
.lib PSM025.mos
This is required to indicate where the simulator should search for the models of the two process devices indicated in table 1.
(c) create a symbol following the instruction above;
(d) create a new cell (File->New Schematic) to be used as a work-bench;
(e) Instantiate (F2) the cell to be tested into the workbench and add the required power/bias sources and input signals, connecting them to the cell terminals.

At this point, set all required values to the bias/stimuli, power supply sources and launch the simulation from the work-bench. Simulation type has to be specified with the Simulate->Edit Simulation Cmd command.
This command opens a dialog window where the analysis type and parameters can be specified. Once the “OK” key is pressed, the corresponding textual spice command is created and can be placed in a convenient area of the schematic view (any free area where components or other Spice directive are not present).

Before launching the simulation, be sure that the program is instructed to save all currents and voltages at any hierarchical level. This has to be set using the control panel (Tools->control panel) window as indicated in the following figure:

Fig. 7. Control panel setting for saving both currents and voltages at any hierarchical level

Launch the simulation by Simulation->Run.
If a simulation that involves creation of a plot has been selected (for example DC sweep), a graphical plot windows opens. To add traces go back to the circuit windows and go with the mouse over the nodes which carry the signals to be plotted. The mouse pointer changes into an oscilloscope probe symbol. left click to add the signal into the simulation output window. To specify a current, place the mouse pointer on the terminal (of a subcircuit or other component) which carries the current to be plotted. The mouse pointer changes into the picture of a current probe. See the following figures, showing the mouse symbol in the two cases:

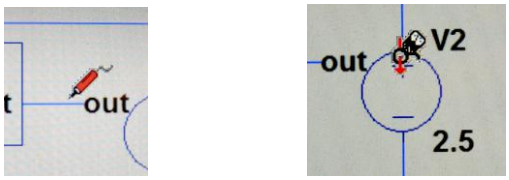

Fig. 8. Mouse symbol for voltage probing (left) and current probing (right)

Traces can be selected also from the simulation output window by Plot Settings->Visible Traces. This is correct method to add expressions (i.e. voltage differences).

In the case of operating point simulations, a textual window with the circuit and subcircuit node voltages and currents is displayed. Once that window is closed, it is still possible to read the operating point solution (node voltages and terminal currents) by going over the selected node or terminal: the operating point value is displayed in the bottom of the schematic window. To use the same procedure for the subcircuit values, simply open the subcircuit schematic view (from the menu entry "File", or simply right clicking on the subcircuit symbol in the workbench.

To show the operating point data of all circuit and subcircuit devices, open the so called "Spice Error Log" by the menu entry View->Spice Error Log. Note that the V_{GS} and V_{DS} are reffered to the terminals according to the convention in fig.2. The VDSAT can be used as an approximation of the overdrive voltage V_{GS}-V_T in normal operating conditions (saturation and strong inversion).

2.1.6 Netlist extraction

When the simulation results are satisfactory, it is necessary to save the netlist for comparison with the neltlist that will be extracted from the layout. This can be obtained by the following steps:

1) Open the schematic view of the cell to be designed.
2) Right click and select view->Spice netlist
3) Once the spice netlist is open, right-click over it and choose "Edit as independent netlist".

For a simple example of a project, see the inverter circuit included in the design kit. The combination of all windows is shown in next figure.

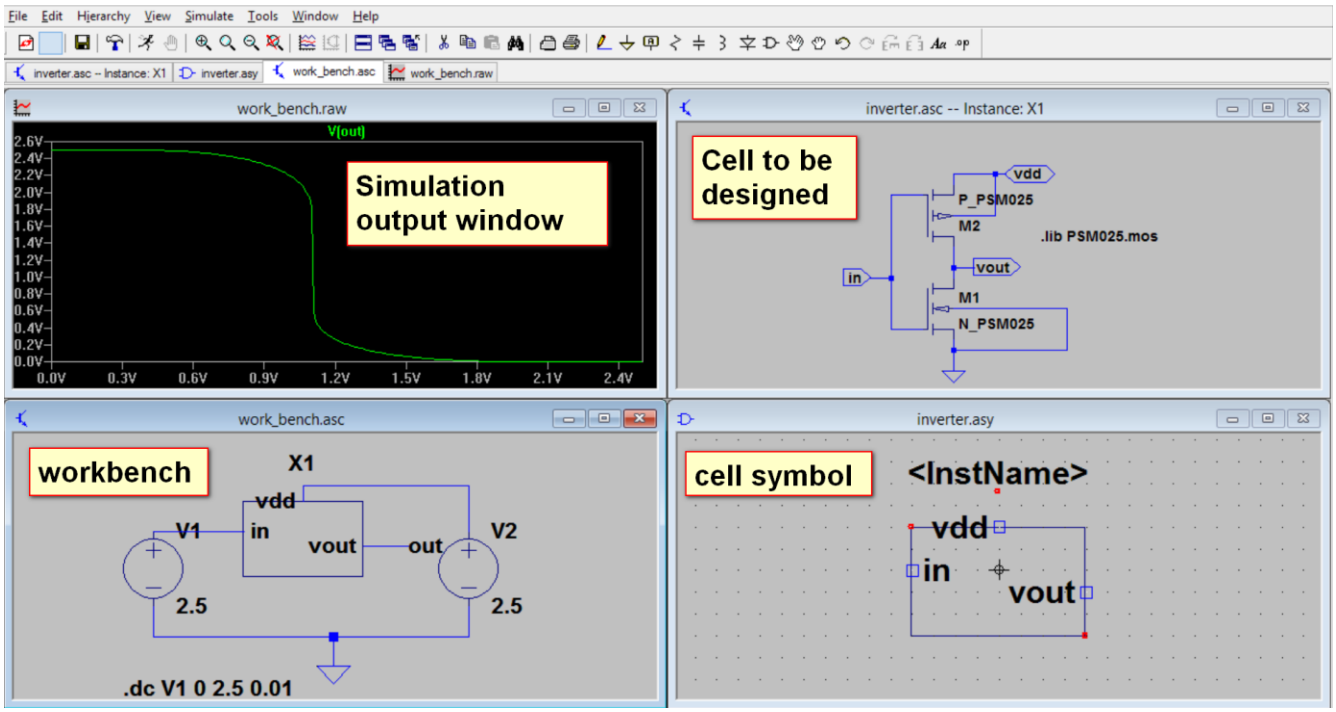

Fig. 9. Elements of the schematic project

2.2 Layout design and verification: Glade

We will refer to the layout home directory with "lay-home". The lay-home should include the following files:

layout.bat	Batch file used to launch glade
PSM025.tch	The technology file (layer definitions, via definitions, layer colors)
drc.py	The design rule file.
extract.py	The extraction rule file.
N_PSM025.py	Parametric *n*-mos extraction cell (for extraction purposes)
P_PSM025.py	Parametric *p*-mos extraction cell (for extraction purposes)

2.2.1 Operations to execute at the first access to the program

1) Follow the installation instructions for modifying the layout.bat file in order to set the correct program path.
2) Launch layout.bat
3) When glade opens, open the menu entry "Tools" and activate: "LSW", "Library Browser", "Message windows", if they are not yet selected.
4) Create the project library: File->new Lib

Set the library technology by importing the technology file:
File->Import->Import Techfile or simply press Ctrl-L.

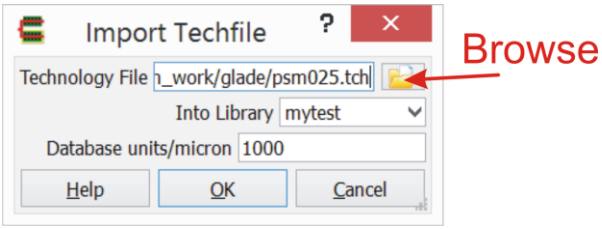

Fig.10 Dialog window for techfile import

Choose the PSM025.tch tech-file included into the lay-home dir, by using the browse button of the window. file; be sure that the "Into Library" indicates the new library.

5) Create the project cell with: File->New cell (specify the project library and give a name to the cell. Check that the view is layout. The layout editing window should open.
6) Save the library in the lay-home directory: File->Save lib. Use the browser tool to select the lay-home dir. The program automatically create a new dir with the name of the saved library into the lay-home.
7) Open the Display options window (Edit->Display Option). The settings in all four tabs of the window are shown below.

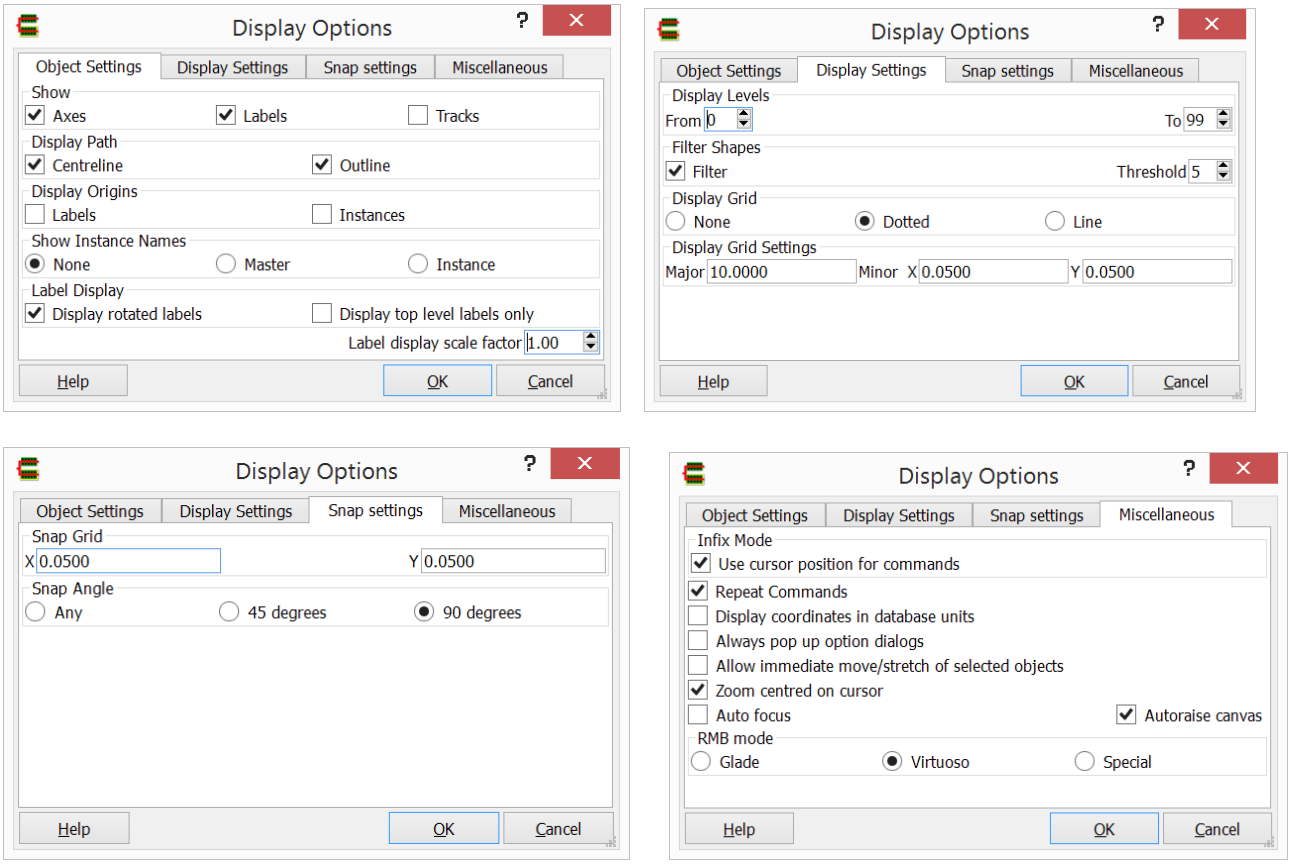

Fig.11 Dialog window for techfile import

It is mandatory that the Display Grid Settings and the Snap Grid are set to the value indicated in the figure, In particular.
Display grid: major=10, minor x and y 0.05. This means that the major grid points are separated by 0.5 microns, while the minor grid (visible only when zooming in) by 0.05 microns.
Snap grid x and y: 0.05 microns
Other important settings: deselect “always pop up option dialogs” and select “zoom center on cursor”.
When these options are set, they are remembered at any new session and do not need to be set again.
For any further access to the program, it will be simply necessary to open the saved library by File->Open Lib and then open the cell from the library browser.

2.2.2 Drawing commands

Drawing a layout means introducing geometrical shapes into the layout editor. The basic shapes that should be used in the project are rectangles and paths. Paths help creating connections. Before creating a shape it is necessary to choose the layer (technological layer) in the LSW panel on the right. The LSW main elements and operations are shown in next picture:

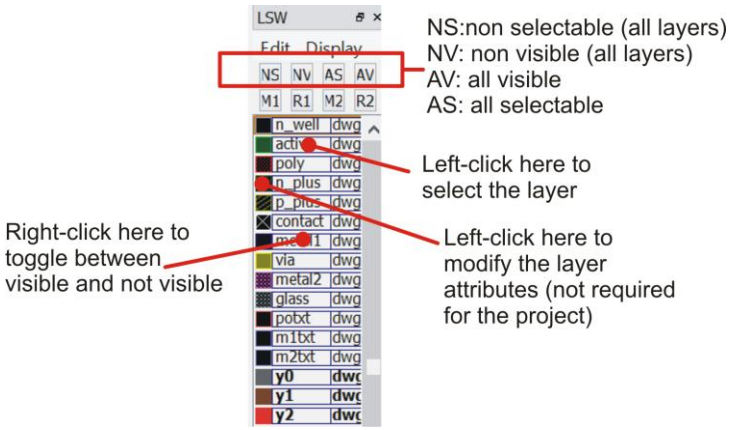

Fig.12 LSW elements and operations

Rectangle and path creation can be commanded from the upper toolbar as shown in the following figure. In order to precisely set the rectangle dimensions (for example when they are active or poly layers that sets the mosfet width or length, respectively), rulers are available.

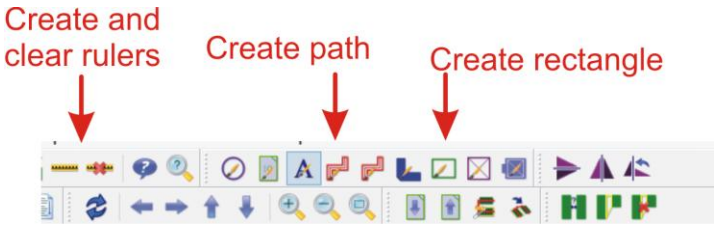

Fig.12 Upper toolbar elements

To create a rectangle, chose the rectangle tool, then left-click on the first and then on second vertex of the rectangle. To create a path, choose the path command, then left-click on the path starting point and drag the mouse (without holding any button) to the final point. Path vertices are

introduced by left-clicks. The final point (end of the path) is indicated by a double-click. The path width is set by clicking the F3 key after starting the path.

2.2.3 Vias and contacts

To introduce a contact or a via, press “v” The following dialog window opens:

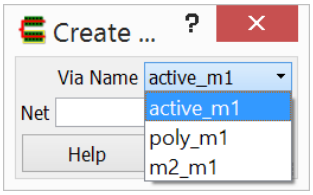

Fig.13 Upper toolbar elements

It is possible to choose within all the possible combinations available in the PSM025 process. The command place a square via or a contact included into squares of the two layers that have to be connected. The square size is the minimum required by the minimum overlap rule.

2.2.4 Selection modes

There are two possible selection modes in glade: full and partial. By full selection, objects are completely selected. For example selecting a rectangle in full mode selects the whole rectangle. In partial mode it is possible to select only a part of the rectangle, for example one single side. To switch between full and partial mode press the F4 key.
Dragging the mouse over a series of objects by keeping the left-key pressed, selects all objects included into the area being defined in this way. Selection is partial or total depending on the chosen selection mode.

2.2.5 Basic editing

Shapes can be modified by moving, copying or stretching them. To **move** a shape or a series of shapes, select them and press “m”. Then move the mouse (with no key pressed) and see the object(s) being moved. Press F3 to choose the way the move is applied and the following window opens:

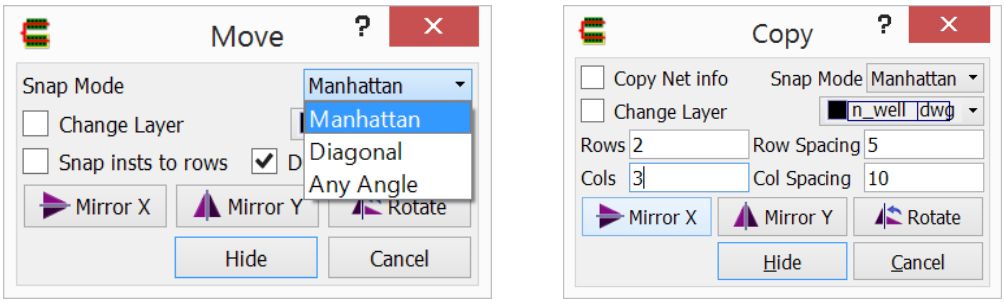

Fig.13 Dialog windows that open during a move or copy command by pressing the F3 key.

The snap mode controls which directions are possible. “Manhattan” force the shape to be moved only along perpendicular directions starting from the initial position. “Anyangle” allows all

directions. The “Manhattan” mode is very useful to guarantee that an object is moved only horizontally or vertically.
Proper buttons also allow rotating or mirroring the shapes while they are moved.

The **copy** command is used to make copies of a selected object. To copy an object, first select it then press “c”. Move the mouse to indicate where the copy should be places. Press F3 to change the possible directions as in the move operation, rotate or mirror the copy or make multiple copies organized in arrays of N rows and M columns. See the dialog windows that opens by the pressing the F3 key during a copy command in Fig. 13.
The **stretch** command require that a rectangle side or path end have been selected in partial select mode (see the select paragraph). After that, press “s” and move the mouse. The side or path end moves, modifying the object. This can be used to trim the dimensions of a rectangle or the length of a path. A dialog window that sets the way the stretch is applied can be opened pressing F3.
To select a rectangle side, enter partial selection mode and then click on the chosen side. to select a path end, enter partial selection mode and click on the path end (end of the line visible inside a path).

Another important command is the “**property**” command. It is called by the “q” shortcut. This command should be invoked after having selected an object (for example a rectangle). A pop-up window is opened showing many parameters of the object. In the case of a rectangle the width and length is shown, alongside other characteristics. Using the property command it is possible to trim the dimensions or position of an object in a precise way.

2.2.6 Labelling nodes

This step is useful for the extraction phase. All shapes corresponding to interconnect layers can be labelled so that the extraction will assign the chose name to the extracted node. Only shapes in polysilicon, metal1 and metal2 can be labelled. To do this, choose a proper layer as in indicated in the following table:

Technological layer of the shape to be labelled	Label layer
Poly	potxt
Metal1	m1txt
Metal2	m2txt

Tab. 3. Correspondence between the technology layers and the label layers.

After that, select the command Create->create label from the menu (or press “t”) and write the chosen net name in the pop-up window. Then drag the label to the chosen shape, paying attention to place the small dot over the text (the “label contact point”) on the shape.

2.2.7 Design Rule Checking (DRC).

DRC is executed by the menu entry:

Verify->DRC->Run.

In the pop-up window, browse for the rule definition file “drc.py”. For successive DRC run, the DRC rule file remain stored and there is no more need to specify it. See the message window at the

bottom of the glade workspace to see if errors are present. If there has been errors, they are indicated in the layout with white lines (error marks). To visualize the errors in sequence and get an explanation, open:

Verify->DRC->View Errors

Clicking on each line in the pop-up windows zooms to the error in the layout editor.

2.2.8 Netlist extraction (DRC).

Electrical circuit extraction from the layout is executed by the menù command:

Verify->Extract->Run

In the pop-up window, browse for the file "extract.py". This operation should not repeated in successive extract runs.

The result of the extraction is the creation of another cell view, called "extracted". This cell is a representation of the layout where connectivity and devices are recognized.
The Spice netlist can be saved from the extracted view by the command:

File->Export->Export CDL

Nevertheless, this operation is not explicitly required for the LVS operation, described in next paragraph

2.2.9 Layout versus Schematic (LVS) verification.

To perform an LVS check, you need to have previously extracted the schematic neltilst from the LTSpice cell (see paragraph 2.1.6).
Then, in glade, open the extracted view of the layout cell and execute the command:

Verify->LVS->Run

In the pop-up window, browse to choose the schematic netlist (the layout netlist, represented by the extracted view, is automatically selected).
In the "Gemini options" section, set the following items:

-) Do not collapse fingered transistors
-) Do not collapse transistor chains
-) Set Transistor L/W tolerance: 0 % (to enable parametric verification)
-) Verbose mode

The result of the verification is shown in the message window. The textual output of the LVS check produces a sentence like:

n devices and m nets written to <work directory><cell>.err file.

The number" n" indicates how many devices (mosfets) does not match between the two netlists, while "m" refer to unmatched nodes (nets). The LVS check can be considered passed if n=m=0.
Due to a bug, the detailed result of the LVS comparison is not shown in the error file <cell>.err but it is appended at the end of the glade log file, This file is created when glade is started and its name is like: glade_13.05.2014_08.09.26.log where the numbers are actually updated with the current

date and time. Copy that file into another_one and open it with a text editor. It includes a log of all operations performed from the last glade start. In the final part it includes the LVS report (if it is the last operation before the file has been copied). It is necessary to copy the file since it may be impossible to open it while it is still owned by the glade program. Furthermore, this file is cancelled and restarted at any new run of glade (as set by the layout.bat launch file).
An example of LVS check result, showing two mismatch errors is shown below

```
Graph "C:\lavoro\didattic\corsi\PSM\psm_work\glade\inverter_extracted.cdl":  Number of devices: 2
    Number of nets: 4

Graph "C:\lavoro\didattic\corsi\PSM\psm_work\LTSpice\inverter.cir":   Number of devices: 2
    Number of nets: 4


The following transistors do not match in size:
   sm_work\glade\inverter_extracted.cdl : si\PSM\psm_work\LTSpice\inverter.cir
(1) Device type p:
s,d:              out               vdd :               vout                vdd
g:                 in  l/w: 0.310/1.000 :                 in  l/w: 10.000/10.000
(2) Device type n:
s,d:              out               gnd :               vout                  0
g:                 in  l/w: 0.310/1.000 :                 in  l/w: 10.000/3.000

2 (33%) matches were found by local matching
All nodes were matched in 2 passes

2 devices and 0 nets written to C:\lavoro\didattic\corsi\PSM\psm_work\glade\inverter.err
# INFO: LVS finished with exit code 0
# INFO: LVS completed.
Note: LVS writes the error report into the glade .log file.
```

Once all errors have been corrected, use a text editor to separate the LVS report from the other part of the log file and save it to include it into the final project document.
Errors are also marked in the layout in the same way as the DRC errors. They can be listed and viewed also opening the Verify->DRC->View Errors command.