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E C P D 10

Dual Layer Metal 1.0 Micron Design Rules

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E S 2 - M T D

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1. Title

Dual Layer Metal 1.0 um Logic CMOS Design Rules (ECPD10) .

2. Index

3.0 Introduction

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This Dual layer metal, 1.0 um, N-Well CMOS technology is designed for high speed, low voltage (5V), custom logic circuits. It is to be processed according to the flow DM07. This process is the second generation of ES2 1.0 um processes.

The circuits designed with the following rules can be processed in a state-of-the-art wafer fab. facility. Advanced wafer steppers or E-beam Direct Writing Systems and Dry Etchers must be used for all lithography steps.

The Design Rules ECPD10, as well as the electrical parameters are compatible with the C200DM Design Rules of PHILIPS.

4.0. General Rules

4.1 All dimensions in this package are expressed in microns, except if specifically indicated.

4.2 All dimensions indicated are absolute minima. It is strongly recommended, whenever possible, to use larger values, except for contacts and vias which must be drawn at nominal values. No width or spacing on any layer are allowed below 1.0 micron.

4.3 Notches are to be considered as spacings and must respect the same minimum values.

4.4 The design rules are formulated in final dimensions as measured on the silicon wafer.

The dimensions involving the active region refer to the edge of the thin oxide region, at the bottom of the bird's beak.

The dimensions involving the implant layers (Well, N+, and P+ implants, threshold voltage adjustement) refer to the resist edge after development.

A skew is applied to the database prior to mask making or direct writing so that the geometries drawn by the designer will be reproduced exactly on the wafer (see section 13.0).

4.5 Non orthogonal, including fourty-five degree, lines are prohibited. If fourty-five degree lines cannot be avoided in a particular layout, contact your design center for further analysis.

4.6 Special values are given for corner rules to account for the fact that sizing has an increased effect on corners. For the sake of generality, corner rules are defined by (1) a worst case sizing value and (2) the minimum dimension to be met after sizing.

4.7 The design rules fit to the registration accuracy of 5X stepper or better. The same design rules are valid if E-Beam lithography is used. Either lithography can be used to process ECPD10 circuits.

4.8 The scribe line structure and design rules are described in section 14.0.

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4.9 The database must be digitized on a 0.125 micron grid.

This means that all verticles of polygons shall have x and y coordinates which are integer multiples of the grid size.
Elements such as paths or boxes shall therefore have a width and/or a height equal to an even multiple of the grid size.

4.10 Metal stress rules.

Temperature cycling behaviour, particularly aluminum shift, depends on absolute distances. It occurs principally at the periphery of large chips.
For large designs which are to be produced in large quantities, it is necessary to contact ES2-MTD about this subject.

4.11 **This process is intended for pure logic applications and only digital devices are guaranteed. The usage of any other/special devices (resistors, capacitors, analog structures, ...) requires prior checking with MTD.**

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5.0 Layer Symbols.

Mask N°	TITLE	LAYOUT SYMBOL
10	N-Well Implant	
20	Active Area	
	All	
	N+	
	P+	
50	Polysilicon	
60	N+ Source/Drain Implant	
65	P+ Source/Drain Implant	
70	Contacts	
80	Metal1	
75	Vias	
85	Metal2	
90	Passivation	

6. Topological Design Rules

The following conventions are used for the definition of the layout rules.
Layer B is defined after layer A in the process flow.
All dimensions are always either absolute minima, or values to be met exactly

6.1 Width : Minimum distance between inside edges of a figure.

6.2 Space : Minimum distance between outside edges of two figures, belonging to the same or to different layers, in order to prevent interaction.

6.3 Coincidence : Minimum distance common to two figures, in layer A and layer B respectively.

6.4 Overlap : Minimum distance that figure in layer B has to extend outside figure in layer A.

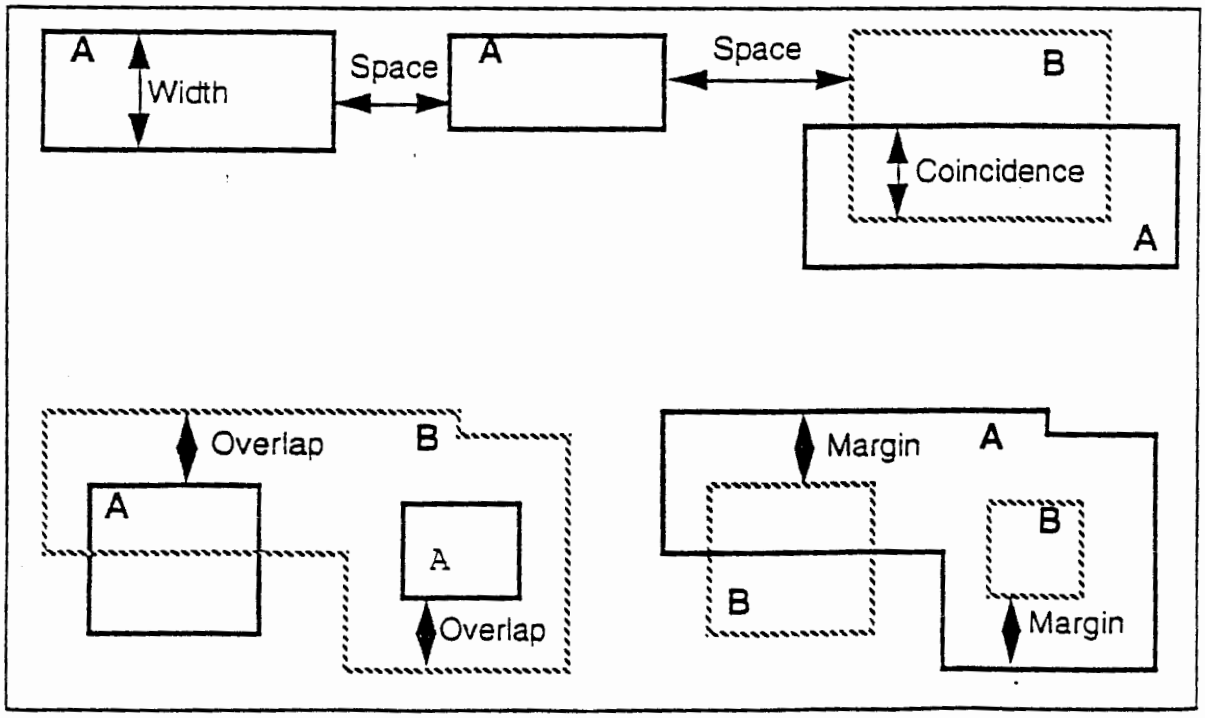
6.5 Margin : Minimum distance that figure in layer B has to be within figure in layer A.

6.6 Hot Diffusion : All N+ diffusion regions outside the N-Well which have a potential not equal to the substrate voltage ; All P+ diffusion regions inside the N-Well which have a potential not equal to the N-Well potential.

6.7 Cold diffusion : outside the N-Well a diffusion which has the same potential as the substrate. Inside the N-Well a diffusion which has the same potential as the N-Well.

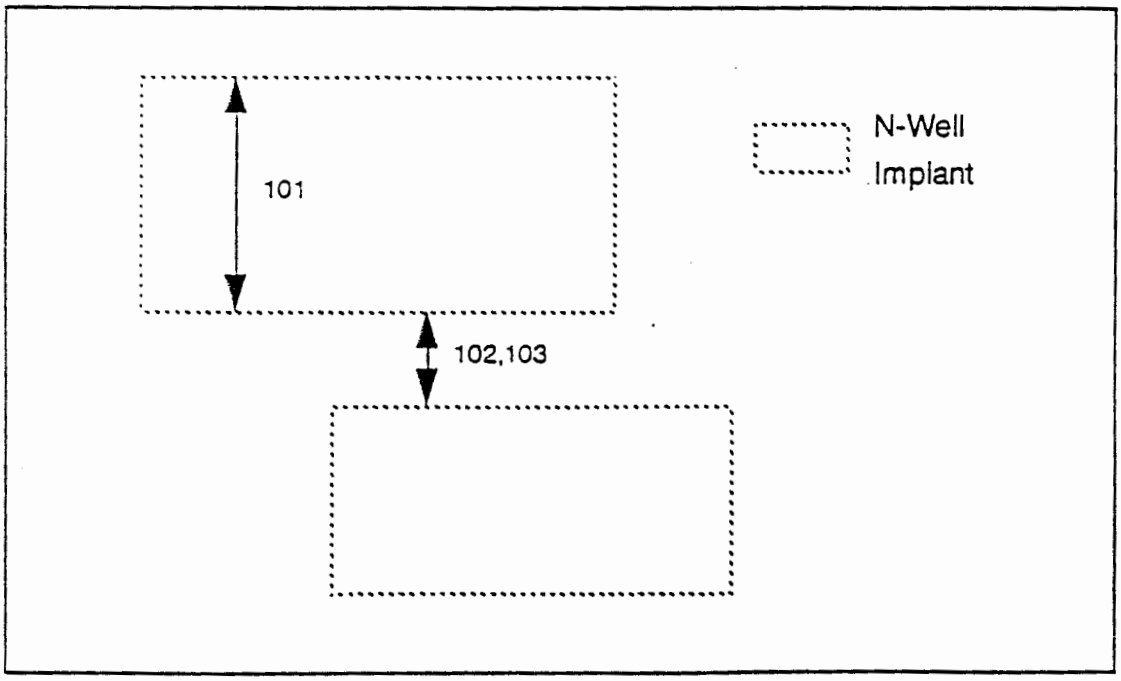
6.8 Hot N-Well : N-Well not connected to the most positive voltage (VDD).

6.9 Cold N-Well : N-Well connected to the most positive voltage (VDD).



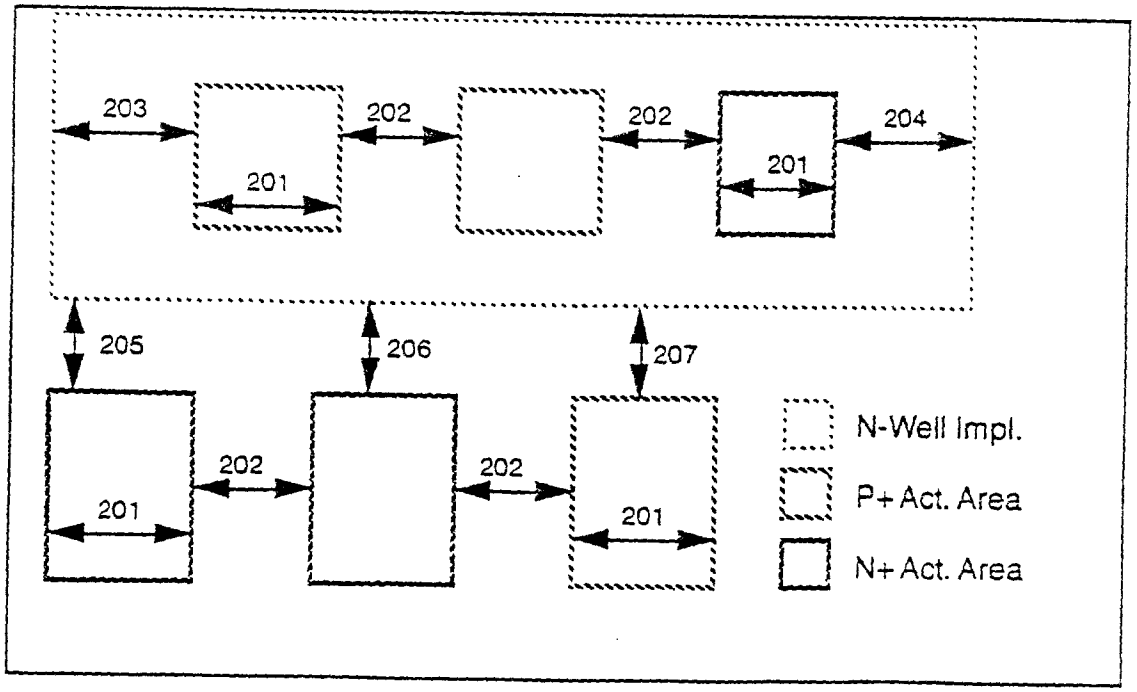
Layer 10 - N-Well Implant

Rule Nb	Parameter	Min Dimens (um)
101	Width of N-Well	5.0
102	Spacing between wells at same potential Merge if below 2 um (cold Well)	4.0
103	Spacing between wells at different potential (Hot Well)	8.0



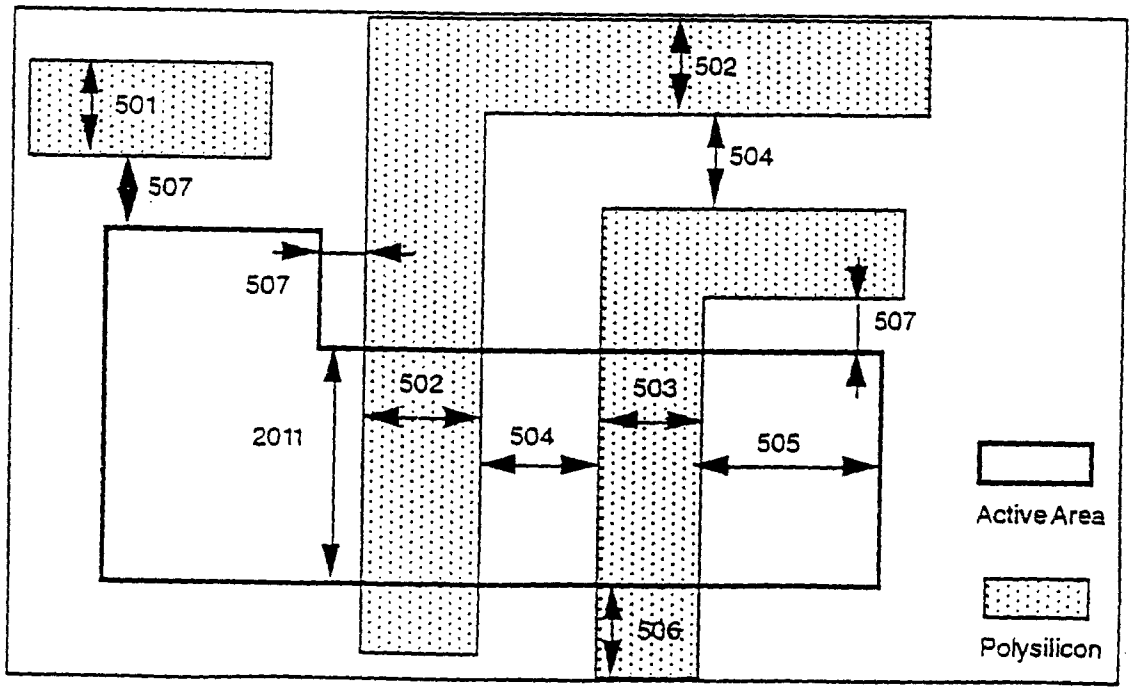
Layer 20 - Active Area

Rule Nb	Parameter	Min Dimens (um)
201	Width of N+ / P+ active area for interconnect	1.0
2011	Width of gate region	1.25
202	Spacing between active areas or diffusions	2.0
2021	Spacing between two corners of active areas or diffusions, after sizing by 0.375 µm per edge	1.25
203	Margin of P+ Area to N-well	3.0
204	Margin of N+ area to well (well tap) (N+ Area inside Well for Well Tap)	0.0
205	Spacing between N+ area and N-well (cold Well)	3.0
206	Spacing between N+ area and N-well (hot Well)	6.0
207	Spacing between P+ Area and N-Well (P+ Area outside Well for substrate Tap)	3.0



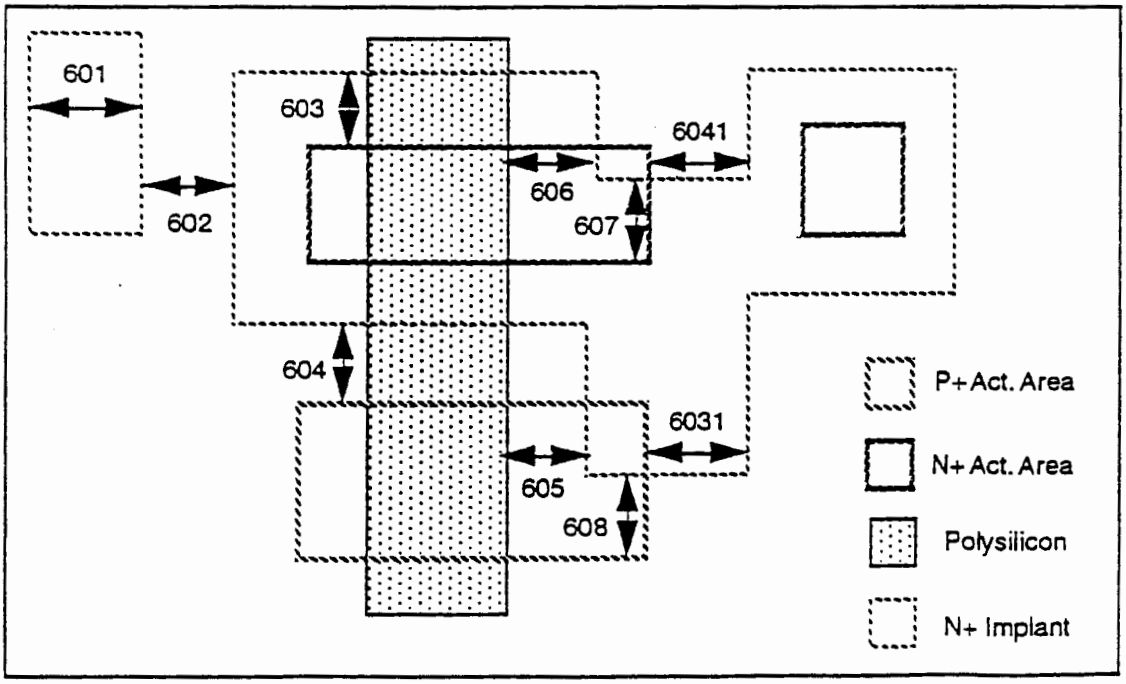
Layer 50 - Polysilicon

Rule Nb	Parameter	Min Dimens (um)
501	Width of Polysilicon (Interconnect)	1.0
502	Width of polysilicon : NMOS	1.0
503	Width of polysilicon : PMOS	1.0
504	Spacing between two stripes of polysilicon	1.5
505	Margin of Polysilicon to active Area Actual value should be determined by the Design engineer with consideration to spreading resistance.	1.5
506	Polysilicon overlap of active Area	1.0
507	Spacing between polysilicon and active Area	0.5



Layer 60 - N+ Source / Drain Implant

Rule Nb	Parameter	Min Dimens (um)
* 601	Width	1.25
* 602	Spacing (merge if less than 1.5 um)	1.5
603	overlap of N+ Active Area on substrate	1.0 1.25
6031	overlap of N+ Active Area on N-Well	0.5
604	Spacing to P+ Active Area on N-Well	1.0
6041	Spacing to P+ Active Area on Substrate	0.5
605	Spacing to polysilicon gate over P+ Active Area	1.25
606	Overlap of polysilicon gate over N+ Active Area	1.0
607	Coincidence of N+ implant to active Area for when N+ implant Does not overlap active Area	1.25
608	N+ implant margin to Active Area for N-Well contact.	1.25



Layer 65 - P+ Source / Drain Implant

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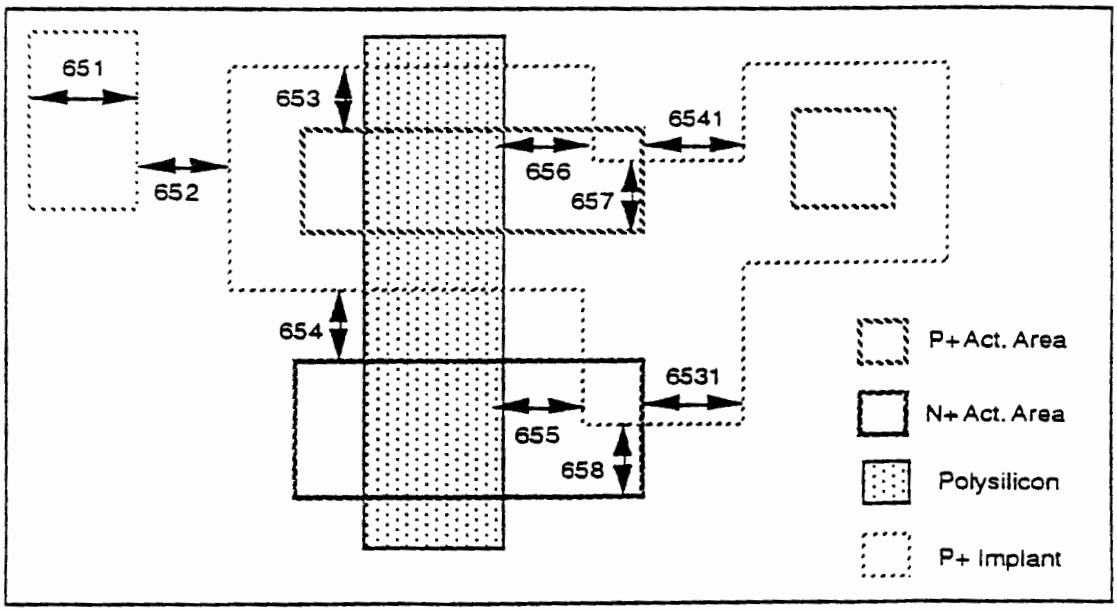
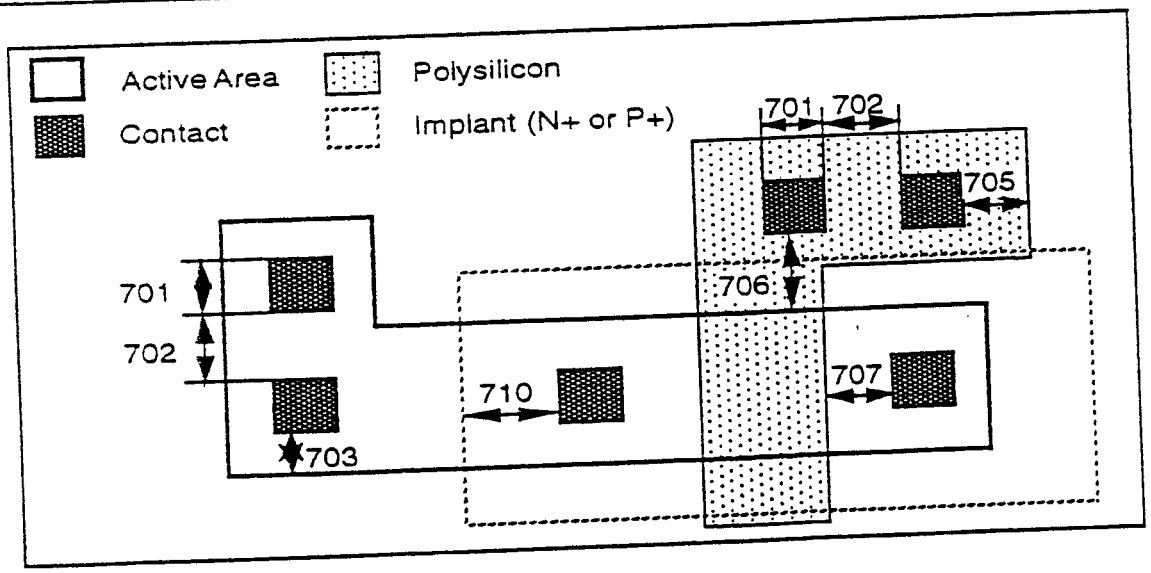
Rule Nb	Parameter	Min Dimens (um)
651	Width	1.25
652	Spacing (merge if less than 1.5 um)	1.5
653	overlap of P+ Active Area on N-Well	1.0
6531	overlap of P+ Active Area on Substrate	0.5
654	Spacing to N+ Active Area on substrate	1.0
6541	Spacing to N+ Active Area on N-Well	0.5
655	Spacing to polysilicon gate over N+ Active Area	1.25
656	Overlap of polysilicon gate over P+ Active Area	1.0
657	Coincidence of P+ implant to active Area for when P+ implant Does not overlap active Area	1.25
658	P+ implant margin to Active Area for Substrate contact.	1.25
659	Active Area must be N+ or P+ implanted	
660	No coincidence between N+ and P+ implant	
661	Adjacent (Butting) P+ and N+ active Areas must be at the same potential	



Layer 70 - Contacts

Rule Nb	Parameter	Min Dimens (um)
701	Minimum and maximum contact width (Active area and polysilicon)	1.0 1.5
702	Spacing	0.75
703	Diffusion contact margin to active area	0.75
705	Poly contact Margin to polysilicon	1.0
706	Poly contact spacing to active area	1.0
707	Diffusion contact spacing to polysilicon gate	0.5
709	Margin of Diffusion contacts to N+ implant (cold diffusions only)	0.5
710	Margin of Diffusion contacts to P+ implant (cold diffusions only)	0.5
711	Spacing of diffusion contacts to P+ implant (cold diffusions only)	0.5
712	Spacing of diffusion contacts to N+ implant (cold diffusions only)	
713	Contact to polysilicon not allowed over active area	
714	Shorting contacts are not allowed	
715	Contacts must be on polysilicon or on active area	
716	Max current through a contact is : at 70 C : 3.3 mA at 100C : 1.4 mA at 125C : 0.7 mA	



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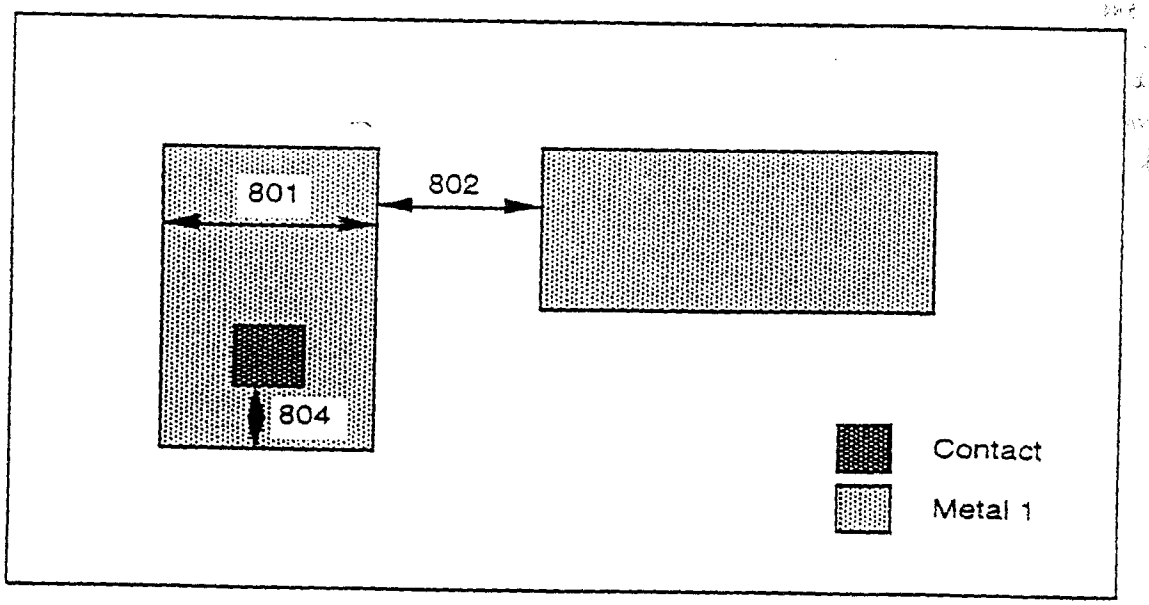
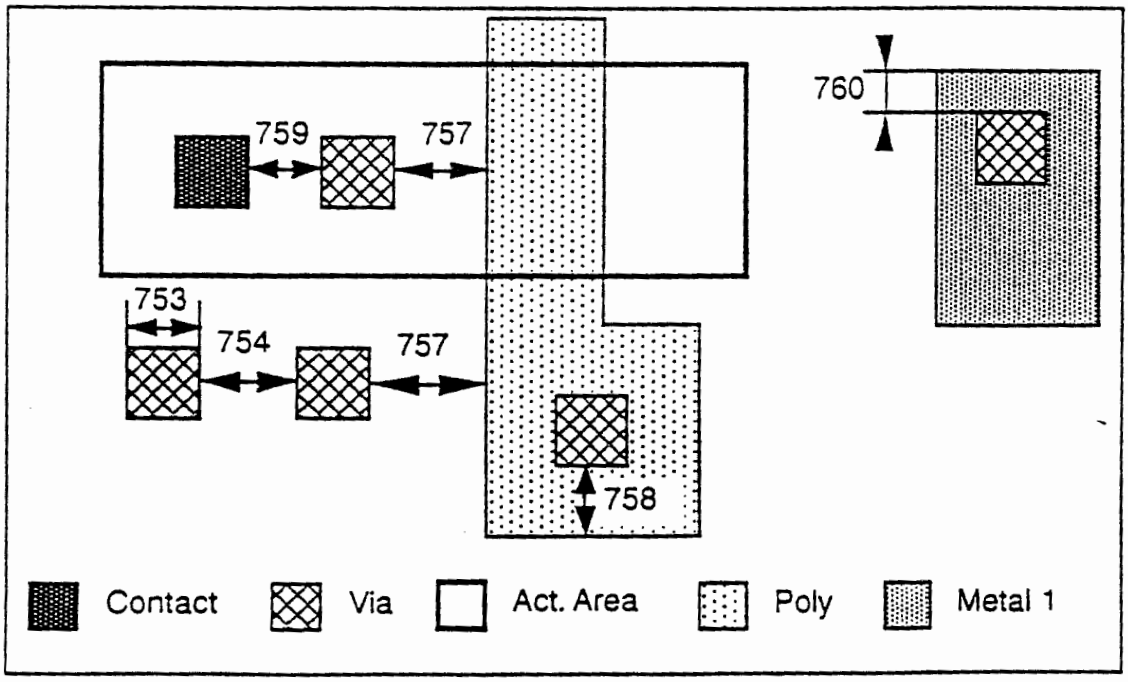
Layer 80 - Metal 1

Rule Nb	Parameter	Min Dimens (um)
801	Width	1.5
802	Spacing	1.5
8021	Spacing between two corners of metal 1, after sizing by 0.125 µm per edge	1.25
804	Overlap of contact	0.75
805	All contacts must be covered with metal 1	
806	Maximum allowed current for a line of width W (in µm) is : - At 70 DC : I=2.5*(W-0.2) (mA) - At 100 DC : I=1.1*(W-0.2) (mA) - At 125 DC : I=0.53 (w-0.2) (mA) Where current I is : - Average current for frequency > 10 Hz - Root mean square current for frequency < 10 Hz - Max DC current for DC Analysis Maximum allowed peak current is : 3*I	
807	The usage of Metal1 for capacitor is not allowed since related dielectric layers are subject to change with process optimization. For more information, contact ES2/MTD.	



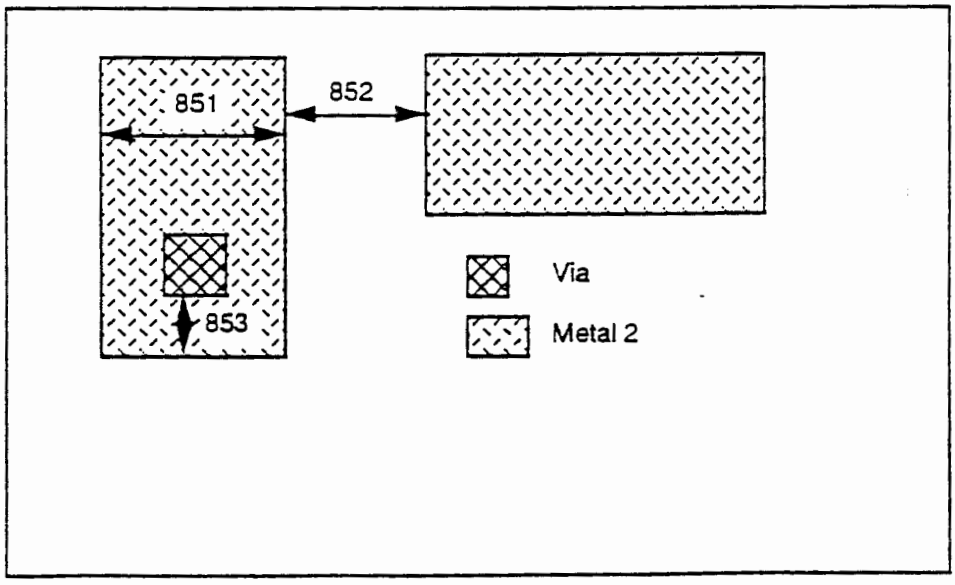
Layer 75 - Vias

Rule Nb	Parameter		Min Dimens (um)
751	Via opening is allowed only between Metal 1 and Metal 2		-
752	Stacked via on contact not allowed		-
753	Minimum and maximum width (except for bonding pads)		1.0
754	Spacing		1.5
757	Spacing to polysilicon		1.5
758	Margin to polysilicon		1.5
759	Spacing to contact		1.5
760	Margin to metal 1		0.75
761	Max current through a via is :	at 70C : 3.3 mA at 100C : 1.4 mA at 125C : 0.7 mA	



Layer 85 - Metal 2

Rule Nb	Parameter	Min Dimens (um)
851	Width	1.5
852	Spacing	1.5
8521	Spacing between two corners of metal 2, after sizing by 0.125 µm per edge	1.25
853	Overlap of via	0.75
854	Maximum allowed current for a line of width W (in µm) is : - At 70 DC : I=3.1*(W-0.2) (mA) - At 100 DC : I=1.3*(W-0.2) (mA) - At 125DC : I=0.66 (W-0.2) (mA) Where current I is : - Average current for frequency > 10 Hz - Root mean square current for frequency < 10 Hz - Max DC current for DC Analysis Maximum allowed peak current is : 3*I	
855	The usage of Metal 2 for capacitor is not allowed since related dielectric layers are subject to change with process optimization.	



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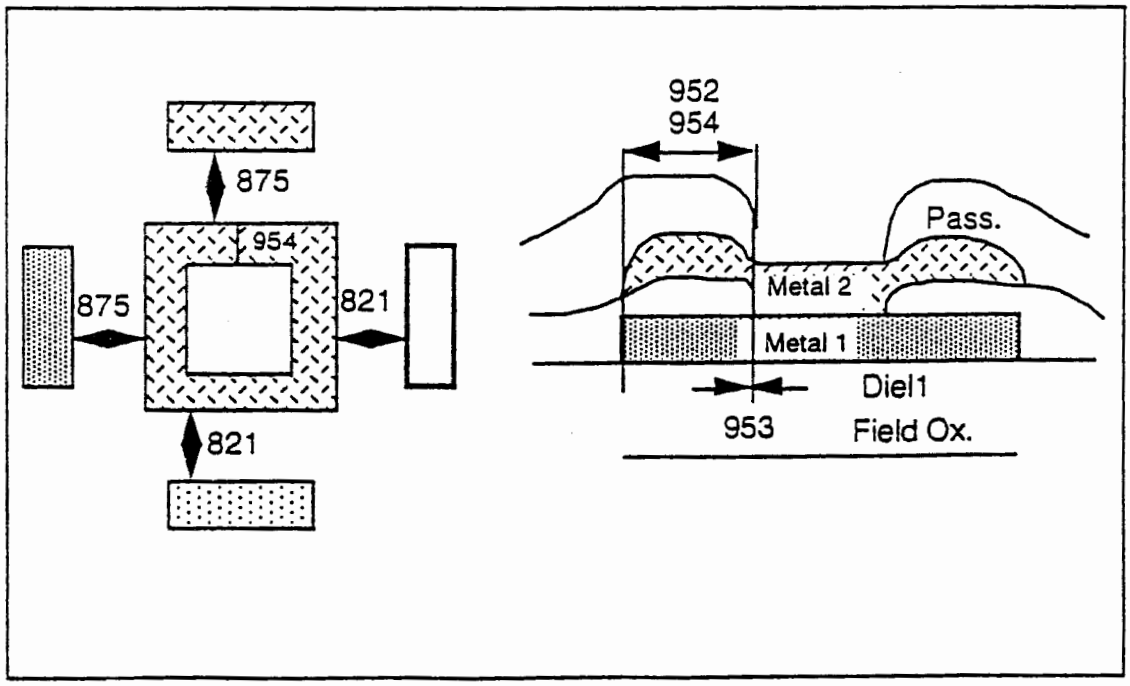
Layer 90 - Passivation Openings

Rule Nb	Parameter	Min Dimens (um)
901	Width	95.0
902	Opening to opening space : Best case	25.0
	Note : this allows for best case assembly pitch. This best case might not be possible for all configurations and packages types. For plastic assembly, the opening to opening space must be: Please refer to assembly rules.	55.0

Bonding Pads

Rule Nb	Parameter	Min Dimens (um)
951	Bonding pads shall consist of metal 2 / via / metal 1	-
952	Margin of passivation opening to metal 2	5.0
953	margin of passivation opening to pad via, min and max value	0.0
954	Margin of passivation opening to metal 1	5.0
875	Spacing of metal 2 pad to unrelated metal 2, metal 1, polysilicon or active area	25.0
821	Spacing of metal 1 pad to unrelated metal 1, metal 2, polysilicon or active area	25.0
960	Spacing of metal 1 &2 pad to next metal 1 & 2 pad : Note : For plastic assembly the pad center to pad center pitch must be 150 um (refer to rule 902).	15.0

Note : Rule 753 does not apply for bonding pads.



7.0 Layer Assignment

The following information is given for reference only. For full information about layer assignment, please consult the specification EG2-L001 "Database transfer to MTD".

The data will be assigned to the following layers :

Layer content	GDSII	CIF name
Drawn circuit data	layer 1-20	Cxyz
Sized circuit data	layer 21-40	Sxyz
Service patterns (PID, logo, scribe...)	layer 41-60	Pxyz
Label	layer 61	TLAB
Cell boundary	layer 62	TCLB
Text	layer 63	TEXT

Layer Title	GDSII	CIF name
Exclusion layer for DRC, must cover only PID block	00	CXCL
N-well implant	01	CNWI
Active Area	02	CTOX
Field Implant (not drawn, generated by MTD)	04	CNFI
Polysilicon	11	CPOL
N+ implant	12	CNPI
P+ implant	14	CPPI
Contacts	16	CCON
Metal 1	17	CME1
Vias	18	CVIA
Metal 2	19	CME2
Passiv. opening	20	CPAS

8.0 LATCH-UP Guidelines.

Customers can use their own Latch-up protection, however in that case, no garantee will be given regarding latch-up immunity. They can also use I/O pads description and layout provided by ES2 Design Center.

8.1. All output transistors have to satisfy the following rules :

Regle × : Transistor de sortie

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8.1.1 PMOS Transistor :

8.1.1.1 The gate has to be a closed ring of PS with the drain inside.

8.1.1.2 A N+ base guard ring must be placed around the source covered by metal 1 as much as possible with contact holes at minimum spacing. The guard ring must be connected to VDD using unbroken metal.
Minimum width of the base guard ring : 2.5 um.

8.1.1.3 Maximum distance between a point inside the N+ base guard ring and the N+ base guard ring itself : 18.75 um.
Note : More than one gate ring may be inside the base ring.

8.1.1.4 A P+ collector guard ring must be placed around the N+ base guard ring covered by metal1 as much as possible with contact holes on minimum spacing. The P+ guard ring must be connected to VSS using unbroken metal.
Minimum width of the collector guard ring : 2.5 um.
Distance of base guard ring to collector guard ring : 7.5 um.

8.1.2 NMOS Transistor :

8.1.2.1 The gate has to be a closed ring of PS with the drain inside.

8.1.2.2 A P+ base guard ring must be placed around the source covered by metal 1 as much as possible with contact holes at minimum spacing. The guard ring must be connected to VSS using unbroken metal.
Minimum width of the base guard ring : 2.5 um.

8.1.2.3 Maximum distance between a point inside the P+ base guard ring and the P+ base guard ring itself : 18.75 um.
Note : More than one gate ring may be inside the base ring.

8.1.2.4 A N+ collector guard ring must be placed around the P+ base guard ring covered by metal1 as much as possible with contact holes on minimum spacing. The N+ guard ring must be connected to VDD using unbroken metal.
Minimum width of the collector guard ring : 2.5 um.
Distance of base guard ring to collector guard ring : 7.5 um.

8.1.3 Minimum distance of the collector guard ring of P-MOS to the collector guard ring of N-MOS : 9 um.

8.1.4 The guard ring should be covered with metal 1 and connected to metal 1 as frequently as possible.

8.1.5 The connection of guard rings to VDD or VSS may not be of PS.

8.2. Input transitors must be connected to the input bondpad via a prescribed ESD protection Device. The protection Device will also contain latch-up precautions compatible to those specified under 8.1. Any device connected to the pad area must have a guard ring.

8.3 Internal logic.

8.3.1 The internal Logic must be surrounded with a P+ base guard ring and connected to VSS. This base guard ring must be surrounded with a N+ collector guard ring and connected to VDD. Special attention is needed for large drivers (e.g. clock buffers).

8.3.2 In a N-Well at least one Well contact should be present. For large Wells more than one contact is needed, with a spacing between the contacts of 100 um at most.

8.3.3 Substrate contacts have to be placed as much as possible with a spacing of 300 um at most, but 100 um spacing is preferred.

9. Input ESD protection.

9.1. Customers may use their own ESD input protection structures. However, in that case no guarantee will be given regarding the ESD protection.

9.2. They can also use ESD protected inputs provided by ES2. Please contact your design center regarding those input pads.

10.6 Parameters of parasitic devices.

RESISTANCES	UNIT	SLOW	TYP.	FAST
N-Well Sheet Res.(Field)	Kohm/sq	1.4	1.25	1.0
N+ Sheet Res.	Ohm/sq	68	55	42
P+ Sheet Res.	Ohm/sq	95	70	50
Poly Sheet Res.(Int.)	Ohm/sq	35	27	18
Metal 1 Sheet Res.	mOhm/sq	100	60	T.B.D
Metal 2 Sheet Res.	mOhm/sq	50	30	T.B.D
N+ Contact Res.(1.0)	Ohm	40	15	
P+ Contact Res. (1.0)	Ohm	80	50	
Poly Contact Res. (1.0)	Ohm	25	8	
Via Contact Res. (1.0)	Ohm	3	0.5	-

CAPACITANCES	UNIT	SLOW	TYP.	FAST
MOSFET CAPACITANCES.				
Gate to Substr.	µF/m2	1920	1730	1570
N+ junction (Area)	µF/m	570	520	470
N+ junction (Edge)	pF/m	330	300	270
P+ junction (Area)	µF/m2	660	600	540
P+ junction (Edge)	pF/m	900	820	740
INTERCONNECT RELATED CAPACITANCES.				
AREA.				
Poly to Substr. (Field)	µF/m2	64	58	52
Metal 1 to Substr. (Field)	µF/m2	32	29	26
Metal1 to N+or P+ Diff.	µF/m2	55	49	45
Metal 1 to Poly	µF/m2	67	61	55
Metal 2 to Substr. (Field)	µF/m2	19	17	16
Meaul 2 to N+ or P+ Diff	µF/m2	26	23	21
Metal 2 to Poly	µF/m2	31	27	25
Metal 2 to Metal 1	µF/m2	55	49	45
FRINGING.				
Poly to Substr. (Field)	pF/m	56	51	46
Metal 1 to Substr.	pF/m	49	44	39
Metal1 to N+or P+ Diff.	pF/m	57	51	47
Metal 1 to Poly	pF/m	59	54	49
Metal 2 to Substr.(Field)	pF/m	61	55	52
Metal 2 to N+ or P+ Diff.	pF/m	70	62	57
Metal 2 to Poly	pF/m	76	66	61
Metal 2 to Metal 1	pF/m	92	82	75

11. Electrical Key parameters

These parameters are part of the electrical conformance test performed on ES2 wafers . The full contractual acceptance list should be requested from your design center. The min and max parameters are taken from the process limit files (# 3 sigma) . The drain current are determined from the slow and fast cases of the transistors models .

PARAMETER	DEVICE		MIN	TYP	MAX	UNITS	Conditions
VT LIN EXT	20/20	N	0.66	0.82	0.97	V	EXT at VDS = .1V
BETA	20/20	N	86	97.6	114	µA/V2	SLOPE OF Lin Cha
GAMA1	20/20	N	0.65	0.75	0.85	V1/2	VSUB = 0,-.5V
GAMA2	20/20	N	0.48	0.58	0.69	V1/2	VSUB = -4, -5V
VT LIN EXT	20/1.0	N	0.56	0.73	0.90	V	EXT at VDS = .1V
GAMA1	20/1.0	N	0.42	0.58	0.73	V1/2	VSUB = 0,-.5V
GAMA2	20/1.0	N	0.17	0.30	0.42	V1/2	VSUB = -4, -5V
ISAT	20/1.0	N	5.04	6.60	8.47	mA	Vgs=Vds=5 V
DELTA L		N	-0.39	-0.24	-0.09	µm	from BETA L=20 & 1.0 um
CD N+ (1.0 um)		N	1.0	1.3	1.6	µm	

PARAMETER	DEVICE		MIN	TYP	MAX	UNITS	Conditions
VT LIN EXT	20/20	P	- 1.21	-1.06	- 0.91	V	EXT at VDS = -.1V
BETA	20/20	P	33	38	43	µA/V2	SLOPE OF Lin Cha
GAMA	20/20	P	0.52	0.63	0.76	V1/2	VSUB = 0, 2.5 V
VT LIN EXT	20/1.0	P	- 1.24	- 1.08	- 0.94	V	EXT at VDS = - .1V
GAMA	20/1.0	P	0.23	0.38	0.52	V1/2	VSUB = 0, 2.5 V
ISAT	20/1.0	P	- 2.13	- 2.97	- 4.26	mA	Vgs=5V , Vds=-5 V
DELTA L		P	-0.23	-0.08	+0.07	µm	from BETA L=20 & 1.0 um
CD P+ (1.0 um)		P	1.0	1.3	1.6	µm	

12. Process flow.

1 Starting Material
2 Initial Oxide
3 P-Well Implant
4 N-Well Mask
5 N-Well Implant
6 N-Well Drive
7 Pad Oxyde
8 Nitride deposition
9 Active Area/Diffusion Mask
10 Nitride Etch
11 Field implant Mask
12 Field implant
13 Field Oxide
14 Nitride removal
15 Thin Gate Oxide
16 VT adjust implant
17 Poly Si deposition
18 Poly Si Doping
19 Poly Si Mask
20 Poly Si Etching
21 Poly Si Oxide
22 N- implant Mask
23 N- implant
24 Oxide Deposition
25 Spacer Etch
26 N+ implant Mask
27 N+ implant
28 Poly oxidation
29 P+ S/D implant Mask
30 P+ S/D implant
31 Isolation Oxide
32 Flow
33 Contact Mask
34 Contact Etch
35 Contact Reflow
36 Metal1 deposition
37 Metal1 mask
38 Metal Etch
39 Intermetal Oxide
40 Via Mask
41 Via Etch
42 Metal2 deposition
43 Metal2 Mask
44 Metal Etch
45 Passivation layer deposition
46 Pad Mask
47 Passivation Etch
48 Alloy

LAYER STACKING IN GUARD RING AND SCRIBE-LINE