Very basic rules to facilitate analysis / synthesis of integrated analog circuits

In these slides:

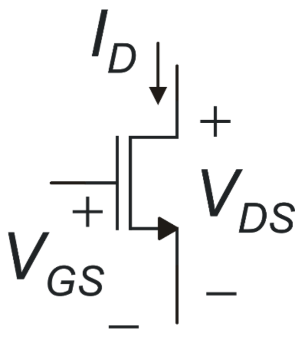
1. How to obtain the large signal equation of p-type transistors from n-type ones and a few intuitive views about both.
2. Basic expressions for the resistances seen from each terminal in notable single-transistor configurations.
3. The $g_m r_d$ ($g_m r_o$ in BJTs) product
4. Power rails, floating rails and reference nodes

1. From n-type transistors to p-type ones

We will start from MOSFETs and, at last, will briefly cite the case of BJTs. These considerations apply to the **large signal behavior**, since the small-signal equivalent circuits of n-type and p-type transistors are identical.

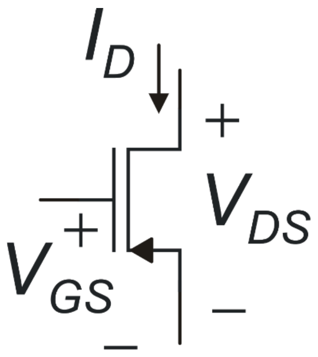
From n-MOSFETs to p-MOSFETS

N-MOS



$$V_{DS} \geq 0$$
$$V_{GS} - V_{tn} \geq 0$$
$$I_D \geq 0$$

P-MOS



$$V_{DS} \leq 0$$
$$V_{GS} - V_{tp} \leq 0$$
$$I_D \leq 0$$

Apply this transformation:

$$-V_{DS-p} \Rightarrow V_{DS-n} \quad (-V_{DSAT-p} \Rightarrow V_{DSAT-n})$$
$$-\left(V_{GS-p} - V_{tp}\right) \Rightarrow \left(V_{GS-n} - V_{tn}\right)$$
$$-I_{D-p} \Rightarrow I_{D-n}$$

And put it into the n-MOS equations:

$\Downarrow$

Obtain the correct p-MOS equations!

Useful examples: transition between triode and saturation region

$$V_{DS} \geq V_{DSAT}$$

$$V_{DSAT} = \begin{cases} \cong 100 \text{ mV (weak inversion)} \\ V_{GS} - V_{tn} \text{ (strong inversion)} \end{cases}$$

N-MOS

Applying the transformation

$$-V_{DS} \geq -V_{DSAT} \Rightarrow V_{DS} \leq V_{DSAT}$$

$$-V_{DSAT} = \begin{cases} \cong 100 \text{ mV (weak inversion)} \\ -\left(V_{GS} - V_{tp}\right) \text{ (strong inversion)} \end{cases}$$

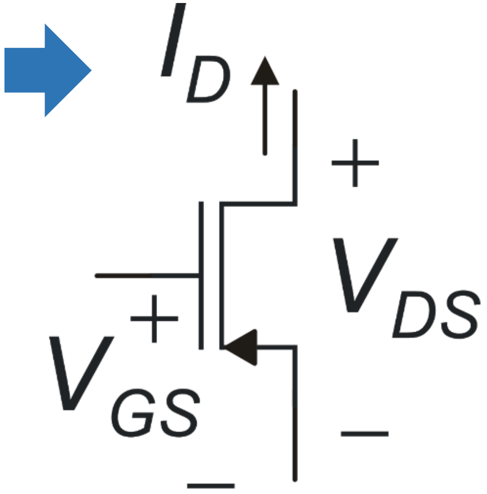
P-MOS

The "natural" direction of the current in P-type transistors

$$I_D \Rightarrow -I_D$$

This is equivalent to reverse the conventional direction of the drain current for P.MOSFETs

By this convention, the drain current is positive also in P-MOSFETs



An intuitive view to deal with p-MOSFETs

always

$$\boxed{V_{DS} \leq 0 \Rightarrow -V_{DS} = \left|V_{DS}\right|}$$

$$\boxed{\left(V_{GS} - V_{tp}\right) \leq 0 \Rightarrow -\left(V_{GS} - V_{tp}\right) = \left|V_{GS} - V_{tp}\right|}$$

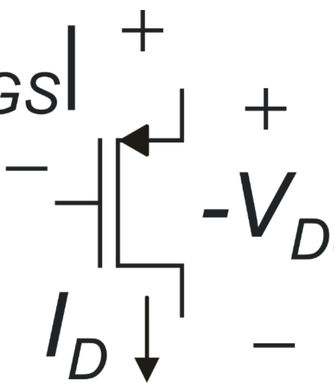
in strong and moderate inversion

$$\boxed{\begin{array}{l} V_{tp} < 0 \Rightarrow -V_{tp} = \left|V_{tp}\right| \\ V_{GS} - V_{tp} \leq 0 \Rightarrow V_{GS} \leq V_{tp} \leq 0 \end{array}}$$

in strong inversion for enhancement p-MOSFETs

The voltage drop across the mosfet, measured along the natural direction of I_D is $|V_{DS}|$

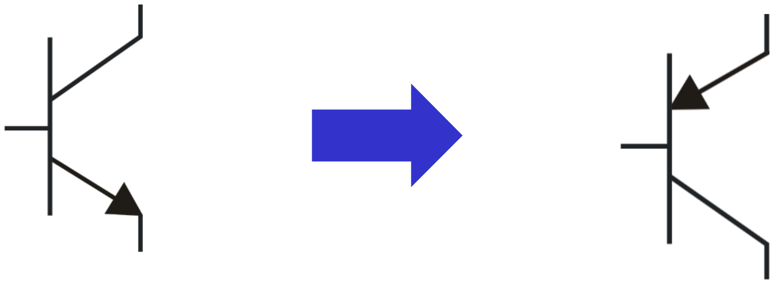
$-V_{GS} = |V_{GS}|$

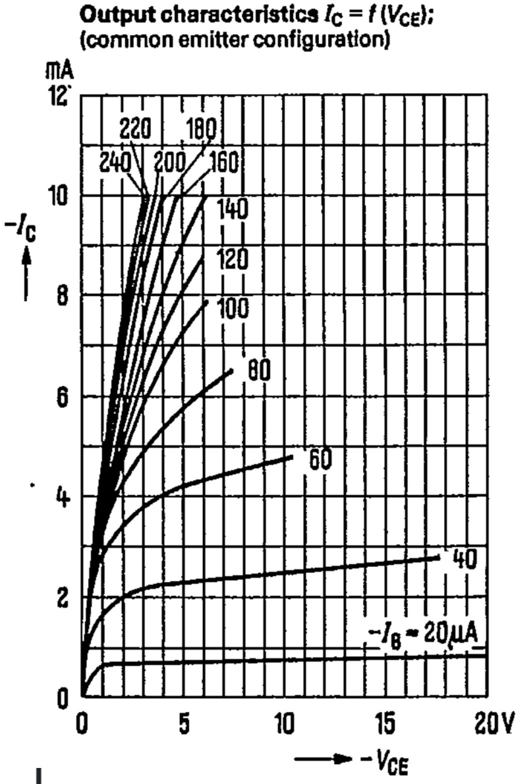


$-V_{DS} = |V_{DS}|$

Passing from the gate to the source the voltage is increased by $|V_{GS}|$

From NPN BJTs to PNP ones

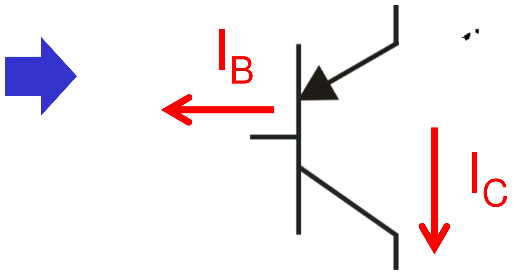




Transformations

$$\begin{cases} V_{CE} \Rightarrow -V_{CE} \quad (V_{CESAT} \Rightarrow -V_{CESAT}) \\ V_{BE} \Rightarrow -V_{BE} \\ \left.\begin{matrix} I_C \Rightarrow -I_C \\ I_B \Rightarrow -I_B \end{matrix}\right\} \end{cases}$$

These two can be avoided if the opposite convention for the current direction is used

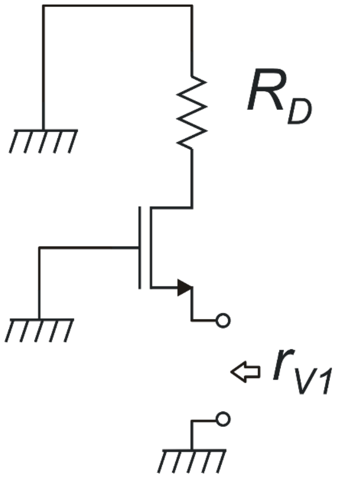


2. Notable case of small signal resistances

In order to simplify the analysis of circuits including a large number of devices, it is important to keep in mind simple expressions of the resistances that are seen from one terminal of a transistor to *gnd* in different configurations.

In the next slides, cases of great importance for the synthesis of electronic circuits are recalled. The expressions may be complicated, and it is important to remember only the simplified forms and the broad conditions for which the approximations hold true

The six basic (small signal) resistances: MOSFETS (for simplicity, body effect is neglected in these formulas)

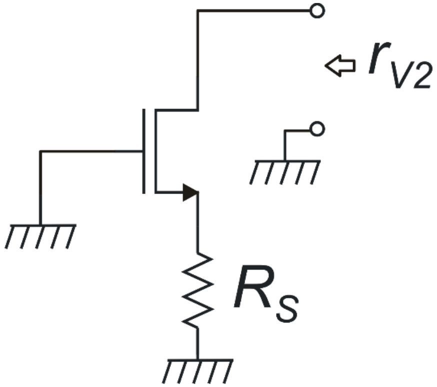


$$r_{v1} \cong \frac{1}{g_m}$$

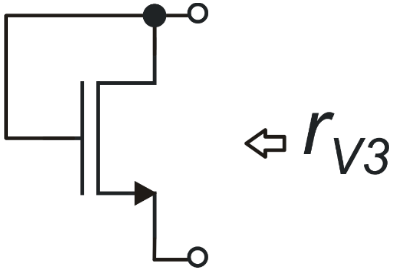
$$r_{v1} = \frac{R_D + r_d}{1 + g_m r_d}$$ exact result

Conditions for approximation

$$g_m r_d >> 1 \quad \text{and} \quad R_D << r_d \quad \Rightarrow \quad r_{v1} \cong \frac{1}{g_m}$$



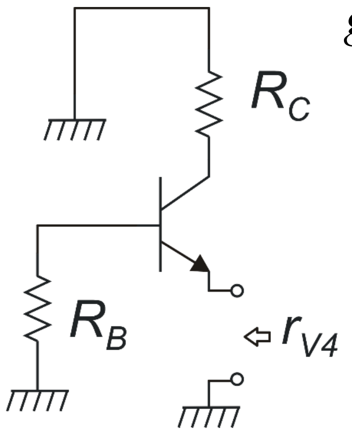
$$r_{v2} = R_S + r_d\left(1 + g_m R_S\right)$$



$$r_{v3} = \quad r_D \,//\, \frac{1}{g_m} \quad \cong \frac{1}{g_m}$$

Diode-connected MOSFET

The six basic (small signal) resistances: BJTs



$$g_{meq} \equiv \frac{r_{be}}{R_B + r_{be}} g_m = \frac{h_{fe}}{R_B + r_{be}}$$

$$h_{fe} = g_m r_{be}$$

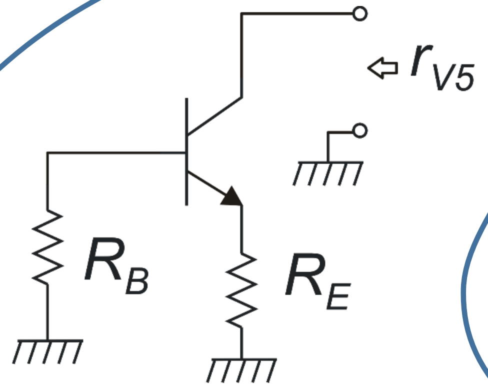
$$r_{v4} \cong \frac{1}{g_{meq}}$$

exact result

$$r_{v4} = \frac{R_C + r_o}{1 + g_{meq} r_o} // \left(r_{be} + R_B \right)$$

Conditions for approximation

$$g_{meq} r_o >> 1 \,, \quad R_C << r_o \,, \quad \frac{1}{g_{meq}} << \left(R_B + r_{be} \right)$$



exact result

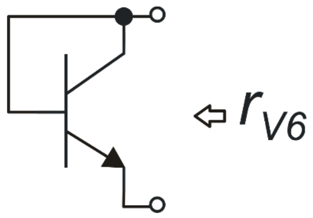
$$r_{v5} = R_{Eeq} + r_o \left(1 + g_{meq} R_{Eeq} \right)$$

$$R_{Eeq} = \left(R_B + r_{be} \right) // R_E$$

approximations

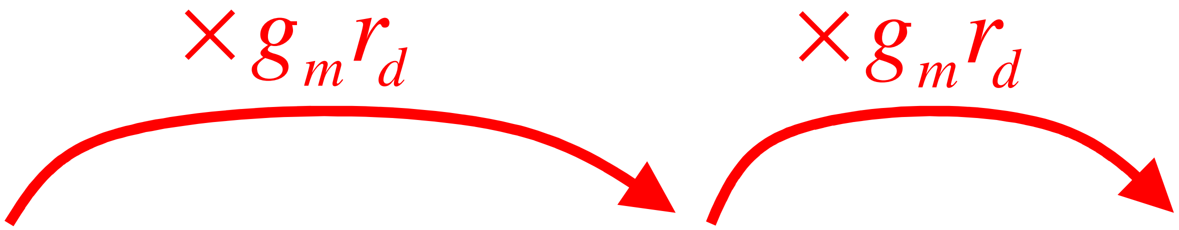
1) $R_E << \left(r_{be} + R_B \right) \Rightarrow r_{v5} \cong r_o \left(1 + g_{meq} R_E \right)$

2) $R_E >> \left(r_{be} + R_B \right) \Rightarrow r_{v5} \cong r_o \left(1 + h_{fe} \right)$



$$r_{v6} = \quad r_o // \frac{1}{g_m} // r_{be} \quad \cong \quad \frac{1}{g_m}$$

Classification of device small-signal resistances



	Small	Medium-large	Large	Very large
MOSFETs	$1/g_m$	-	r_d	$(g_m r_d) r_d$
BJTs	$1/g_m$	$r_{be}\ (h_{ie})$	r_0	$h_{fe} r_o$

3. The $g_m r_d$ product in MOSFETs ($g_m r_o$ in BJTs)

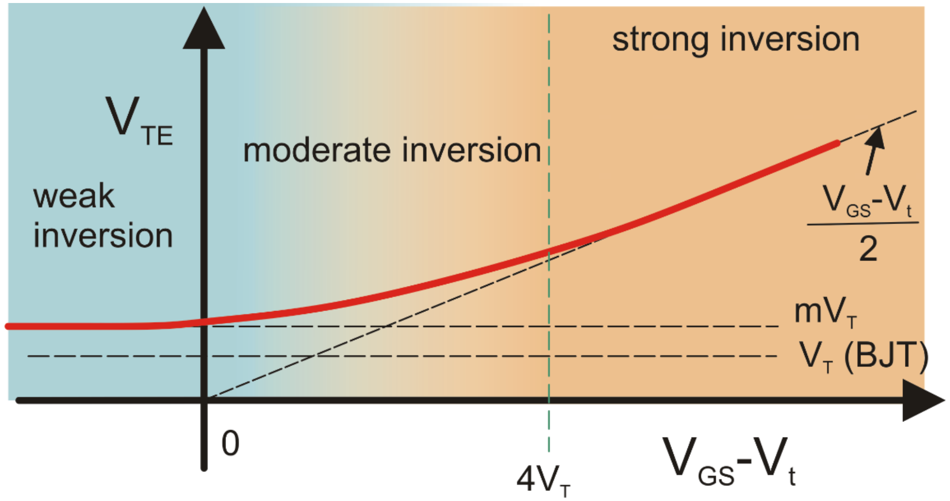
The $g_m r_d$ product in MOSFETs and JFETs, or the equivalent $g_m r_o$ product in BJT, plays an important role in many circuit configurations.

For example, this product appears in the voltage gain expression of most topologies used to design high-gain amplifier stages. A large $g_m r_d$ product is also beneficial for the output resistance of high-performance current sources.

In the next slides we will consider which are the factors that affect the $g_m r_d$ ($g_m r_o$) product.

The $g_m r_d$ product (in saturation region)

$$\left.\begin{aligned} g_m &= \frac{I_D}{V_{TE}} \\ r_d = \frac{1}{g_{ds}} = \frac{1}{\lambda I_D} &= \frac{\lambda^{-1}}{I_D} \end{aligned}\right\} \quad g_m r_d = \frac{1}{V_{TE}} \cdot \frac{1}{\lambda}$$



$$\frac{1}{\lambda} \propto L_{eff}$$

Large $g_m r_d$ products are obtained for small V_{GS}-V_t and large L

As a broad estimate, $g_m r_d$ can be considered to be of the order of **100**

$g_m r_0$ for BJTs in active zone

$$\left.\begin{array}{l} g_m = \dfrac{I_C}{V_T} \\[2ex] r_o = \dfrac{V_A}{I_C} \end{array}\right\} \quad g_m r_0 = \frac{V_A}{V_T}$$

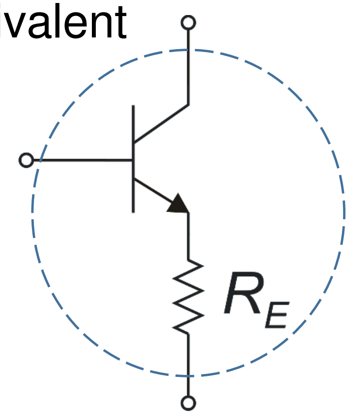
This result is correct in the I_C region where the exponential I_C vs. V_{BE} dependence holds (see the Gummel Plot)

- $g_m r_0$ may easily reach 1000 (e.g. for V_A=25 V)
- $g_m r_0$ does not depend on the BJT operating point
  (this is an important difference between BJT and MOSFETS)

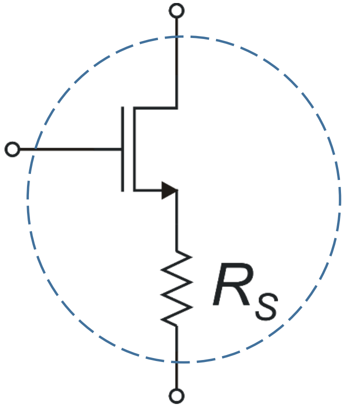
In general, the performance of BJT integrated circuits is affected by less degrees of freedom (DOFs) than CMOS ones. One of the reason is that, for a given temperature the ***g_m/I_C*** ratio is a constant (=$1/V_T$). If there is the need to change this ratio, emitter degeneration is the simplest choice.

Emitter degeneration (source degeneration)

Equivalent BJT



- Lower effective g_m for the same I_D (I_C)
- Higher equivalent r_o
- Higher input resistance (BJT)



reduced g_m

$$g_{mrid} \cong \frac{g_m}{1+g_m R_E}$$

$$\frac{g_{mrid}}{I_C} \cong \frac{1}{V_T} \cdot \frac{1}{1+g_m R_E}$$

$$g_m R_E = \frac{\boxed{I_C R_E}}{V_T}$$

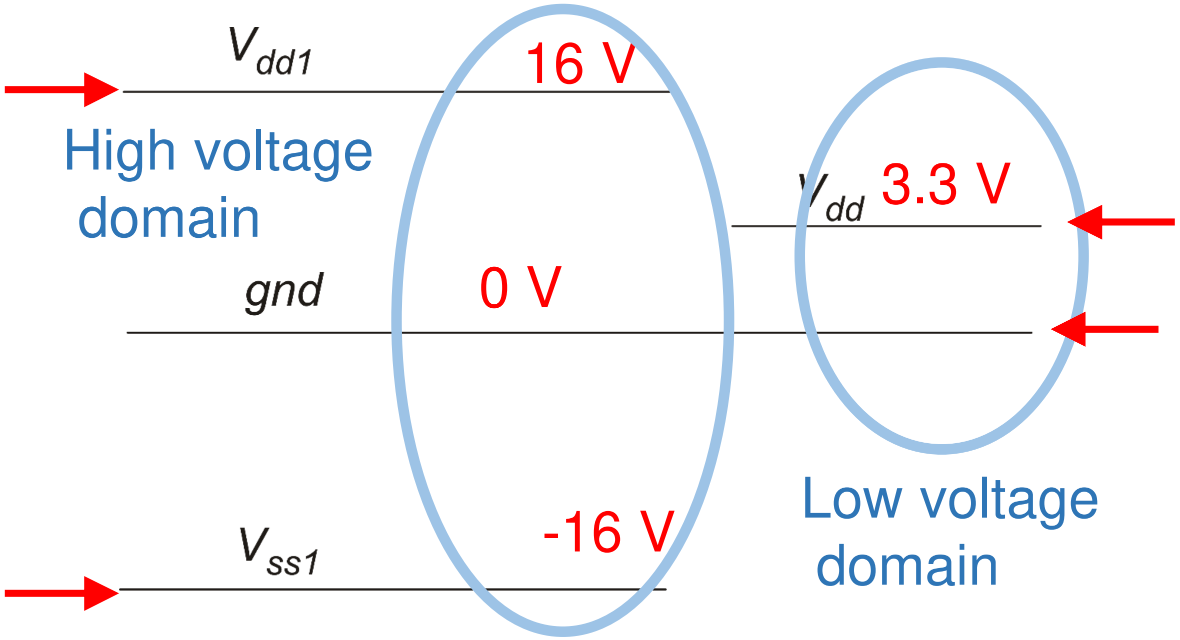
voltage drop across R_E in the operating point

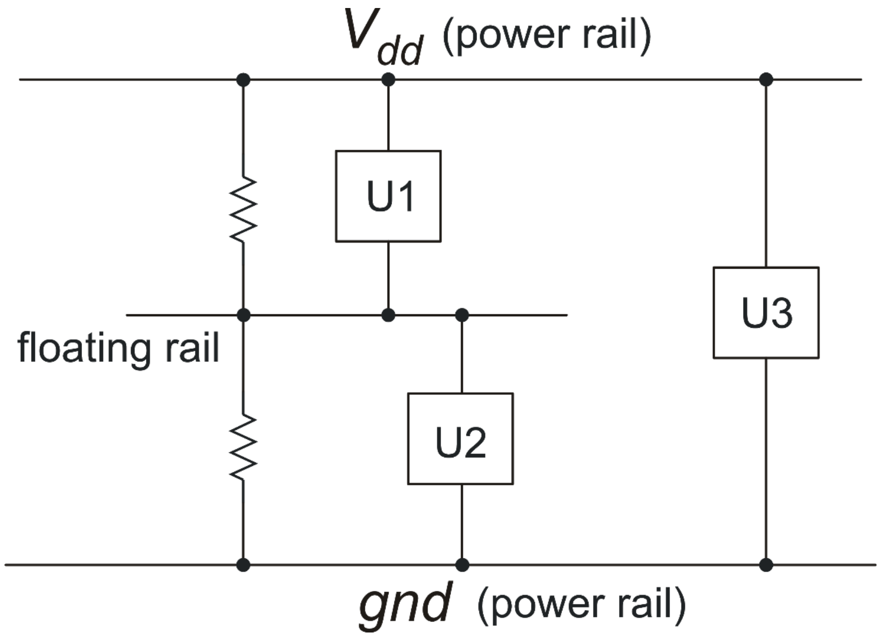
$$g_{mrid} = \frac{g_m}{1+g_m R_S}$$

$$\frac{g_{mrid}}{I_D} = \frac{1}{V_{TE}} \cdot \frac{1}{1+g_m R_S}$$

$$g_m R_S = \frac{I_D R_S}{V_{TE}}$$

4. Power rails and floating rails

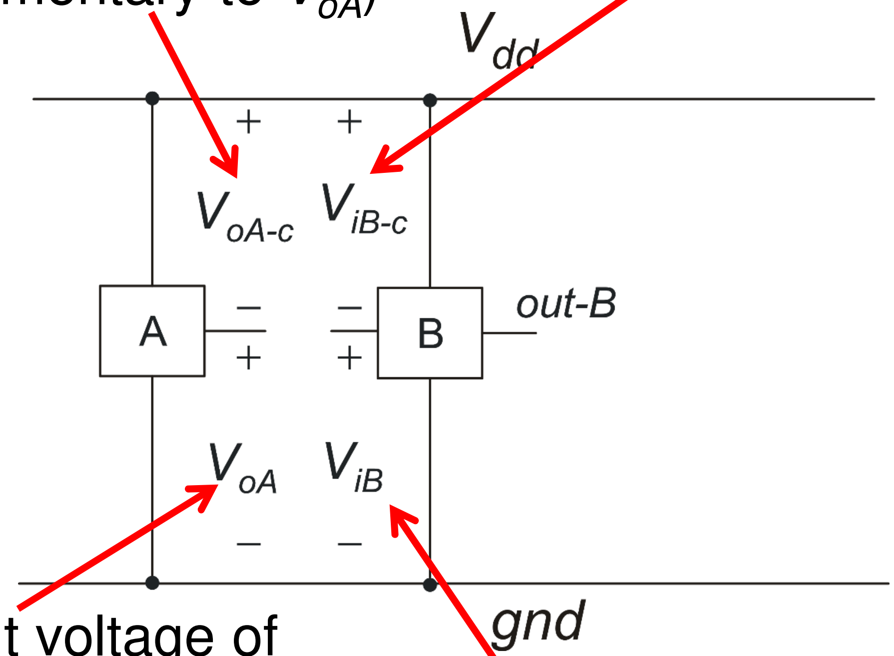




Each **power rail** is connected to a single terminal of the power supply. Power rails carry the **supply currents** to all blocks of the IC

If the currents that the **floating rail** provides to the circuits connected to it (U1 and U2) are too large, the voltage of the floating rail can be altered. In that case it is necessary to use an active circuit (e.g a voltage buffer) to create the floating rail.

Reference node for voltages: power supply invariance



Output voltage of circuit A, referred to $\boldsymbol{V_{dd}}$ (complementary to V_{oA})

Input voltage of circuit B, referred to V_{dd}

Output voltage of circuit A, referred to **gnd**

Input voltage of circuit B, referred to **gnd**

$$V_{oA-c} = V_{dd} - V_{oA}$$

Important property:

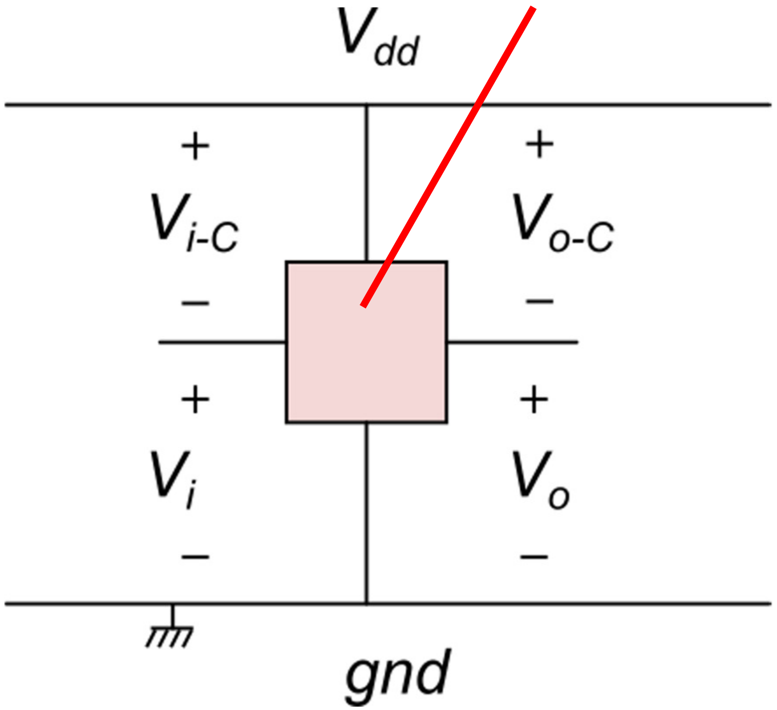
Only one out of $\boldsymbol{V_{oA}}$ and $\boldsymbol{V_{oA\text{-}C}}$ can be made invariant with respect to Vdd variations

$$V_{iB-c} = V_{dd} - V_{iB}$$

The same property applies to $\boldsymbol{V_{iB}}$ and $\boldsymbol{V_{iB\text{-}C}}$

Invariance of input and output voltages with respect to supply voltage

Depending on the topology of a given block (A) two cases are possible:



Input.

1) The "real" input signal is V_i **or**
2) The "real" input signal is $V_{i\text{-}C}$

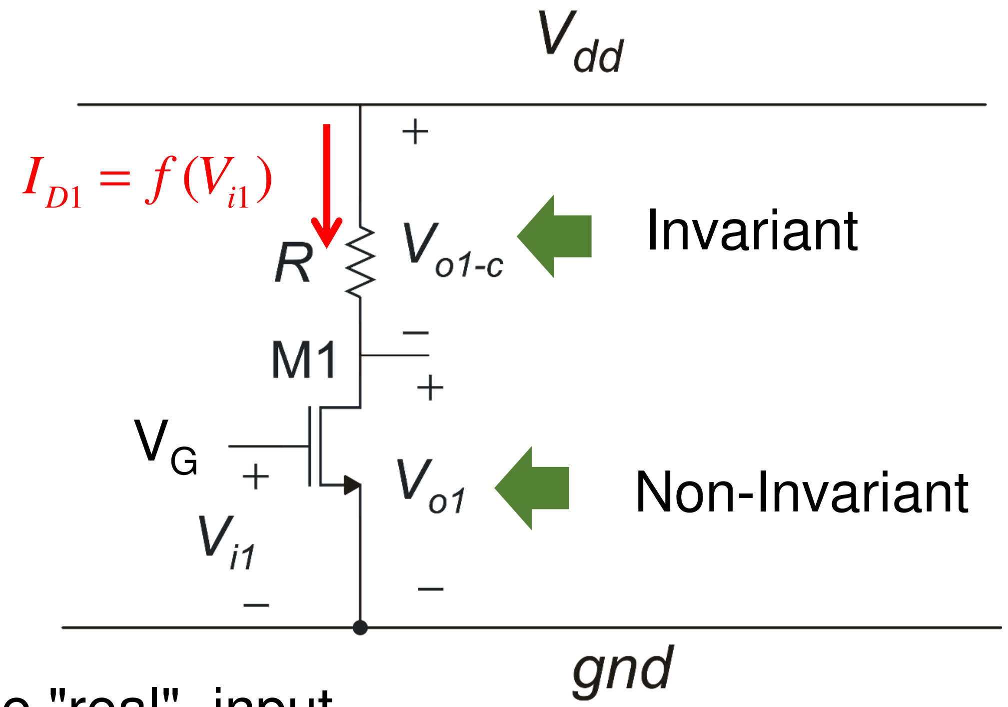
(The internal currents and output voltages do not vary if the real input is kept constant when V_{dd} varies)

Output.

For a constant input voltage:

1) V_o is independent of V_{dd} **or**
2) $V_{o\text{-}C}$ is independent of V_{dd}

Example: n-MOS common source amplifier with resistive load (unipolar)



$$V_{o1} = V_{DD} - RI_{D1} = V_{DD} - Rf(V_{i1})$$

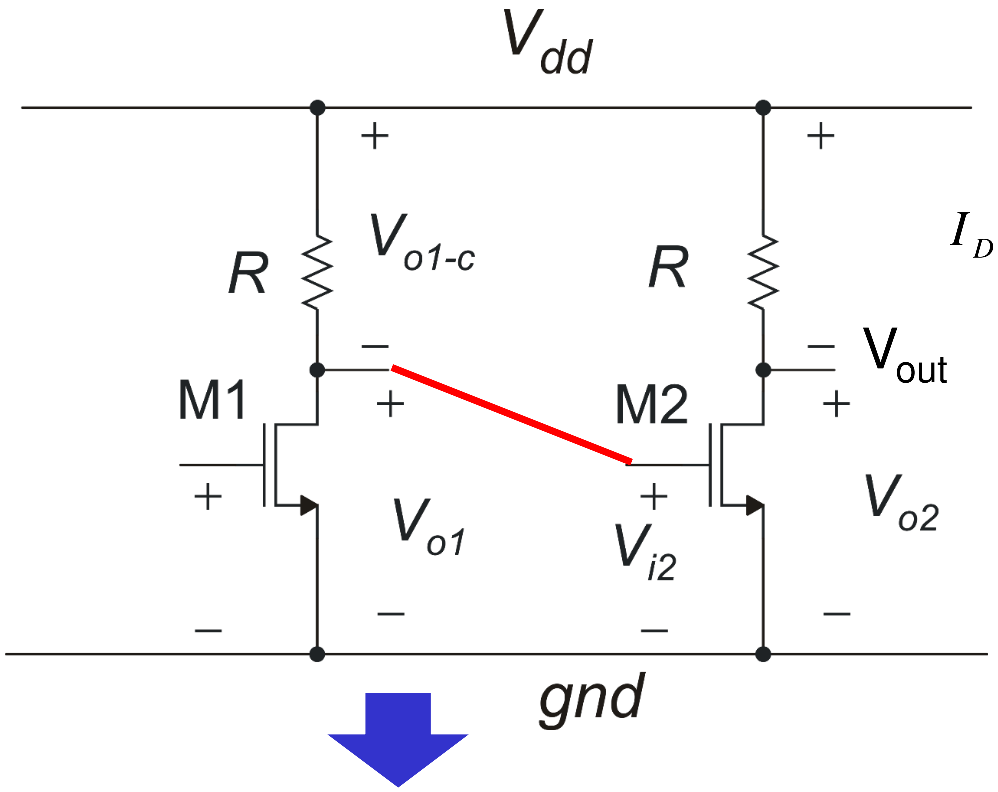
$$V_{o1-c} = RI_{D1} = Rf(V_{i1})$$

When referred to the **gnd** rail, the output voltage of this amplifier is **not** invariant with respect to the the power supply voltage (V_{dd}).

The "real" input is V_{i1}, i.e V_G referred to gnd

On the other hand, the complementary voltage $V_{o1\text{-}c}$ is invariant with respect to the supply voltage.

Example: cascade of two n-mos common source stages



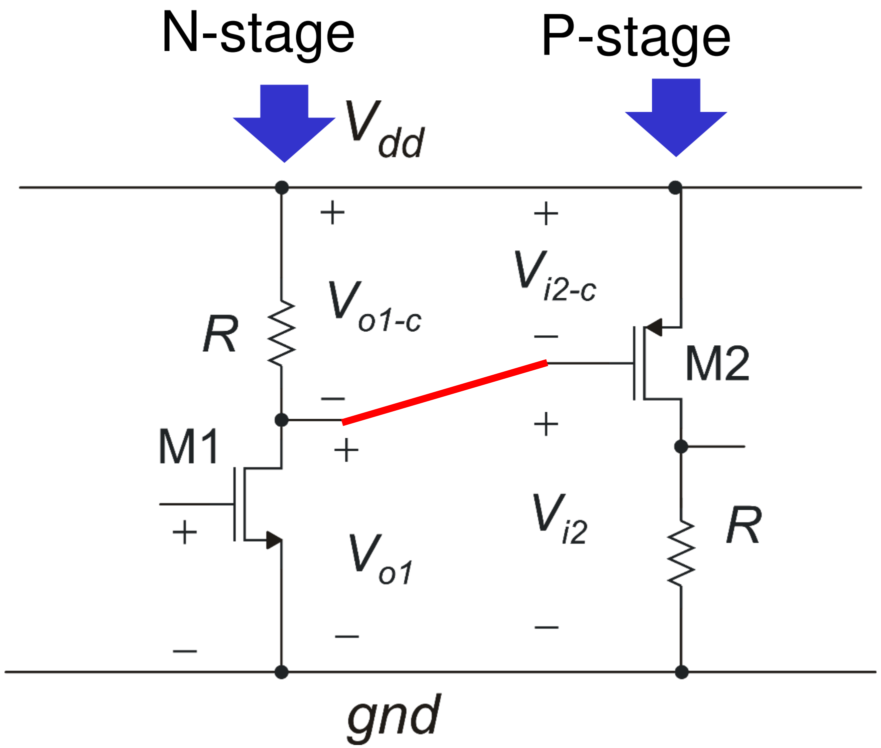
wrong configuration!

$$V_{i2} = V_{o1} = V_{DD} - Rf(V_{i1})$$

$$I_{D2} = f(V_{GS2}) = f\left[V_{DD} - Rf(V_{i1})\right]$$

I_{D2} (and then V_{out}) is strongly dependent on V_{dd}. This means a very low PSSR. For large V_{dd} variations, the operating point of M2 can be altered in an not acceptable extent.

Example: cascade of two complementary common source amplifiers



correct configuration!

$$I_{D2} = f\left(V_{GS2}\right) = f\left[Rf\left(V_{i1}\right)\right]$$

The N-stage:

- requires an input voltage (V_{i1}) that is invariant when referred to *gnd*.
- Produces a voltage that is invariant when referred to V_{dd}

The P-stage:

- requires an input voltage (V_{i1}) that is invariant when referred to V_{dd}.
- Produces a voltage that is invariant when referred to *gnd*

P-type and N-stages can be cascaded with low sensitivity to V_{dd} (high PSSR)