Project guidelines.

1. Rules for the execution of the course projects

- Projects are optional. Their aim is to improve the students' knowledge of the basic full-custom design flow. The final score of the exam is not affected by the choice of carrying out a project.
- Projects can be carried out by groups of up to 5 students. Project can be assigned to single student. The complexity of the project increases with the number of students of the group.
- Projects can be assigned in any period of the year.
- Verification of the projects consists of two phases: (1) Once the schematic project and the required simulations are completed, the students send a preliminary report (pdf) to the professor, including screenshots of the schematics and of the graphical results of simulations. If the result is satisfactory, the professor authorizes them to complete the design with the layout drawing. (2) Once the layout is completed and the verification steps (DRC, LVS) are passed, the students send a short report to the teacher by e-mail (pdf format).
- The report should include:
  -) A brief description of the task and of the criteria used for the design (two pages max).
  -) A snapshot of the schematic view, taken from LTSpice schematic editor;
  -) All the required simulation results (plots) in graphical format;
  -) A snapshot of the layout
  -) A copy of the lvs report;
- All figures in the report should be provided of a small caption, indicating the content of the figure.

2. Students' design task.

2.1 Introduction

Projects generally have the following characteristics that greatly simplify the students' design work:

1) The topology is assigned
2) The bias current is assigned.
3) The lengths of all mosfets are fixed to the same value (typically 1 μm).
4) A few design choices (e.g. mirror ratios) are given.

Once the given design choices have been implemented, the circuit topology is such that the drain currents of all mosfets can be derived from the bias current by very simple calculations that do not involve process parameters.

The students have to determine the aspect ratios (W/L ratios) of all mosfets (i.e. the W, since L is given), in order to guarantee acceptable dc operation (operating point and input/output ranges). In most cases this reduces to setting the overdrive voltage (V_{GS}-V_t) to a value, which is:

1) Large enough to bias the mosfet in strong inversion region.

2) Small enough to have a negligible impact on the input and output ranges

For these reasons, the students are asked to set the $V_{GS} - V_t$ of all mosfets to a value close to 200 mV. Deviations from this rule are acceptable, provided that the overdrive voltage stays within the [100 mV- 300 mV] interval.
This applies to all mosfets whose V_{GS}-V_t is a free parameter that can be set as small as possible, to increase the input and/or output ranges and allow operation at small power supply voltages.
This rule does not apply to particular devices whose V_{GS}-V_t should be made larger than the other ones, in order to obtain a correct operating point. These particular mosfets, if present, are indicated to the students when the project is assigned. Just for an example, consider the wide swing cascode current mirror where the V_{GS}-V_t of a single mosfet in the input branch is made larger (typically doubled) than the other overdrive voltages.

2.2 A method to set all V_{GS}-V_t to the target (200 mV) value in a simple way.

First of all, let us consider that the V_{GS}-V_t of a mosfet in strong inversion (and saturation) region can be approximated by:

$$V_{GS} - V_t = \sqrt{\frac{2I_D}{\beta}} \qquad (1)$$

where

$$\beta = \mu C_{OX} \frac{W}{L} \qquad (2)$$

Using these expressions, we can determine the W/L of all mosfets in the circuit, since, as stated in the introduction: (i) the current in all mosfet is known if the bias current is given; (ii) the bias current is assigned.
In practice, it is more convenient to find the W/L of a chosen mosfet and then proceed to all other mosfets by simple proportionality rules. Let us suppose that the chosen mosfet is n-type and call it M_A. Then consider another mosfet M_B and call K_B the ratio: I_{DB}/I_{DA}.

Then:

$$\left(\frac{W}{L}\right)_B = \begin{cases} \left(\frac{W}{L}\right)_A K_B & \text{if } M_B \text{ is n-type} \\ \left(\frac{W}{L}\right)_A K_B \frac{\mu_n}{\mu_p} & \text{if } M_B \text{ is p-type} \end{cases}$$

Generally, if possible, it is convenient to start from an n-type mosfet and close it in diode configuration, biasing it with the quiescent current that it is expected to receive in the project. To do that, simply use the test circuit shown in Fig. 1.

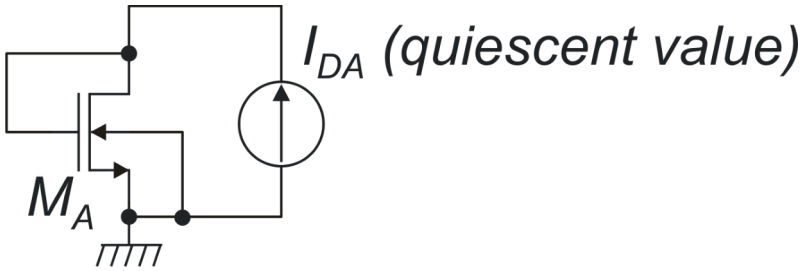

Fig. 1. Test circuit used to design the chosen reference mosfet M_A.

The current source value is set to the drain current that must flow through M_A in the quiescent (rest) condition, As a starting point, calculate the $(W/L)_A$ ratio using equations (1) and (2):

$$\left(\frac{W}{L}\right)_A^* = \frac{2I_D}{(V_{GS}-V_t)^2}\frac{1}{\mu C_{OX}} \qquad (3)$$

where V_{GS}-V_t is the target overdrive voltage (200 mV for the project purpose) and μC_{ox} is given in the process manual (DRM of PSM025 for the projects). The W/L estimate founds in this way has been marked by an asterisk, since it has generally to be adjusted. Indeed, the aspect ratio calculated in this way does not produce the desired V_{GS}-V_t, due to the poor accuracy of the mosfet square laws. To check this, set M_A in the circuit of Fig.1 with (W/L)* and run an operating point simulation (.op). Call (V_{GS}-V_t)* the value found in this way. This will be generally slightly different from our target value (200 mV). Refine the W/L ratio by using equations (1) and (2):

$$\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_A^* \left[\frac{(V_{GS}-V_t)^*}{(V_{GS}-V_t)}\right]^2 \qquad (4)$$

After this refinement, the obtained W/L generally produces a V_{GS}-V_t which is sufficiently close to the target value. For the aim of the project, we will consider that the target is obtained if the actual V_{GS}-V_t obtained by simulating the circuit of Fig.1 differs from the target by less than ± 20 mV.

2.3 Effects of changing the main circuit parameters

Most of the described circuit design choices are indicated to the students with no explanation. Among these choices there are: (i) the bias current; (ii) the mosfet length; (iii) equal overdrive voltage for all devices. In the next paragraphs, these choices are briefly reviewed in order to let the students know which circuit performances and trade-offs are related to the parameters involved.

Bias current.

Increasing the bias current produces the following advantages:

(a) The circuit gets faster. This is due to the fact that most circuit singularities (poles and zeroes) are proportional to g_{mi}/C_{pi} , where g_{mi} is the transconductance of i-th transistor, while C_{pi} is the

parasitic capacitance connected to its drain. If V_{GS}-Vt is fixed by design, the g_m can be conveniently expressed as: $g_{mi}=I_{Di}/V_{TEi}$ where I_{Di} and V_{TEi} are the drain current and equivalent thermal voltage of transistor M_i. Increasing the bias current, increases the quiescent current of all mosfet, shifting their singularities to higher frequencies. This is an approximate and rather qualitative approach, but is useful to understand the relationship between quiescent current and circuit speed.

(b) If we are dealing with an amplifier, the input referred thermal noise density gests smaller.

The drawback of increasing the current is mainly increased power consumption. Since this is an important parameter, a trade-off has to be made between the speed and input noise performance and power consumption.

Channel length (L)

Increasing the channel length produces the following advantages:

(a) Parameter λ decreases, improving the output resistances and then voltage gain of amplifiers. Current mirrors behave more ideally, since the output current depends less on the output voltage due to the increased output resistance.

(b) The gate area increases (if L is increased, also W should be increased of the same factor, to maintain the W/L ratio constant). This improves device matching (reducing amplifier input offsets) and reduces the flicker noise components.

The drawbacks of increasing the device length are clearly:

(a) Increased area occupation (circuit layouts gets bigger).

(b) Reduced speed: increased gate areas result in larger parasitic capacitances.

Overdrive voltages

We have chosen to set all overdrive voltages to the same value (200 mV in our case), except for those that are constrained to assume a particular value or meet a particular relationship. This choice is not optimal, since the overdrive voltages of different mosfets play different roles in determining the circuit behavior in terms of noise, offset and frequency response. For example, in most differential amplifier topologies, an optimal noise reduction is obtained when the overdrive voltage of the input differential pair(s) is minimized, while the overdrive voltage of mosfet in current mirrors is maximized. Such an analysis is beyond the aim of the PSM course, then we have chosen to equalize the V_{GS}-V_t in order to simplify device sizing. Furthermore, the choice of adopting a small overdrive voltage increases the input and output ranges and facilitates operation with small power supply voltages.

2.4 A method for providing independent common mode and differential mode input to a differential amplifier.

The following circuit can be used to explicitly set the common mode and differential mode voltages at the input of an amplifier:

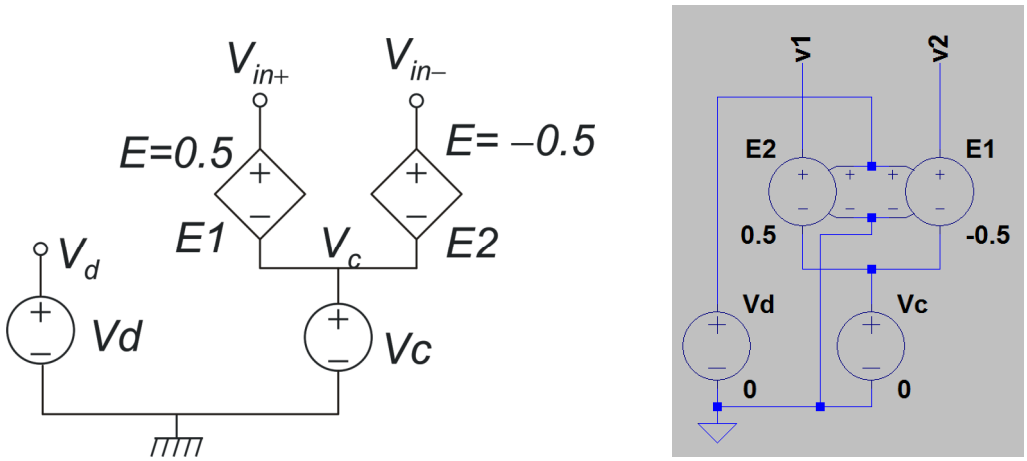

Fig. 2. A method to set the differential mode and common mode voltage by means of independent and dependent (controlled) generators. On the right, the LTSpice implementation is shown, where V_1 and V_2 are the non-inverting and inverting voltages, respectively.

The independent voltage sources indicated with V_d and V_c sets the differential mode and common mode voltage, respectively. The differential voltage produced by V_d, present at node V_d, is added to V_c by the dependent sources E1 and E2. The gain of the latter is set to 0.5 and -0.5, respectively, so that:

$$V_{in+} = V_c + \frac{V_d}{2}; \quad V_{in-} = V_c - \frac{V_d}{2} \qquad (5)$$

as required.