PSM 025-MM

Dual Metal 0.25 Micron CMOS Process
Mixed Mode version

Design Rule Manual (DRM)

For educational purpose only

1. Process description

The PSM025 is an *n*-well – single poly – double metal (1P2M) CMOS process with Al-BEOL (Aluminum Back End of Line). Minimum channel length for both *n*-MOS and *p*-MOS devices is 0.25 µm. Polysilicon and diffusions are silicided for sheet resistance reduction. Use of tungsten plugs allows stacking of vias and contacts.

2 General rules

- All dimensions in this manual are expressed in microns.
- All dimensions are absolute minima. Larger values should be used whenever possible. The only exception is represented by contacts and vias, which must be drawn at nominal values only.
- Notches are to be considered as spaces and should comply with the corresponding rules.
- Non-orthogonal lines are prohibited.
- The database must be digitalized on a 0.05-micron grid.

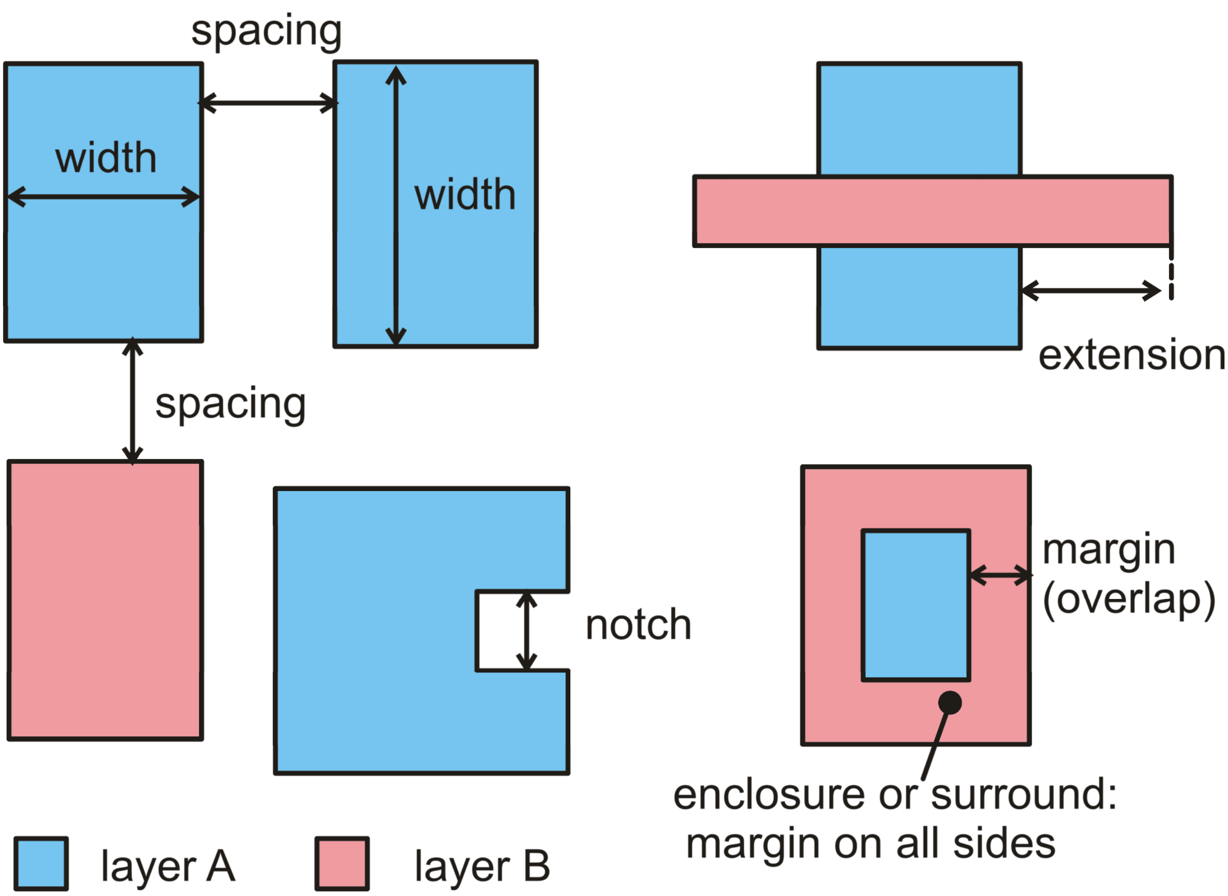
3. Tooling layers

Layer name	Description	GDS N.	Note
n-well	N-well implant	1	Standard
active	Active areas definition	2	Standard
poly	Polysilicon	3	Standard
n_plus	*n*+ implant	4	Standard
p_plus	*p*+ implant	5	Standard
contact	Contact layer for connecting Metal1 to Poly or Active	6	Standard
metal1	First metal interconnect layer (Al)	7	Standard
via	For contacting metal1 to metal2	8	Standard
metal2	Second metal interconnect layer (Al)	9	Standard
passivation	Passivation opening for bonding purposes	10	Standard
siprot	Silicide protection: inhibits silicide formation over active and poly	11	Optional
hires	Selects polysilicon areas with reduced doping for high value resistors	12	Optional
metal1_opt	Optional metal 1 layer for lower MIM capacitor plate	13	Optional

4. Topological Layout Rules (TLR)

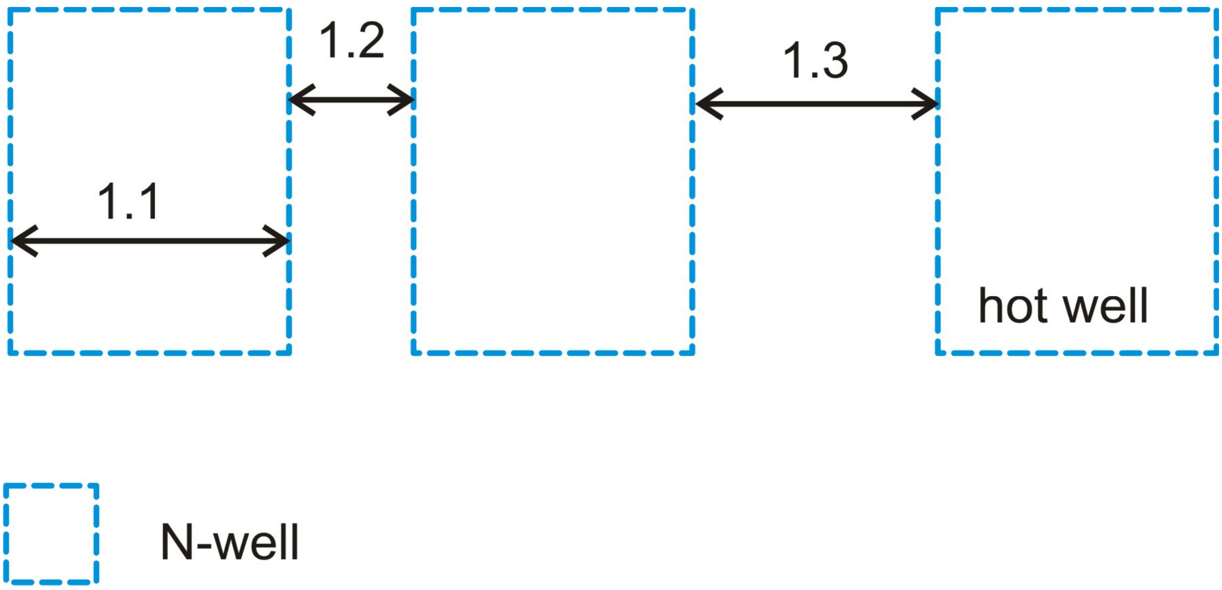
Conventions used in this manual: topological rule types.

- Width
- Spacing
- Margin or overlap (enclosure when on all sides)
- Extension



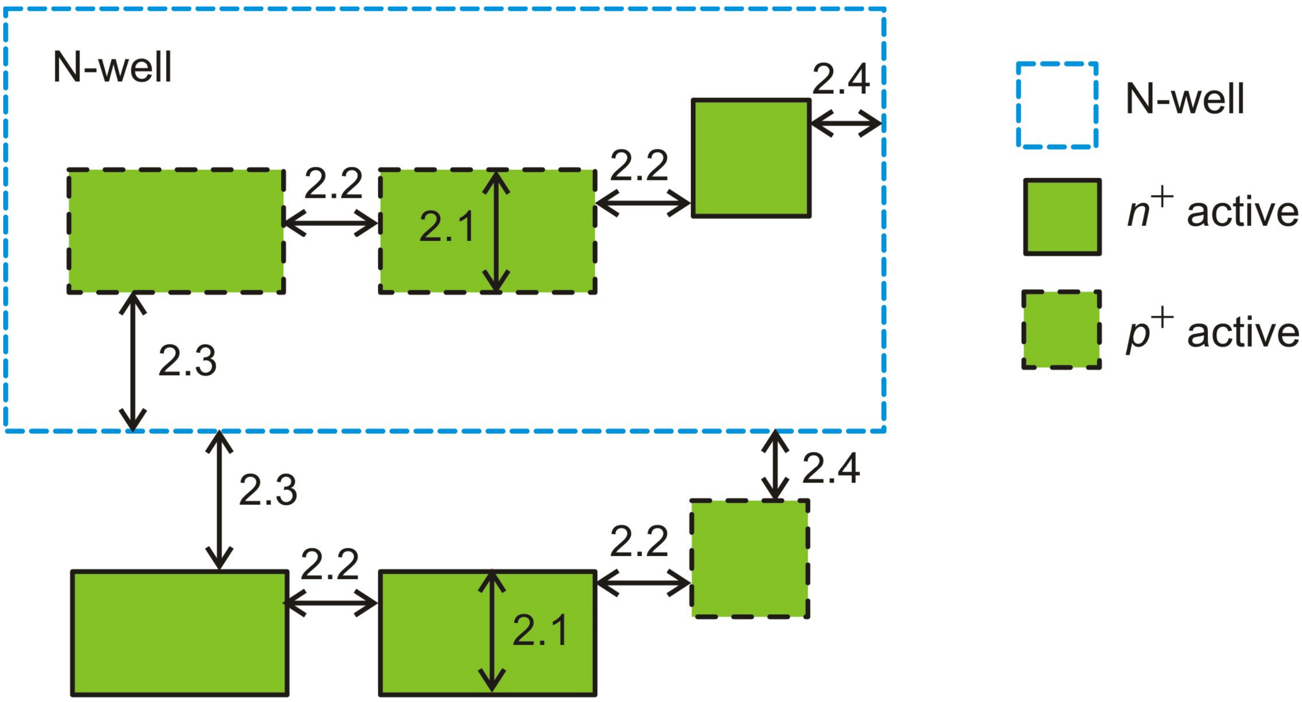
N-Well

Rule	Description	value (micron)
1.1	Minimum width	1.5
1.2	Minimum spacing between wells at same potential	1.0
1.3	Minimum spacing between wells at different potential (hot wells)	2.2



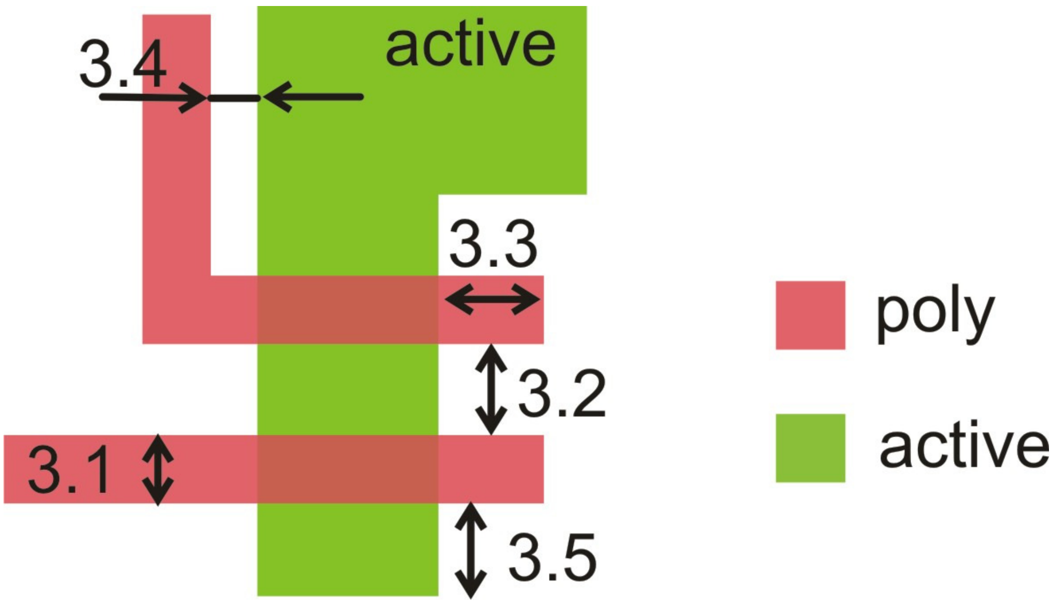
Active

Rule	Description	value (micron)
2.1	Minimum width	0.5
2.2	Minimum spacing	0.5
2.3	Source/drain active to well edge	0.8
2.4	Substrate/well contact active to well edge	0.5



Poly (polysilicon)

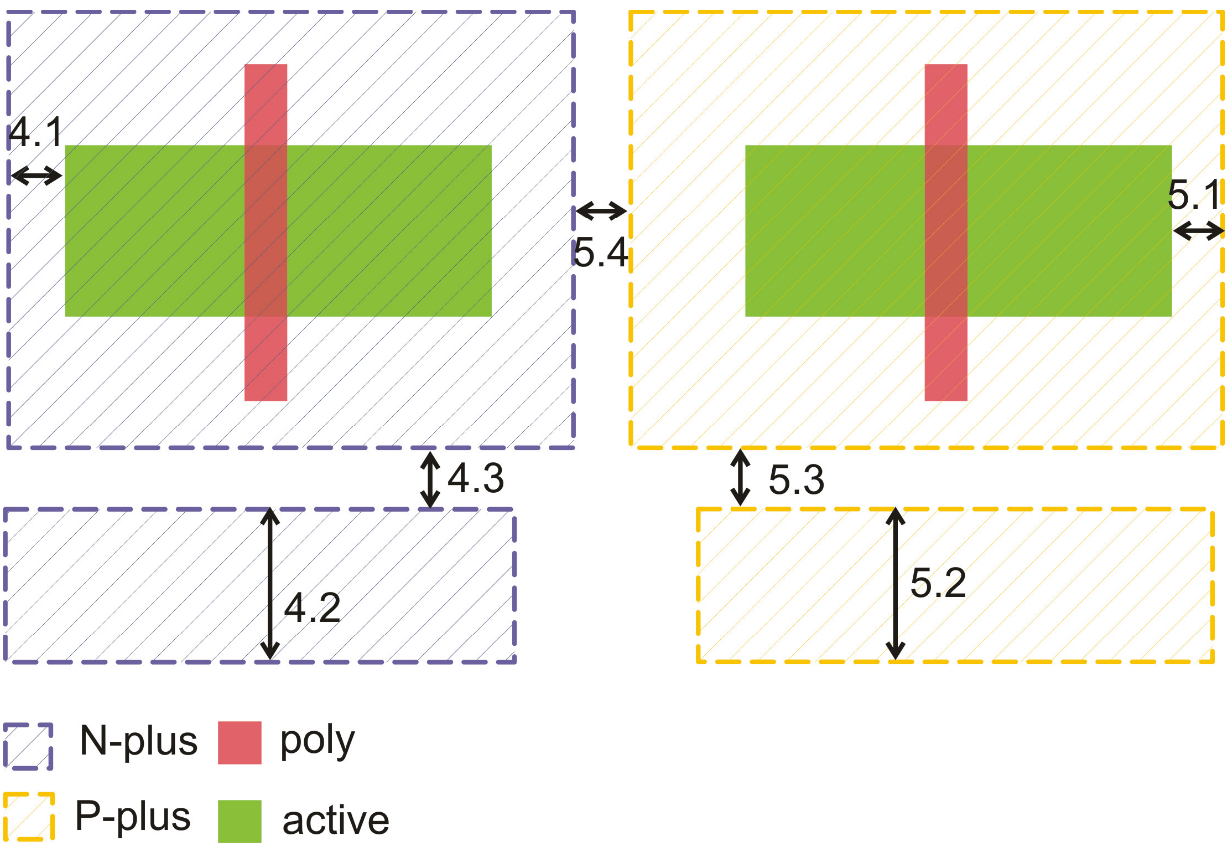
Rule	Description	value (micron)
3.1	Minimum width	0.25
3.2	Minimum spacing	0.5
3.3	Minimum gate extension of active	0.8
3.4	Minimum field poly to active spacing	0.2
3.5	Minimum active extension of poly	0.5



N-plus / P-plus Source/Drain implant

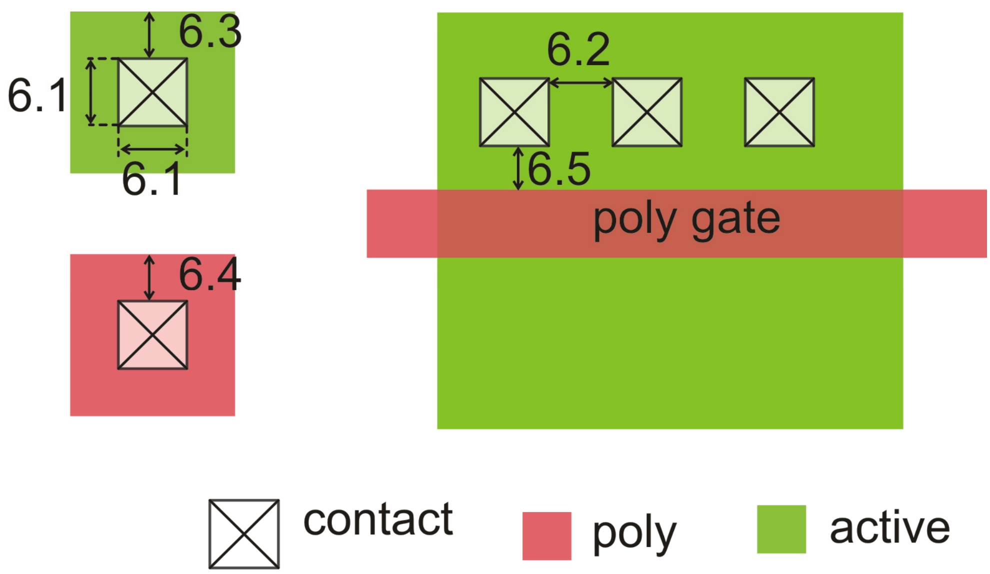
Rule	Description	value (micron)
4.1	Minimum N-plus overlap of active	0.3
4.2	Minimum N-plus width	0.5
4.3	Minimum N-plus spacing (merge whenever possible)..	0.5

Rule	Description	value (micron)
5.1	Minimum P-plus overlap of active	0.3
5.2	Minimum P-plus width	0.5
5.3	Minimum P-plus spacing (merge whenever possible)..	0.5
5.4	Minimum N-plus to P-Plus spacing	0.5



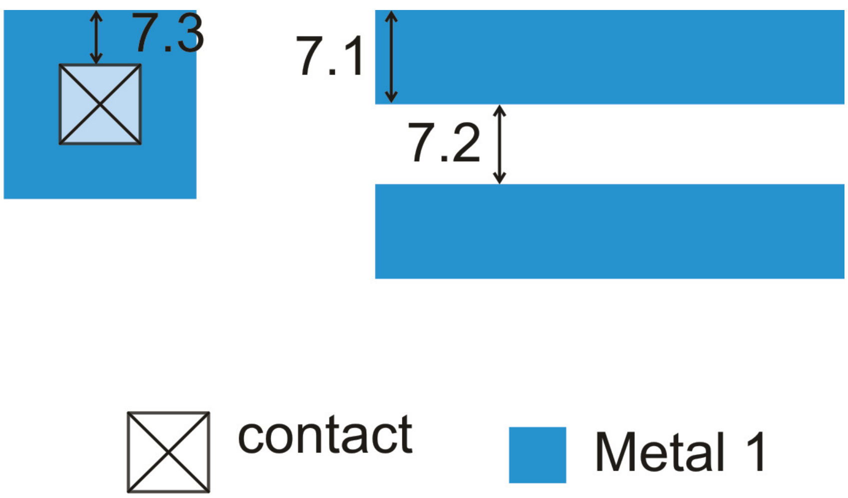
Contact

Rule	Description	value (micron)
6.1	Exact contact size	0.3
6.2	Minimum spacing	0.4
6.3	Minimum margin to active area	0.2
6.4	Minimum margin to polysilicon area	0.2
6.5	Minimum spacing to polysilicon gate	0.25



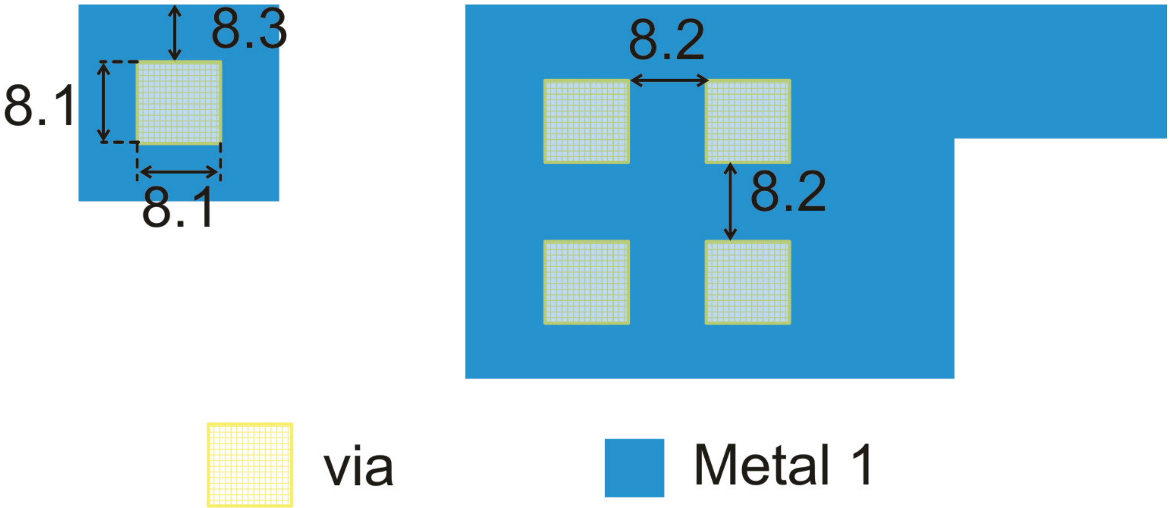
Metal 1

Rule	Description	value (micron)
7.1	Minimum width	0.5
7.2	Minimum spacing	0.5
7.3	Minimum overlap of contact	0.2



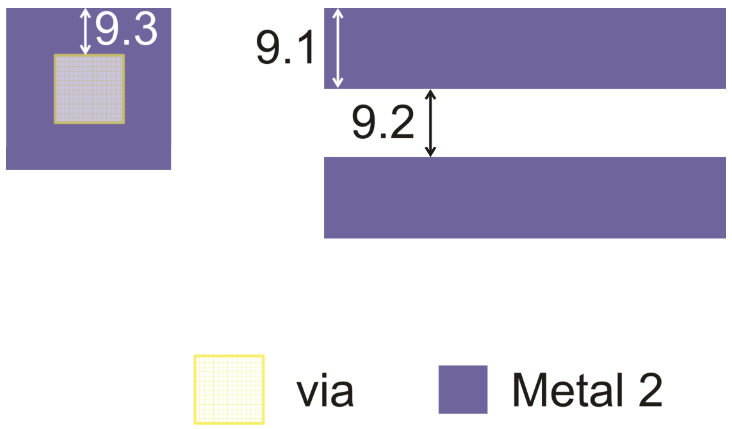
Via

Rule	Description	value (micron)
8.1	Exact via size	0.3
8.2	Minimum spacing	0.4
8.3	Minimum margin to metal 1	0.2
8.4	Stacking of vias and contacts is allowed	



Metal 2

Rule	Description	value (micron)
9.1	Minimum width	0.5
9.2	Minimum spacing	0.5
9.3	Minimum overlap of via	0.2



5. Latch-UP prevention rules

Core devices:

Rule	Description	value (micron)
20.1	Maximum distance between an n+ active area on substrate (n-mos source/drain diffusion) and the closest substrate contact (substrate tap)	25
20.2	Maximum distance between a p+ active area on n-well (p-mos source/drain diffusion) and the closest well contact (well tap)	25

Input/ output devices

NMOS I/O transistor.

Rule 20.3. A *p*+ guard ring covered by metal 1 and filled by as much as possible contacts should be placed around any single *n*-MOSFET. The guard ring should be connected to Vss.

Rule 20.4. An *n*+ collector guard ring, embedded into an *n*-well ring must be placed around the *p*+ guard ring. The *n*+ guard ring must be covered by metal 1 and filled by as much as possible contacts. The *n*+ collector guard ring should be connected to Vdd.

PMOS I/O transistor.

Rule 20.5. An *n*+ guard ring covered by metal 1 and filled by as much as possible contacts should be placed around any single *p*-MOSFET inside the n-well that includes the p-MOSFET. The guard ring should be connected to Vdd.

Rule 20.6 A *p*+ collector guard ring must be placed around the n-well that includes the p-MOSFET. The *p*+ collector guard ring must be covered by metal 1 and filled by as much as possible contacts. The *p*+ collector guard-ring must be connected to Vss.

6. Electromigration rules: current limits through interconnections and contacts.

Interconnections.
Linear current density (mA/µm)

Layer	Width (µm)	**I max at 80 °C (W in µm)**	I max at 100 °C (W in µm)	I max at 125 °C (W in µm)
Metal1	0.5 ≤ W ≤ 1	**1mA×(W+0.5)**	0.5 mA×(W+0.5)	0.3mA(W+0.33)
	W ≥ 1	**1.5 mA×W**	0.75 mA×W	0.4 mA×W
	W=0.5	**1mA**	0.5 mA	0.25 mA
Metal2	0.5 ≤ W ≤ 1	**1mA× (W+1)**	0.5mA× (W+1)	0.25mA× (W+1)
	W≥ 1	**2 mA/µm**	1 mA/µm	0.5 mA×W
	W=0.5	**1.5 mA**	0.75 mA	0.375 mA

Vias and contacts
Current for a single via / contact

Type	**80 °C**	100 °C	125 °C
Contact	**0.7 mA**	0.45 mA	0.3 mA
Via	**1 mA**	0.75 mA	0.5 mA

7. Mosfet electrical parameters

NMOS electrical parameters

Parameter	W /L (μm/ μm)	Min	**Typ**	Max
Vt	10 / 10	0.32 V	**0.38 V**	0.44 V
Vt	10 / 0.25	0.48 V	**0.53 V**	0.58 V
Vt	0.5 / 0.25	0.4 V	**0.45 V**	0.51 V
μ_nCox	10 / 10	180 x 10^{-6} A/V^2	**240 x 10^{-6} A/V^2**	280 x 10^{-6} A/V^2
γ (body effect factor)	10 / 10	-	**0.44 $V^{0.5}$**	-

PMOS electrical parameters

Parameter	size (W /L)	Min	**Typ**	Max
Vt	10 / 10	-0.48 V	**-0.56 V**	-0.64 V
Vt	10 / 0.25	-0.45 V	**-0.5 V**	-0.55 V
Vt	0.5 / 0.25	-0.4 V	**-0.44 V**	-0.5 V
μ_pCox	10 / 10	40 x 10^{-6} A/V^2	**50 x 10^{-6} A/V^2**	60 x 10^{-6} A/V^2
γ (body effect factor)	10 / 10	-	**0.6 $V^{0.5}$**	-

Matching parameters (Pelgrom area parameters)

Parameter	NMOS	PMOS
C_{Vt}	8.5 mV·μm	8.5 mV·μm
C_{β}	0.03 μm	0.03 μm

Parameters of parasitic devices

Resistances

Type	Unit	Min (Fast)	**Typ.**	Max. (Slow)
N-Well Sheet Resistance	Ohm/square	400	**500**	600
N+ / P +Sheet Resistance	Ohm/square	3.5	**5**	8.5
N+ Sheet Resistance (non salicide)	Ohm/square	65	**80**	100
P+ Sheet Resistance (non salicide)	Ohm/square	85	**120**	150
Poly Sheet Resistance	Ohm/square	3.0	**5.0**	8.0
Poly N+ Sheet Resistance (non salicide)	Ohm/square	80	**100**	135
Poly P+ Sheet Resistance (non salicide)	Ohm/square	155	**180**	205
HR Poly	Ohm/square	800	**1.0k**	1.2k
Metal 1 Sheet Resistance	Ohm/square	0.06	**0.08**	0.1
Metal 2 Sheet Resistance	Ohm/square	0.055	**0.065**	0.085
N+ /Metal 1 contact Resistance.	Ohm	5.0	**10**	20
P+ /Metal 1 contact Resistance	Ohm	5.0	**10**	20
Poly /Metal 1 contact Resistance	Ohm	4.0	**8.0**	12
Metal1 /Metal 2 Via resistance	Ohm	2.5	**5.0**	9.0

Capacitances

Mosfet Capacitances

Type	Unit	Min (Fast)	**Typ.**	Max. (Slow)
Gate to substrate / Gate to well (area)	fF/μm^2	5.5	**6.0**	6.5
N+ / Substrate (area)	fF/μm^2	1.66	**1.85**	2.05
N+ / Substrate (edge)	fF/μm	0.35	**0.38**	0.42
P+/Well (area)	fF/μm^2	1.7	**1.9**	2.1
P+/Well (edge)	fF/μm	0.36	**0.39**	0.43

Interconnect Relateted Capacitances

Type	Unit	Min (Fast)	**Typ.**	Max. (Slow)
Poly to substrate (area)	fF/μm^2	0.09	**0.1**	0.11
Poly to substrate (fringe)	fF/μm	0.075	**0.08**	0.09
Metal 1 to substrate (area)	fF/μm^2	0.027	**0.03**	0.033
Metal 1 to substrate (fringe)	fF/μm	0.035	**0.04**	0.045
Metal 1 to Poly (area)	fF/μm^2	0.053	**0.06**	0.065
Metal 1 to Poly (fringe)	fF/μm	0.059	**0.065**	0.071
Metal 2 to substrate (area)	fF/μm^2	0.012	**0.015**	0.018
Metal 2 to substrate (fringe)	fF/μm	0.063	**0.07**	0.078
Metal 2 to Poly (area)	fF/μm^2	0.025	**0.03**	0.035
Metal 2 to Poly (fringe)	fF/μm	0.072	**0.08**	0.088
Metal 2 to Metal 1 (area)	fF/μm^2	0.035	**0.04**	0.045
Metal 2 to Metal 1 (fringe)	fF/μm	0.054	**0.06**	0.066