6) Means for storing the personality of the repaired chip must be provided.

Acknowledgment

The helpful discussions with D. L. Critchlow, R. H. Dennard, and L. M. Terman and their contributions to the 16K design are appreciated.

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A Charge-Oriented Model for MOS Transistor Capacitances

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***Abstract*—A new model for computer simulation of capacitance effects in MOS transistors is presented. Transient currents are found directly from the charge distribution in the device rather than from capacitances. The effective capacitances which result are nonreciprocal. The model guarantees conservation of charge and includes bulk capacitances. Several circuit examples are considered.**

Introduction

THE successful computer simulation of MOS circuits requires an accurate model for transistor capacitances. While use of average capacitance values may suffice for some devices or circuits, it is usually necessary to consider the variation of capacitance with voltage. A model which does this was developed by Meyer [1], and is used in many modern circuit simulators. While this model works well for most cases, it is inadequate for use with some newer device and circuit technologies. In particular, it fails for circuits in which charge storage is important. Such is the case for many dynamic and silicon-on-sapphire (SOS) circuits. A model to handle circuits in which charge is more important than capacitance will be presented here.

Manuscript received December 8, 1977; revised June 2, 1978. This work was initially supported by Hewlett-Packard Corporate Engineering and received continuing research support from the Advanced Research Projects Agency under Contract DAA-B07-C-1344. The work of one of the authors was supported by an NSF Fellowship.

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The Conventional Model

Meyer's model is shown in Fig. 1. Three nonlinear capacitors are defined in terms of the total gate charge Q_G:

$$C_{GD} \triangleq \frac{\partial Q_G}{\partial V_D} \quad C_{GB} \triangleq \frac{\partial Q_G}{\partial V_B} \quad C_{GS} \triangleq \frac{\partial Q_G}{\partial V_S}. \tag{1}$$

The current through each capacitor is computed from

$$i = C(V_0)\frac{dV}{dt} \tag{2}$$

where the capacitance has been evaluated at some appropriate voltage V_0.

Several problems can occur with this model, the most important being the omission of source-bulk and drain-bulk capaci-

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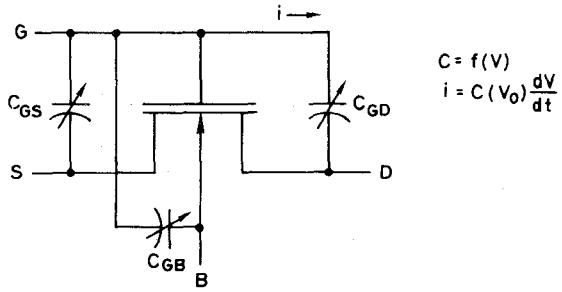

Fig. 1. Meyer model.

tances. These problems lead to a nonconservation of charge (charge pumping) in which the charge stored in a node is not equal to the integrated net current flowing into the node. Discontinuities in the capacitance functions can also cause instabilities in the Newton-Raphson iteration procedure.

The Charge-Oriented Model

The proposed model is based on the actual charge distribution in the MOS structure (Fig. 2). For any region of space we can write

$$i = \frac{dQ}{dt}$$

where i is the net current flowing into the region and Q is the total charge contained in the region. Thus, we can write

$$i_G = \frac{dQ_G}{dt} \qquad i_B = \frac{dQ_B}{dt} \qquad i_S + i_D = \frac{d(Q_S + Q_D)}{dt}. \tag{3}$$

For use in a circuit simulator we integrate these equations:

$$\int_{t_0}^{t_1} i\,dt = Q(t_1) - Q(t_0). \tag{4}$$

In general, Q is a complex function of time. The problem is simplified by assuming that the charge at any time is determined by the terminal voltages at that instant. Then Q can be determined from steady-state conditions.

Any theory of MOS transistor operation which predicts the total gate and bulk charges can be used to find Q_G, Q_B, and $Q_S + Q_D$. The results given here are based on the simple theory of Ihantola and Moll [2]. More sophisticated treatments such as that of Sah and Pao [3] would give more accurate results, but are not suited for use in circuit simulators because of their complexity. Gate and bulk charges are calculated from the one-dimensional Poisson equation applied perpendicular to the surface. Channel charge is computed from

$$Q_C = -(Q_G + Q_B) \tag{5}$$

and is related to the source and drain charges:

$$Q_C = Q_S + Q_D. \tag{6}$$

Unfortunately, the drain and source charges are not as well defined as the gate and bulk charges and must be obtained by partitioning the channel charge. The present model uses

$$Q_S = Q_D = \tfrac{1}{2}Q_C. \tag{7}$$

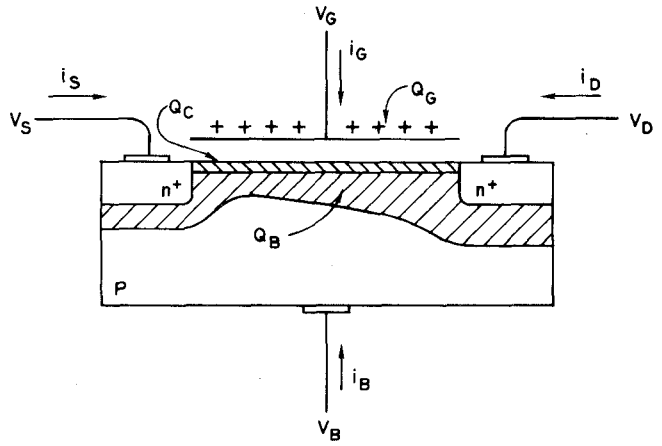

Fig. 2. Charge-oriented model.

The partitioning of channel charge will be considered in more detail later. Note that gate overlap and substrate junction capacitances should be included in addition to the "intrinsic" charge discussed here.

Equations (3) and (4) are used to relate voltage and current as follows. Let subscripts denote timepoints and superscripts denote Newton-Raphson iteration numbers. Thus, we have

V_0 = voltage at last timepoint (known)
V_1^0 = voltage at previous iteration, this timepoint (known)
V_1^1 = voltage at next iteration, this timepoint (unknown).

From (4)

$$\frac{h}{2}(i_1^1 + i_0) = Q_1^1 - Q_0, \qquad h \triangleq t_1 - t_0 \tag{8}$$

where the integral of current has been approximated by a trapezoidal integration formula.

Expanding $Q_1^1(V)$ about V_1^0,

$$Q_1^1(V) \approx Q_1^0 + \sum_x \left.\frac{\partial Q}{\partial V_x}\right|_{V_x = V_{x1}^0} (V_{x1}^1 - V_{x1}^0). \tag{9}$$

The subscript x takes the values "D," "G," "S," and "B," denoting one of the terminals. Thus,

$$\frac{h}{2}(i_1^1 + i_0) = (Q_1^0 - Q_0) + \sum_x \left.\frac{\partial Q}{\partial V_x}\right|_{V_x = V_{x1}^0} (V_{x1}^1 - V_{x1}^0). \tag{10}$$

This equation for i_1^1 can be substituted into the nodal admittance matrix to obtain a solution V_{x1}^1.

It is clear that in this model charge is conserved since it is computed directly from the voltages. Convergence problems are minimized by complete linearization of (4). The inclusion of an equation for the bulk ensures that capacitance effects associated with the bulk will be modeled.

It is convenient to define the capacitances

$$C_{yx} \triangleq \frac{\partial Q_y}{\partial V_x}. \tag{11}$$

Note that there are two capacitances between each pair of terminals. Thus, for example, we have $C_{GB} = \partial Q_G/\partial V_B$ and

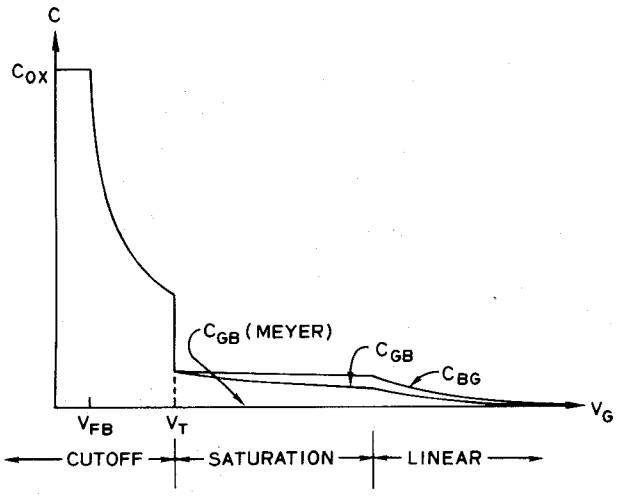

Fig. 3. Gate-bulk capacitances.

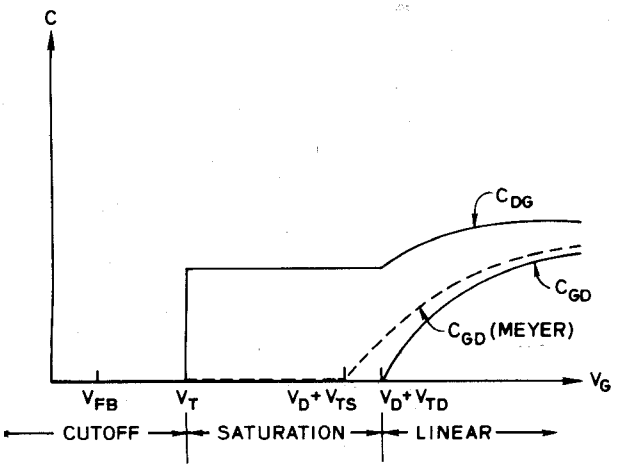

Fig. 4. Gate-drain capacitances.

$C_{BG} = \partial Q_B/\partial V_G$ between gate and bulk. These cannot be represented by a normal, two-terminal, reciprocal capacitor since, in general, $C_{yx} \neq C_{xy}$. As an example, C_{GB} and C_{BG} are plotted as functions of gate voltage in Fig. 3. It is apparent that the present model differs substantially from that of Meyer.

The Meyer model defines C_{GD}, C_{GB}, and C_{GS} in the same manner as the present model, but assumes that $C_{DG} = C_{GD}$, $C_{BG} = C_{GB}$, and $C_{SG} = C_{GS}$. Also, a simpler form for bulk charge is assumed. Thus, as shown in Fig. 3, the gate-bulk capacitance for the Meyer model is zero above V_T, while it can be seen that the charge model gives capacitances which are significant.

Fig. 4 compares C_{GD} and C_{DG} for the charge model and that of Meyer. Here we can readily see a physical basis for the difference between C_{GD} and C_{DG} in saturation. C_{GD} describes the effect of the drain on the gate (a feedback effect). In saturation, the drain voltage is isolated from the channel by the pinchoff condition and cannot affect the gate charge. Thus, C_{GD} is zero. A change in gate voltage, however, will produce a change in channel charge. Some of this change in charge will come about through a drain current. Thus, C_{DG}, which describes the effect of gate voltage on drain charge (a feedforward effect), will not be zero. Fig. 4 also shows C_{GD} for the Meyer model. Although similar to C_{GD} of the charge

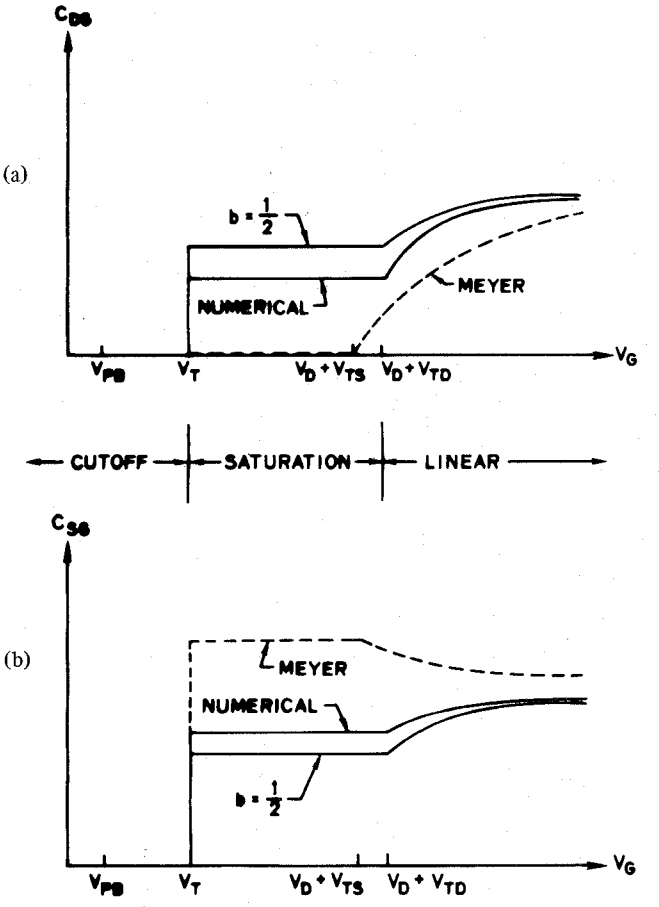

Fig. 5. (a) Drain-gate and (b) source-gate capacitances.

model, the threshold voltage at the drain is computed from the bulk charge at the source.

In order to find the drain and source currents from (3), we must have an algorithm for partitioning Q_C into Q_D and Q_S. This splitting may be done in several ways.

1) Divide the channel physically at some $y_0 = aL$ where L is the channel length. Then take

$$Q_S = \int_0^{y_0} \frac{dQ_C}{dy}\,dy \quad \text{and} \quad Q_D = \int_{y_0}^{L} \frac{dQ_C}{dy}\,dy. \tag{12}$$

Thus, the charge to the source side of y_0 goes into Q_S and the charge on the drain side goes into Q_D. Then $y_0 = aL$ can be found by the following.

a) Take a = constant.

b) Take y_0 as the point where the surface potential is some constant fraction of the drain-to-source voltage.

c) Calculate the transient current in the channel $\delta I(y)$ due to a change in a terminal voltage V_x. Take y_0 so that $\delta I(y_0) = 0$. This gives the exact terminal currents. The point y_0 varies with bias and depends on which voltage V_x is changed.

d) Take $a = y_0/L$ as any empirical function of the terminal voltages.

2) Divide the channel charge mathematically, take $Q_D = bQ_c$, $Q_S = (1 - b)\,Q_c$, and $0 \leqslant b \leqslant 1$. In general, b may be a function of the terminal voltages. In this case, $\partial Q_D/\partial V_x =$

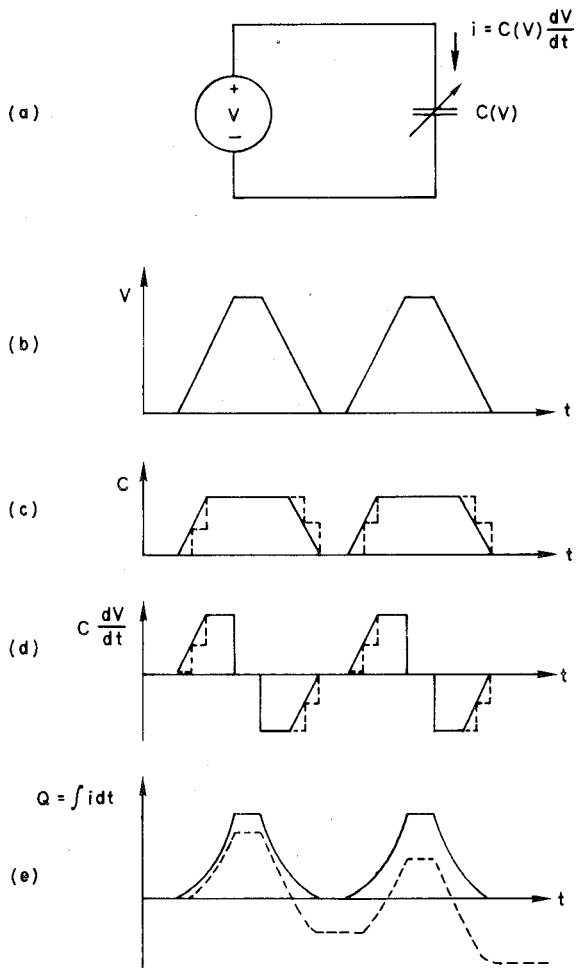

Fig. 6. Circuit showing nonconservation of charge.

$b(\partial Q_C/\partial V_x) + Q_C(\partial b/V_x)$. Thus we must take derivatives of b. The method chosen was method 2) with $b = \frac{1}{2}$.

Although model 1c) gives the exact capacitances, it is difficult analytically. The method was used in a numerical analysis to find the capacitances C_{DG} and C_{SG}. These are compared with the results using method 2), $b = \frac{1}{2}$, and with the Meyer model in Fig. 5. Thus the charge model assigns half the channel charge in saturation to the source and half to the drain, while the Meyer model assigns all the charge to the source. The exact result assigns $\frac{3}{5}$ of the channel charge to the source and $\frac{2}{5}$ to the drain.

Examples

Several examples which illustrate the importance of the charge-oriented model applied in circuit simulation are now considered. Fig. 6(a) shows a nonlinear capacitance driven by the voltage waveform of Fig. 6(b). Fig. 6(c) shows the capacitance as a function of time. The Meyer model approximates this capacitance by the stairstep shown in the dotted line. The size of the step depends on the timestep h used in the simulation. The current entering the capacitor is shown in Fig. 6(d). Note that in the simulated (dotted) waveform, more current flows out of the capacitor than flows in. This represents a charge loss, as shown in Fig. 6(e). In many practical circuits, this charge loss would result in a voltage error.

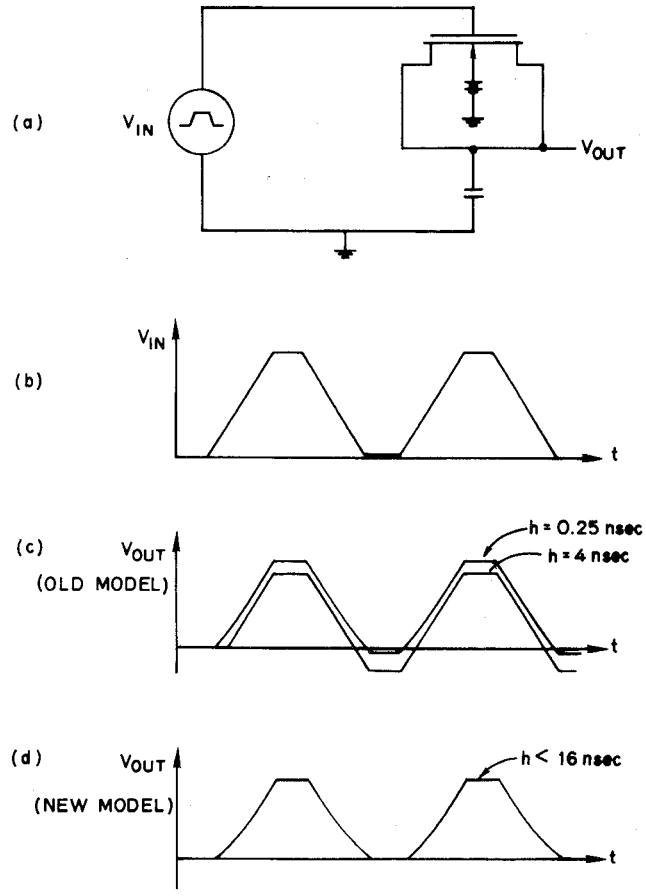

Fig. 7. Bootstrap circuit.

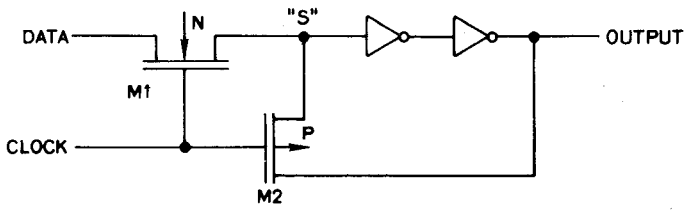

Fig. 8. Circuit of SOS flip-flop.

Fig. 7(a) shows a more realistic version of the previous example. In this bootstrap circuit, the variable capacitor has been replaced by the gate-source and gate-drain capacitance of an MOS transistor, and a load capacitance was added. The simulated output using the Meyer model is shown in Fig. 7(c). Note that the dc levels are in error by several volts. Also, the result depends on the timestep used. Even with 64 timesteps in the risetime of the input, the output is in error by 0.5 V after two cycles. As seen in Fig. 7(d), the charge-oriented model gives accurate dc levels even for a timestep equal to the risetime of the input. Thus, we can greatly reduce simulation time while maintaining increased accuracy.

Fig. 8 is the circuit of a D-type latch fabricated with CMOS-on-sapphire technology. When the clock goes high, $M2$ turns off, breaking the feedback path, and the input data are connected to the inverter pair through $M1$, an n-channel, floating-bulk device. When the clock again goes low, $M1$ turns off and $M2$ turns on, latching the data.

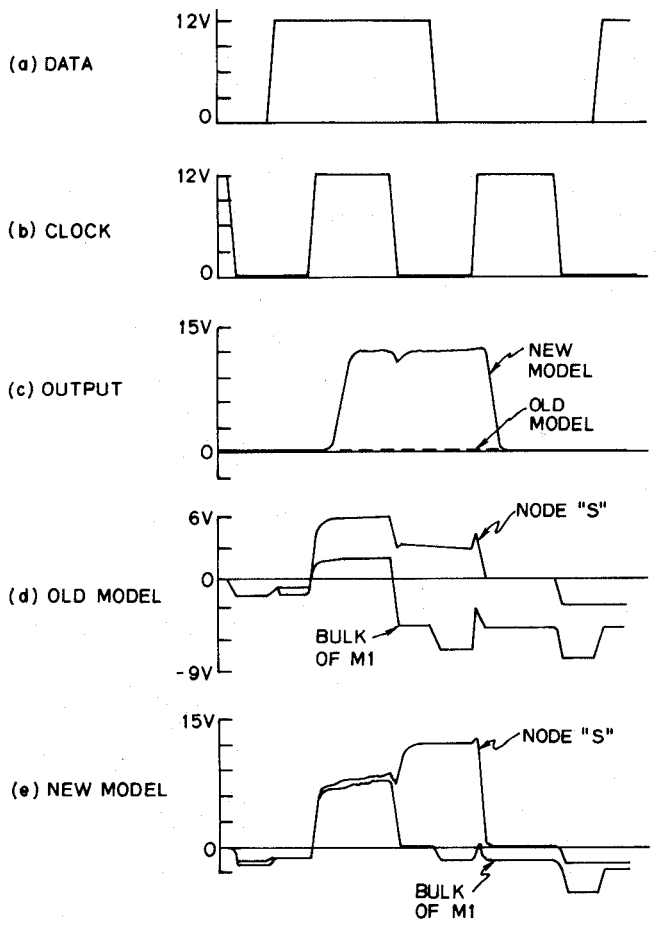

Fig. 9. Waveforms for circuit of Fig. 8.

Fig. 9(c) shows the output of a simulation for the inputs of Fig. 9(a) and (b). According to the old model, the output never goes high. The results predicted by the new model are correct.

The discrepancy is due to the difference in capacitance models during the rising clock. Fig. 10(a) shows the Meyer model for $M1$ at this time. The bulk is coupled to node "S" through a capacitive divider chain consisting of the junction capacitances C_{JSB} and C_{JDB}. Fig. 9(d) shows that while the bulk of $M1$ follows node "S" to some extent, a back-bias of 5 V still develops to turn off the device. An approximate equivalent circuit using the new model, Fig. 10(b), has two more capacitances in the divider network. The bulk-gate capacitance C_{BG} couples the rising clock signal to the bulk, while the bulk-source capacitance C_{BS} couples the bulk to node "S." The result, seen in Fig. 9(e), is that only 1 V of back-bias is produced and node "S" rises to a voltage capable of setting the latch.

Conclusions

A model for MOS capacitance which is based on charge has been presented. It is shown that the capacitive effects cannot be modeled by simple capacitors, but that nonreciprocal elements are required. Thus, while a change in drain voltage in saturation cannot affect the gate, a change in gate voltage will cause a drain current. Numerical results indicate that this gate-to-drain capacitance accounts for $\frac{2}{5}$ of the total gate-to-channel capacitance in saturation. The model is especially suited to circuits where charge conservation is important, such as in dynamic and SOS circuits. Examples have been given for which the charge-oriented model gives correct results, while the conventional model is inadequate.

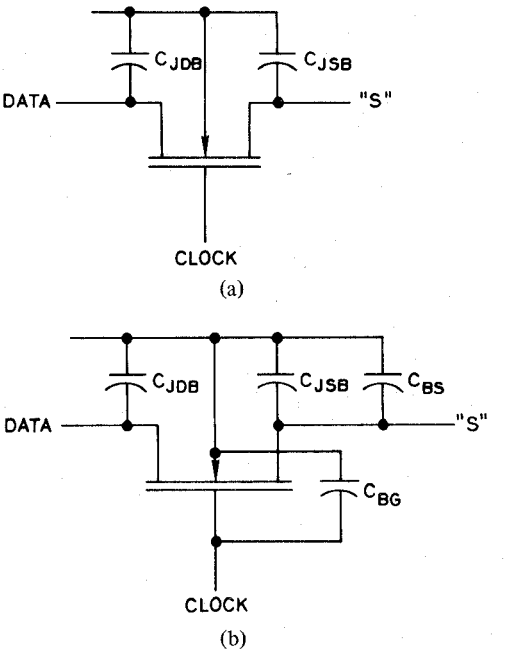

Fig. 10. Meyer and charge representations for $M1$ of Fig. 8.

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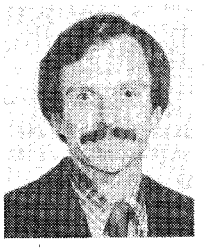

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Special Correspondence

An 8 mm^2, 5 V 16K Dynamic RAM Using a New Memory Cell

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Abstract—A small 16K dynamic RAM utilizing a new memory cell configuration is described. The new cell has two selector transistors and makes a very short bit line possible. The memory on 8 mm^2 is built in a scaled double polysilicon technology with 3.5 μm line width. First samples achieved an access time of 160 ns.

I. Introduction

To date two technologies are prime candidates for the fabrication of 65K RAM's—the double polysilicon technology [1] and the VMOS technology [2].

In this paper a very small 16K RAM in double polysilicon technology is described which can be quadrupled to build a 65K RAM not much larger than some 16K dynamic memories now on the market. This realized 16K RAM has a chip size of only 8 mm^2 and uses supply voltages of +5 and −5 V. First experimental samples achieved an access time of 160 ns.

The high performance of this memory was achieved by utilizing a new memory cell configuration in conjunction with a slightly scaled technology. This advanced technology uses 3.5 μm line width and spacing, a gate oxide thickness of 60 nm, arsenic implantation for shallow diffusions, and a high-ohmic substrate (20 Ω · cm). The following sections will describe the new memory cell, the design and operation features of the memory, as well as the first experimental results.

II. Memory Cell

The size of the storage capacitor of a memory cell is, among other parameters, mainly determined by the magnitude of the signal on the bit line, which must be higher than the sensitivity of the sense/refresh amplifier. The signal magnitude is often expressed as a ratio of storage capacitance C_S to the bit line capacitance C_B. The specific bit line capacitance C_B is determined by the lithography and technological parameters (line width, substrate doping), whereas the total value of C_B is strongly determined by the number of storage cells and the length of the bit line per cell. For a small memory cell, therefore, a short bit line is a prerequisite. The new memory cell shown in Fig. 1 leads to very short bit lines. The cell is basically a single transistor cell [3] with an additional selector transistor. Because of this additional transistor, cells sharing the same word line *WL* can therefore be placed vis-à-vis the bit line *BL*. The word line *WL* is connected to the selector transistors T_2

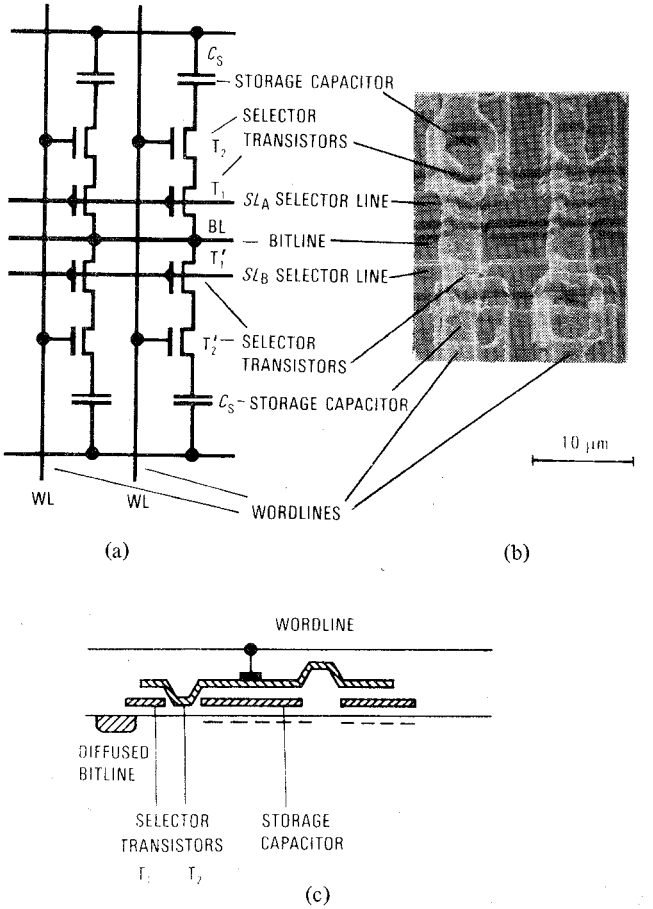

Fig. 1. (a) Circuit configuration. (b) SEM micrograph. (c) Cross section of the new memory cell.

Manuscript received April 5, 1978; revised May 31, 1978. This work was supported by the Technical Program of the Federal Department of Research and Technology of the Federal Republic of Germany. The authors alone are responsible for the contents.

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