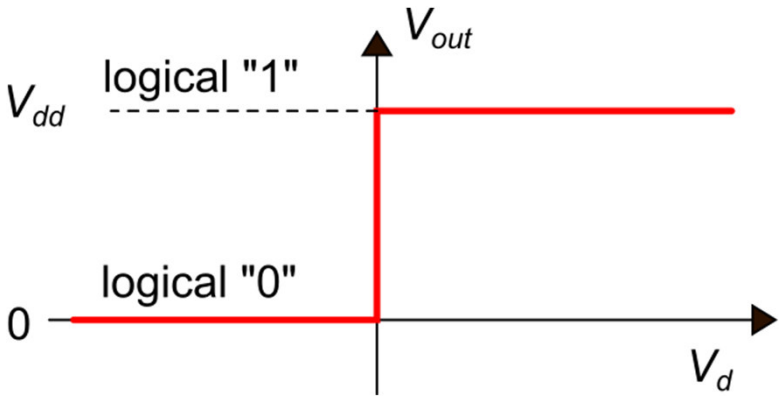
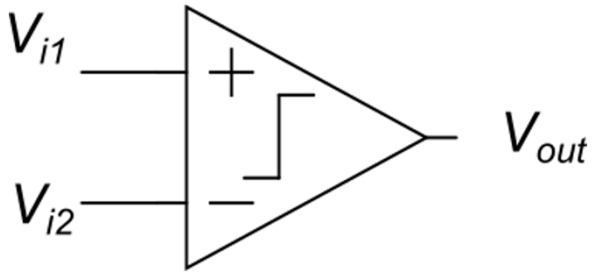
Comparators



$$V_d = V_{i1} - V_{i2}$$

ideal response



Symbol

$$V_{out} = \begin{cases} \text{"0" if } V_d \le 0 \\ \text{"1" if } V_d > 0 \end{cases}$$

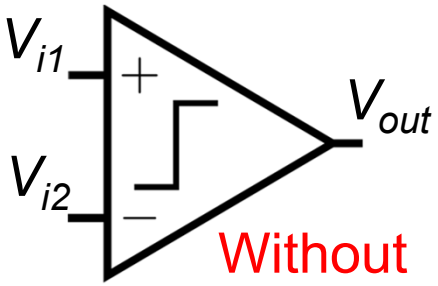
Continuous-time vs dynamic comparator

Continuous-time comparator:

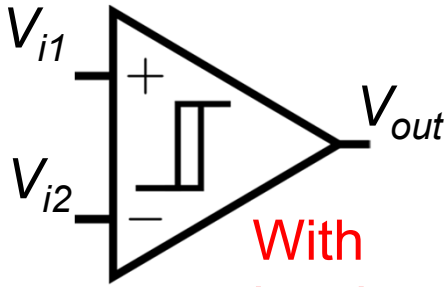
- Higher power consumption
- Hystheresis
- Output always valid

Dynamic comparator (or latched comparator):

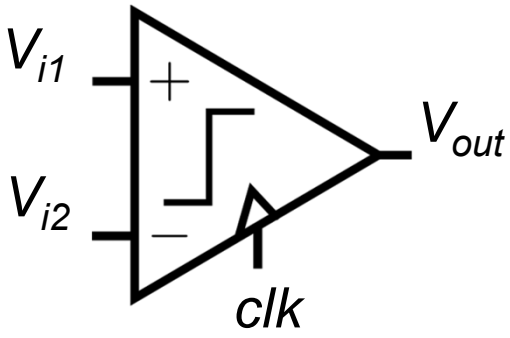
- Lower power consumption
- No hysteresis
- Need a clock signal



Without hystheresis

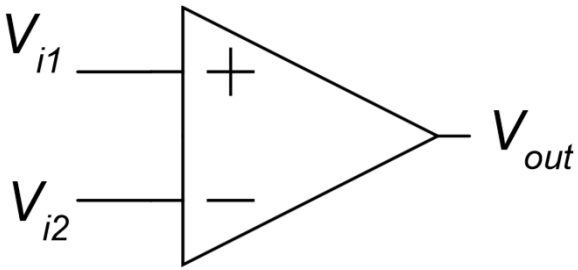


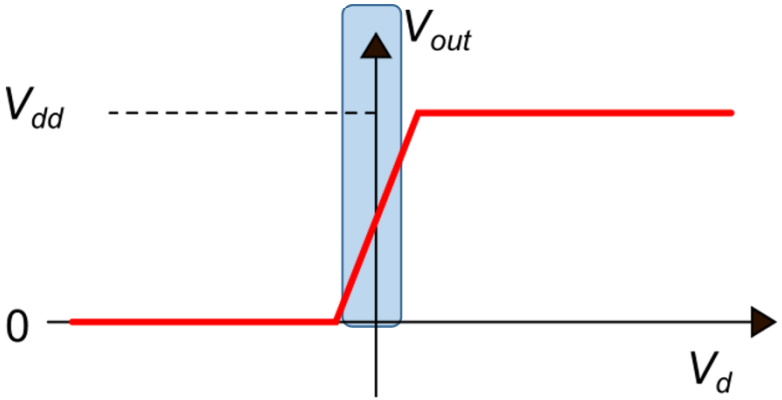
With hystheresis



Comparators: amplifier-based implementations

An amplifier with very high gain can be used as a comparator. Op-amp topologies can be used with no need of frequency compensation since the comparator is used in open loop configuration or positive feedback.



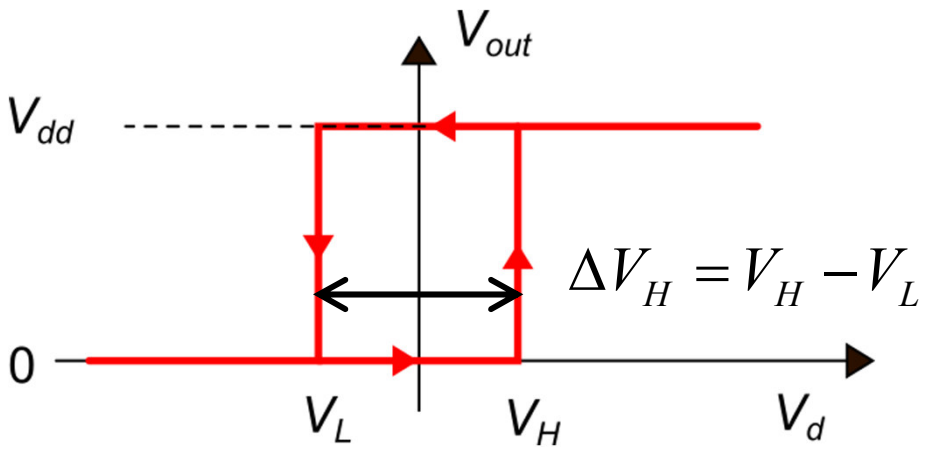


Note:

a region exists where the logical level is undefined

In several application this may lead to unwanted stable or metastable states. For slow-varying signals, threshold crossing may be too noisy

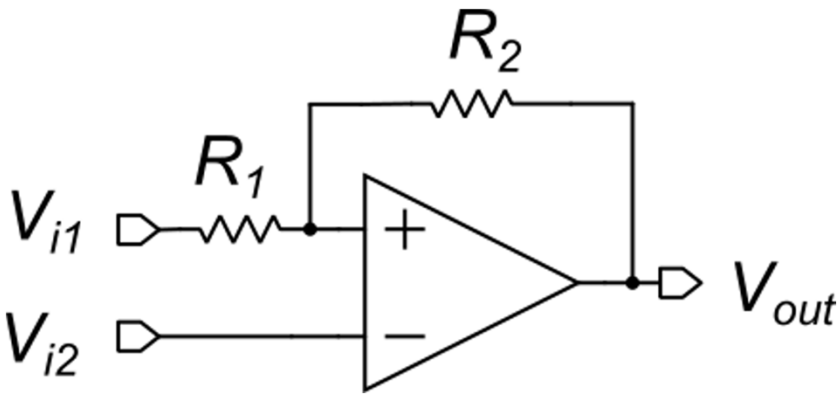
Regenerative comparators: hysteresis



Thanks to the hysteresis, the comparator produces a valid output level across the whole input range

The hysteresis introduces an uncertainty band that reduces the accuracy but helps rejecting noise when the input voltage is close to zero.

Possible regenerative comparator



Op-amp based Smith trigger.

Drawbacks

- Oversized solution for integrated cells
- Low impedance on the non-inverting input

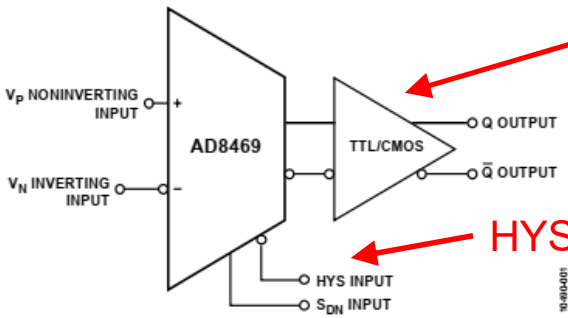
Commercial products

ANALOG DEVICES

Fast, Rail-to-Rail, Low Power, 2.5 V to 5.5 V, Single-Supply TTL/CMOS Comparator

Data Sheet **AD8469**

FUNCTIONAL BLOCK DIAGRAM



The digital output has its own V_{dd}

HYS input

Figure 1.

Programmable hysteresis from 0 to 160 mV

ΔV_h depnding on current on pin HYS

Input common-mode voltage: V_{EE} – 0.2 V to V_{CC} + 0.2 V

Low glitch TTL-/CMOS-compatible output stage

40 ns propagation delay

TEXAS INSTRUMENTS

TLV9022, TLV9032, TLV9024, TLV9034

SNOSDA3B – JUNE 2020 – REVISED NOVEMBER 2020

TLV902x and TLV903x High-Precision Dual and Quad Comparators

- Rail-to-Rail input with fault-tolerance
- 100ns Typ propagation delay

No built-in hysteresis. The datasheet suggests Schmitt trigger configuration

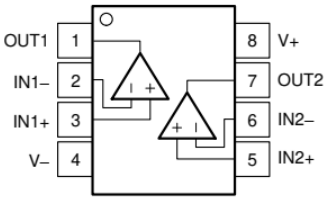
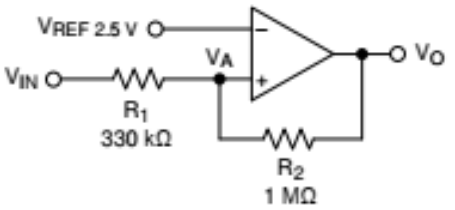
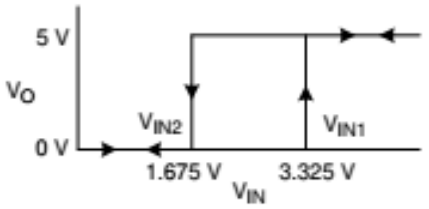


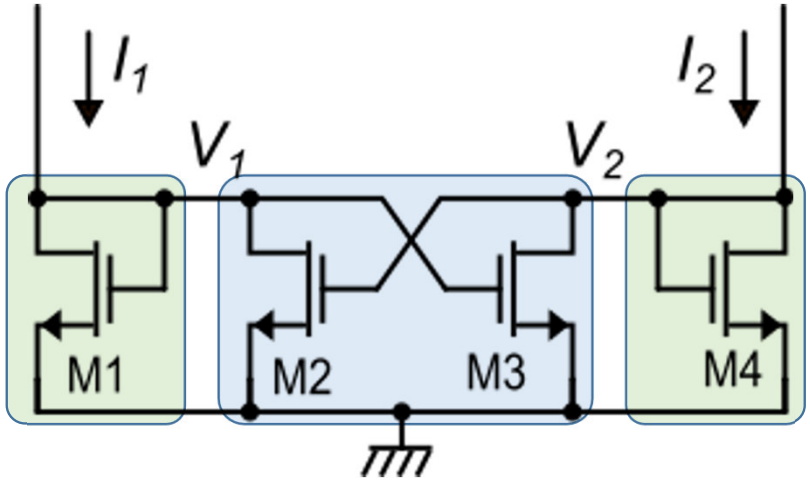
Figure 5-1. D, DGK, PW, DDF Packages 8-Pin SOIC, VSSOP, TSSOP, SOT-23-8 Top View





Compact comparator cell for Systems on a Chip

Four-transistor hysteresis cell

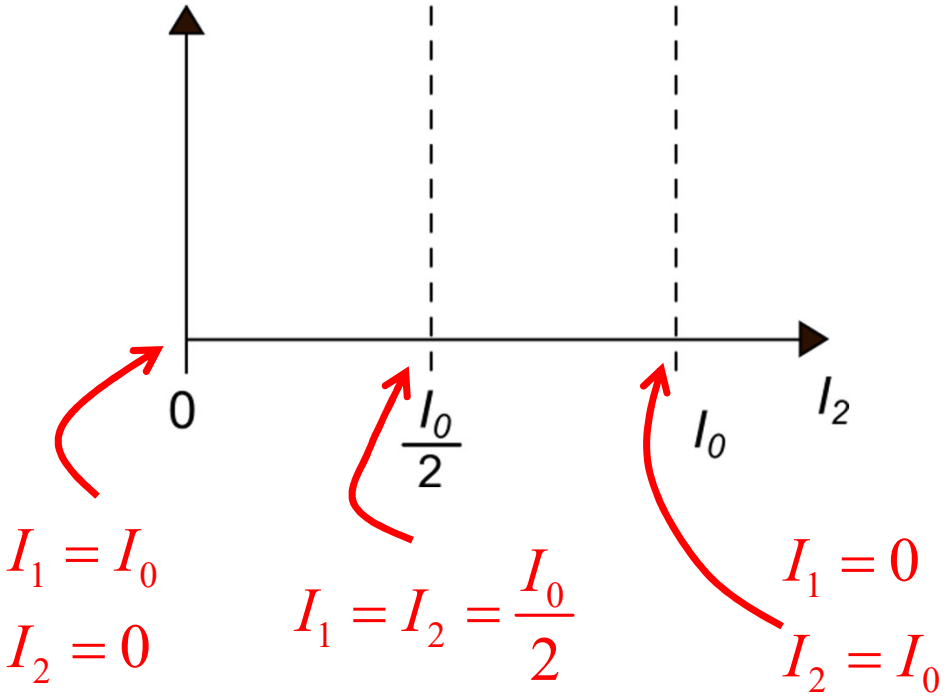


Load MOSFET $\beta=\beta_L$

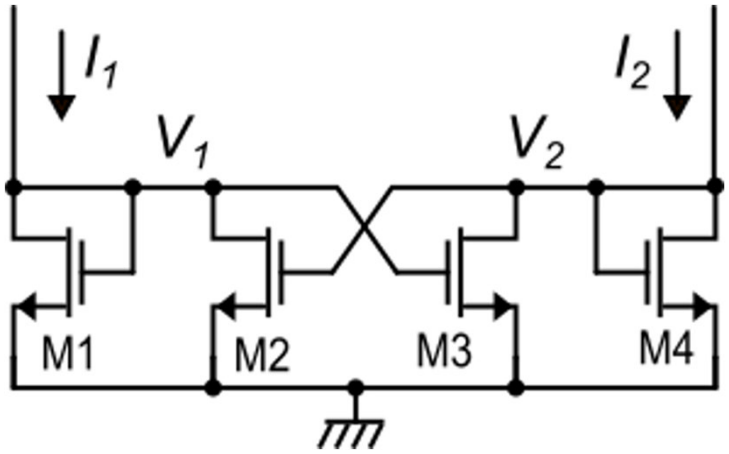
Cross-coupled MOSFETs $\beta=\beta_C$

Load MOSFET $\beta=\beta_L$

Currents I_1 and I_2 varies with the input signal in such a way that: $I_1 + I_2 = I_0 = constant$



Analysis of the four-transistor hysteresis cell: starting point



Let us start from: I_2=0 (I_1=I_0)

$$I_2 = I_{D3} + I_{D4} = 0$$

since: $I_{D3}, I_{D4} \geq 0 \qquad I_{D3} = I_{D4} = 0$

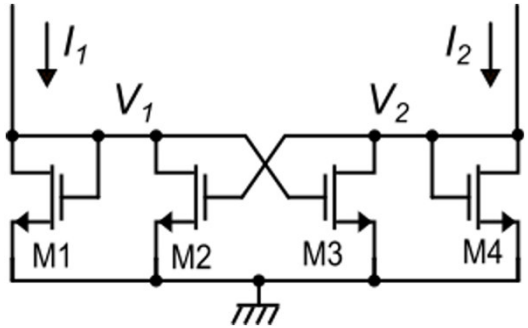
Considering M4: $V_{GS4} \leq V_t$

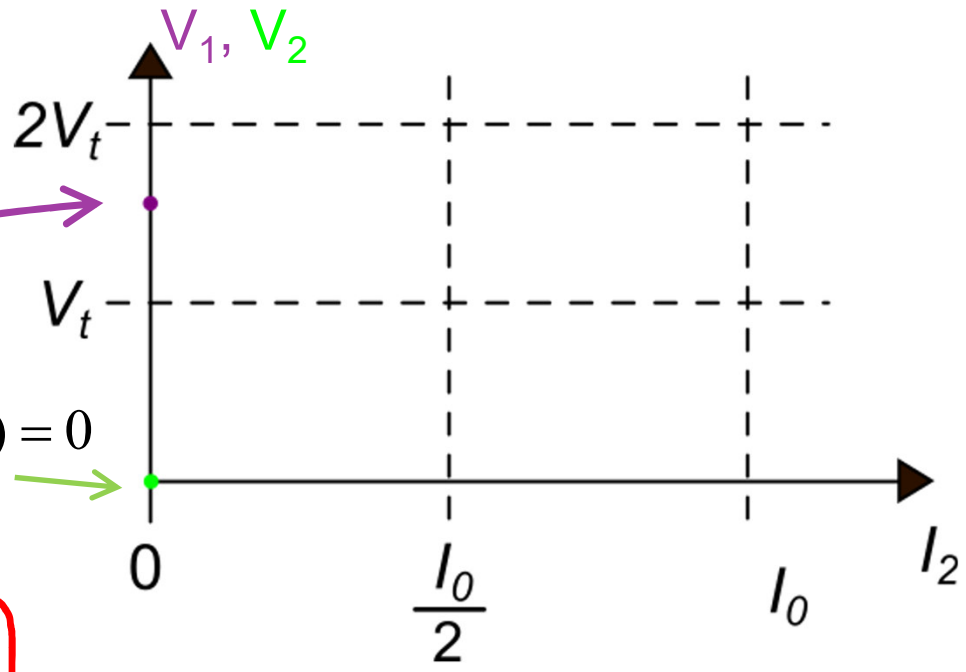
$$V_{GS2} = V_{GS4} \qquad I_{D2} = 0$$

Then it is M1 that carries all current I_1: $V_1 = V_{GS1} = V_t + \sqrt{\frac{2I_1}{\beta_L}} = V_t + \sqrt{\frac{2I_0}{\beta_L}}$

$$\left.\begin{array}{l} V_{GS3} = V_{GS1} \geq V_t \quad \text{(M3 is on)} \\ I_{D3} = 0 \end{array}\right\} \quad V_{DS3} = V_2 = 0$$

Analysis of the 4-transistor cell





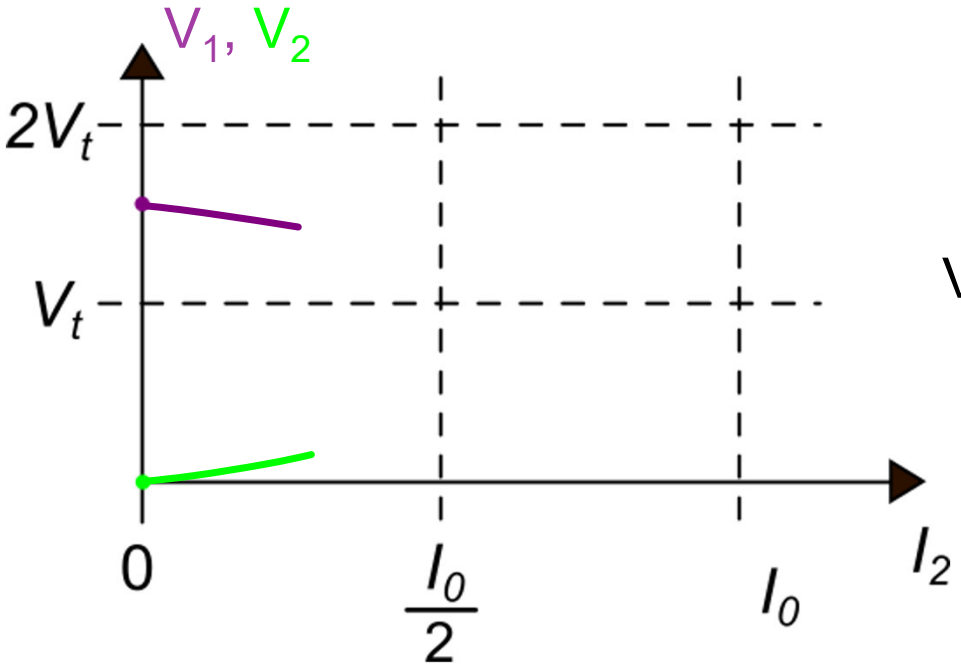
$$V_1(0) = V_t + \sqrt{\frac{2I_0}{\beta_L}} \qquad V_2(0) = 0$$

Design condition:
we size β_L in such a way that:

$$V_1(0) = V_{GS1}(0) < 2V_t \Rightarrow V_{GS1}(0) - V_t < V_t$$

The reason will be clear later

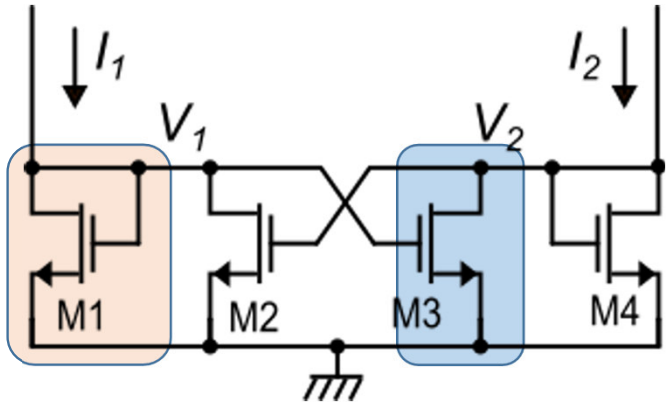
Increasing I_2

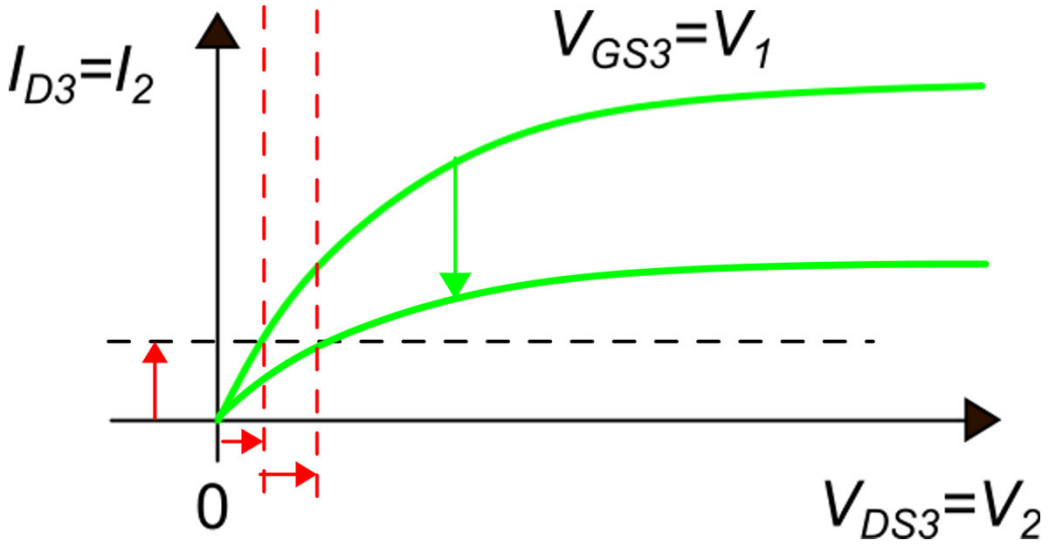


As I_2 increases, I_1 decreases of the same amount, then V_1 decreases:

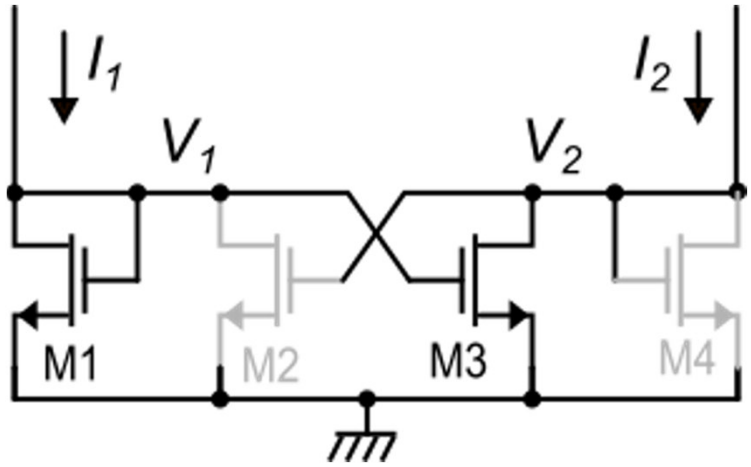
$$V_1 = V_{GS1} = V_t + \sqrt{\frac{2I_1}{\beta_L}}$$

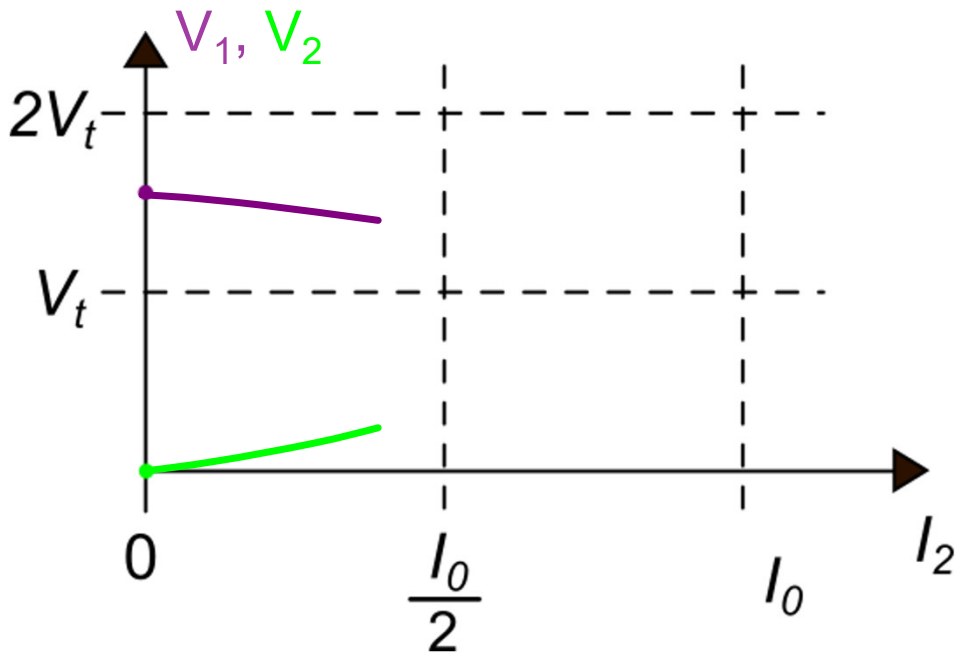
V_2 increases:





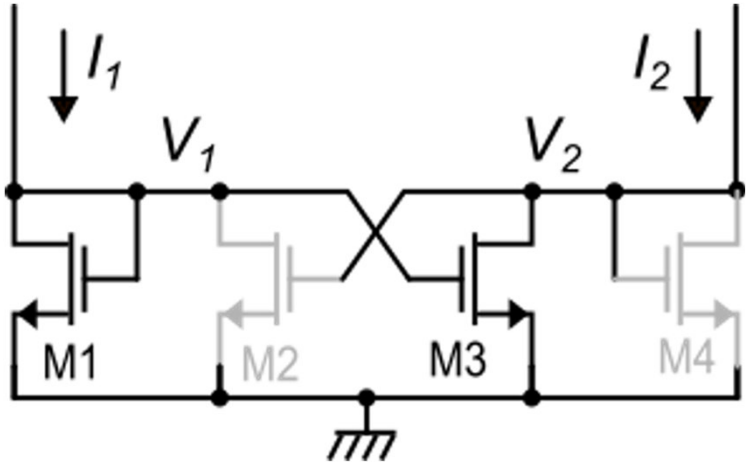
Increasing I_2





As I_2 progressively increases, V_2 increases. Until V_2 remains below the threshold voltage V_t, M2 and M4 are off

V_2 reaches the threshold



For $V_2=V_t$, M2 and M4 are still off. Then:

$$I_1 = I_{D1} \quad I_2 = I_{D3}$$

Since M3 is in saturation:

$$\frac{I_2}{I_1} = \frac{\beta_C}{\beta_L}$$

$$V_2 = V_t$$

Let us check whether M3 is now in saturation (was in triode region at the beginning)

$$V_{DS3} = V_2 = V_t$$

$$V_{GS3} = V_1 < V_1(0) < 2V_t$$

For the design condition mentioned earlier

$$V_{GS3} - V_t < V_t = V_{DS3}$$

$$V_{DS3} > V_{GS3} - V_t$$

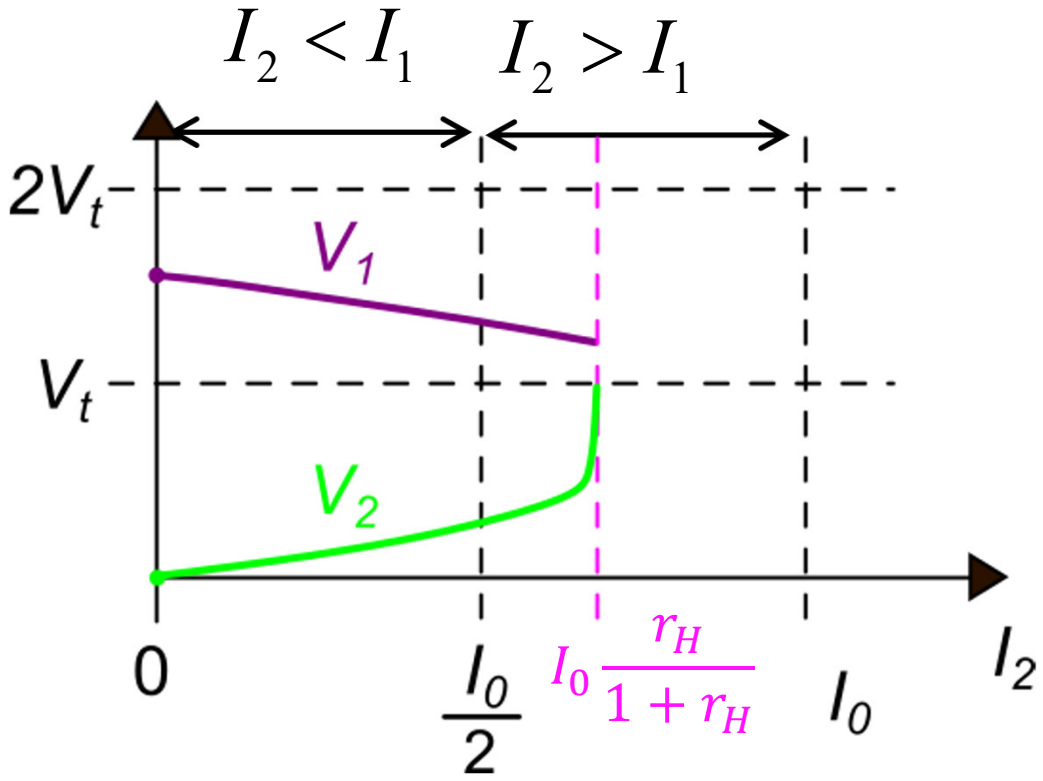
M3 is in saturation

V_2 reaches the threshold

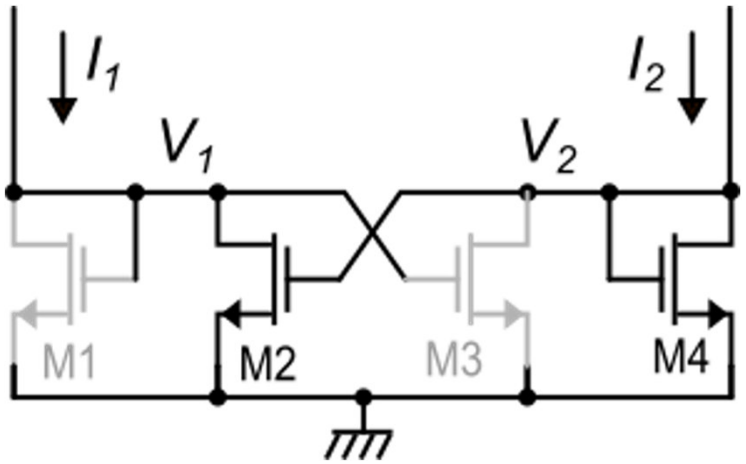
Case of interest: $\frac{\beta_C}{\beta_L} > 1$

$V_2 = V_t$ for $\frac{I_2}{I_1} = \frac{\beta_C}{\beta_L} \equiv r_H > 1$

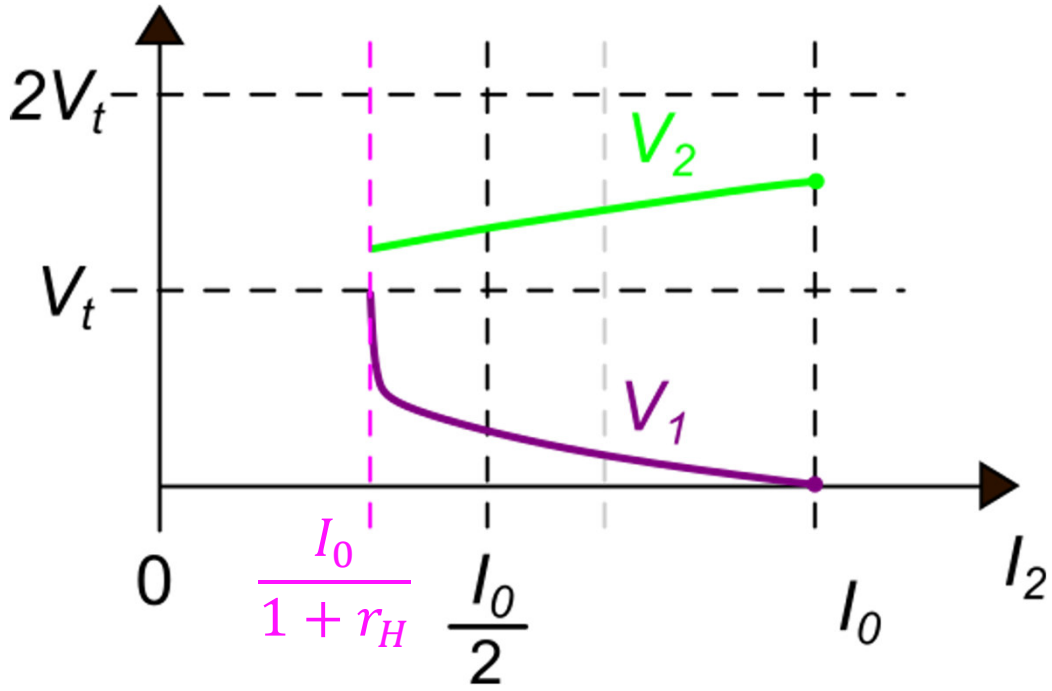
For $\beta_C > \beta_L$, V_2 reaches the threshold when I_2 has overcome the middle of the allowed range $[0, I_0]$



Starting from the other extreme



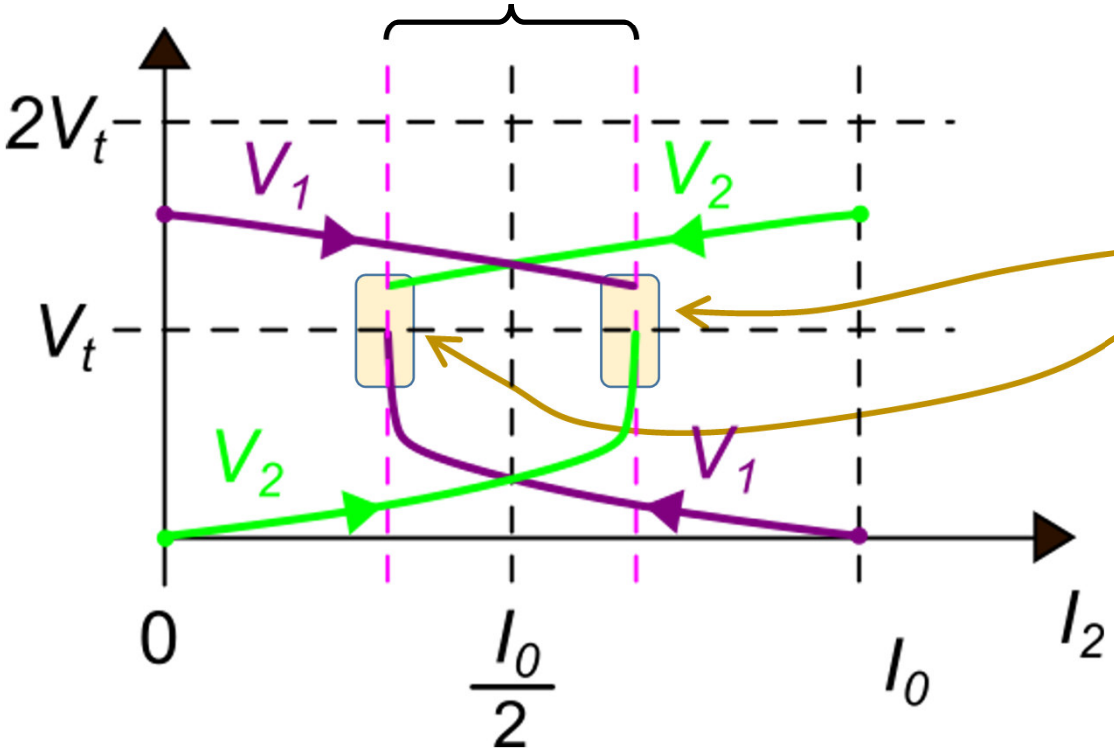
Repeating the same procedure but starting from the rightmost point (I_1=0, I_2=I_0) we obtain a symmetrical behavior with V_1 and V_2 swapped.



$$\frac{I_1}{I_2} = \frac{\beta_C}{\beta_L} = r_H > 1$$

Putting the two behaviors together:

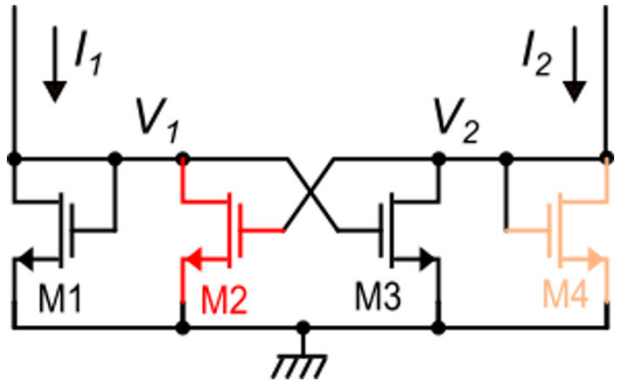
In this region, there are two possible states, depending on which extreme we started from

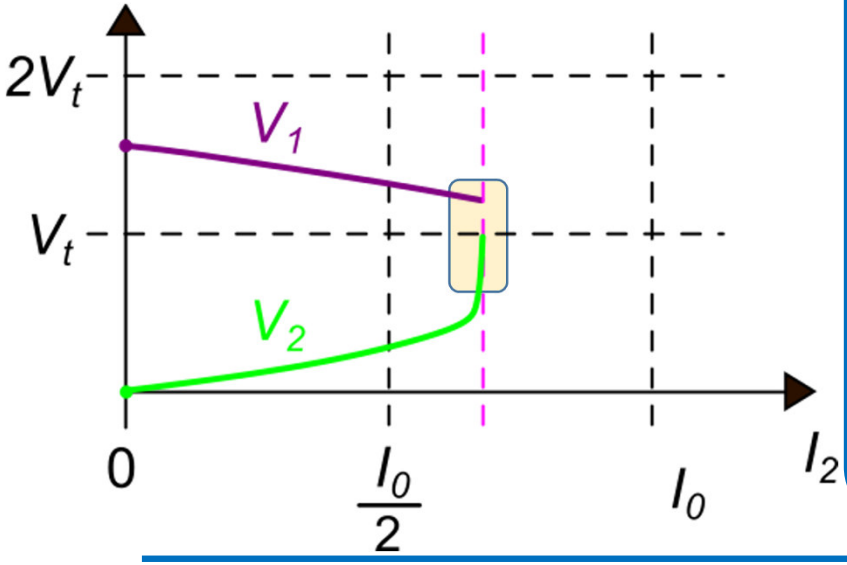


This means that there is hysteresis

Now we have to investigate what happens when the lower voltage hits the V_t line

Phenomena that happen when V_2 overcome V_t



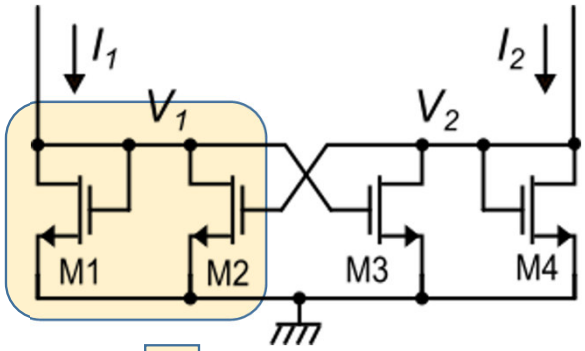


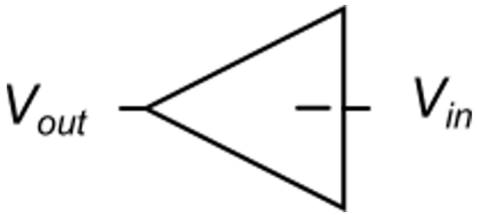
M2 and M4 turn on (while M1 and M3 are still on)

Let us focus on M2 — Positive feedback loop

1. As M2 turns on, it start stealing current from M1
2. V_1 decreases: $V_1 = V_{GS1} = V_t + \sqrt{\frac{2I_{D1}}{\beta_L}}$
3. $V_{GS3} = V_1$, then I_{D3} reduces, increasing the current that flows into M4
4. V_2 increases: $V_2 = V_{GS4} = V_t + \sqrt{\frac{2I_{D4}}{\beta_L}}$
5. $V_{GS2} = V_2$, then I_{D2} increases further

Positive feedback loop: small signal analysis

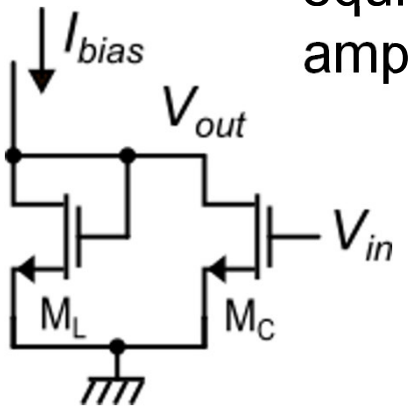


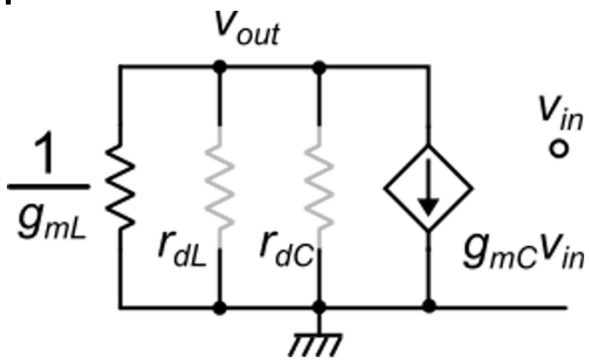


$$A = \frac{v_{out}}{v_{in}} = -g_{mC}\left(\frac{1}{g_{mL}} // r_{dL} // r_{dC}\right)$$

$$A \cong -\frac{g_{mC}}{g_{mL}}$$

Each half circuit is equivalent to an amplifier





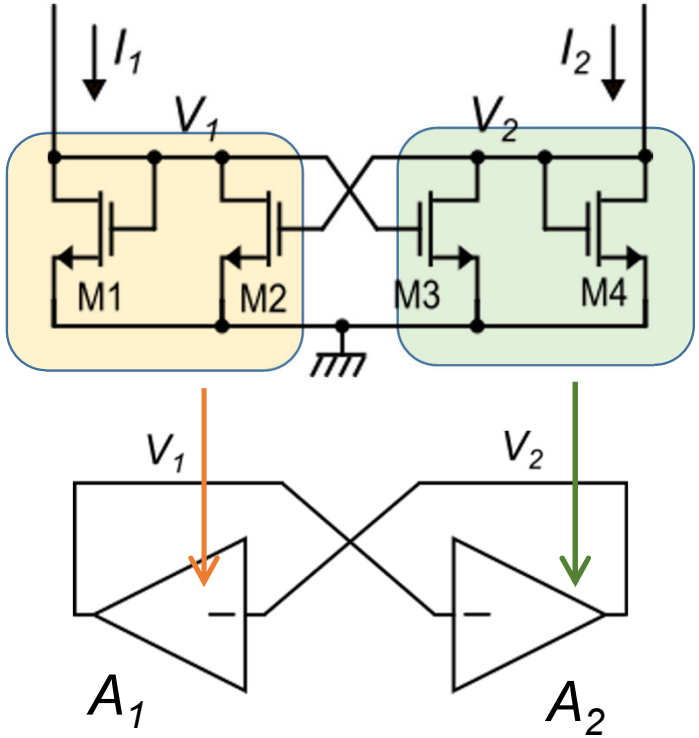
Small signal equivalent circuit

Due to the presence of the r_d's, the magnitude of A is slightly less than

$$\frac{g_{mC}}{g_{mL}}$$

Positive feedback loop: dc instability

When V_2 overcomes V_t, all MOSFETs are on:



$$A_1 = -\frac{g_{m2}}{g_{m1}}; \quad A_2 = -\frac{g_{m3}}{g_{m4}}$$

$$\beta A = A_1 A_2 > 0 \quad \text{Positive feedback}$$

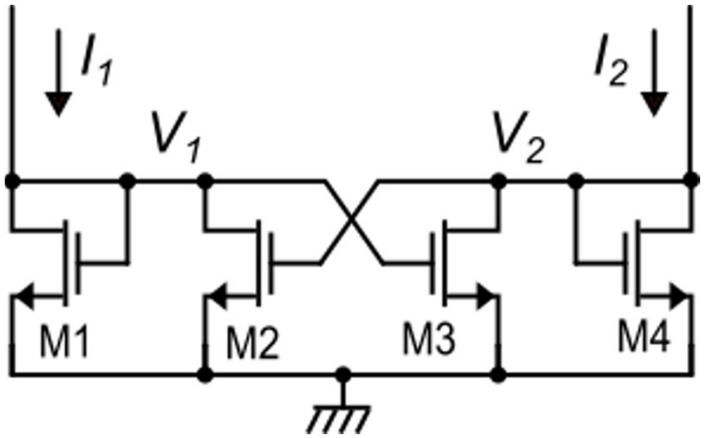
$$g_{m1} = \beta_L \left(V_{GS1} - V_t\right), \; g_{m2} = \beta_C \left(V_{GS2} - V_t\right)$$

$$g_{m3} = \beta_C \left(V_{GS3} - V_t\right), \; g_{m4} = \beta_L \left(V_{GS4} - V_t\right)$$

$$V_{GS1} = V_{GS3} = V_1, \; V_{GS2} = V_{GS4} = V_2$$

$$\beta A = \frac{\beta_C \left(V_2 - V_t\right)}{\beta_L \left(V_1 - V_t\right)} \cdot \frac{\beta_C \left(V_1 - V_t\right)}{\beta_L \left(V_2 - V_t\right)} = \left(\frac{\beta_C}{\beta_L}\right)^2$$

The effect of positive feedback



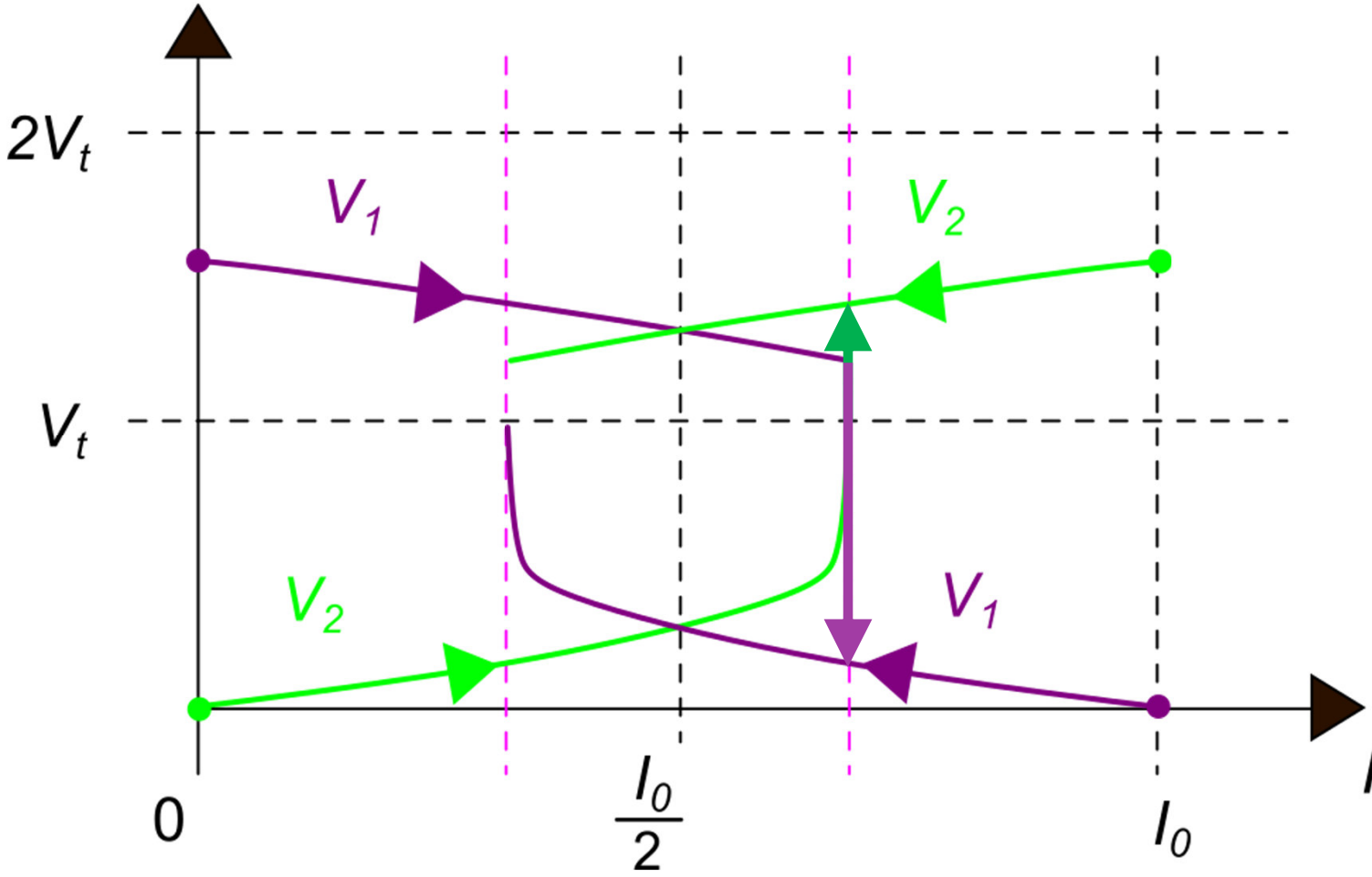
$$\frac{\beta_C}{\beta_L} = r_H > 1 \Rightarrow |\beta A| > 1 \quad \text{(dc instability)}$$

Therefore, a stable condition cannot exist if all MOSFETs are on.

Important condition

V_1 and V_2 cannot be greater than V_t at same time in a stable condition
Then, when M1 is on, M4 is off and vice versa

The "click"

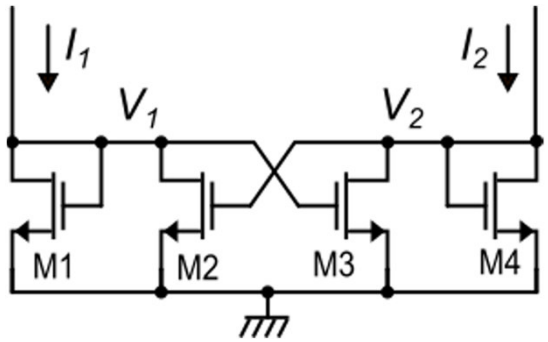


Proceeding from the left, when V_2 overcomes the V_t line, the positive feedback makes the voltage evolve autonomously.
The new stable solution is the one we already found proceeding back from the right

M1,M3: on M2,M4 off

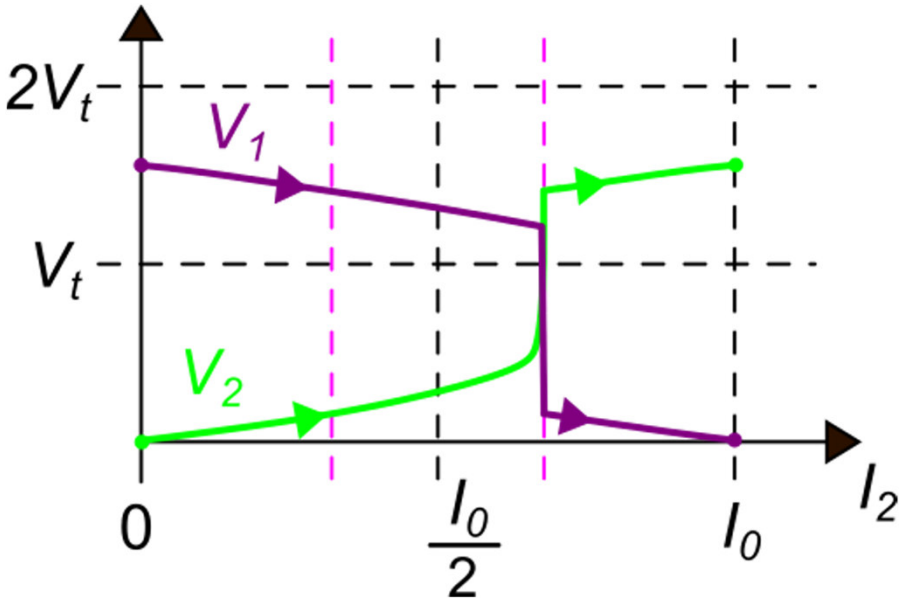
M2,M4: on M1,M3 off

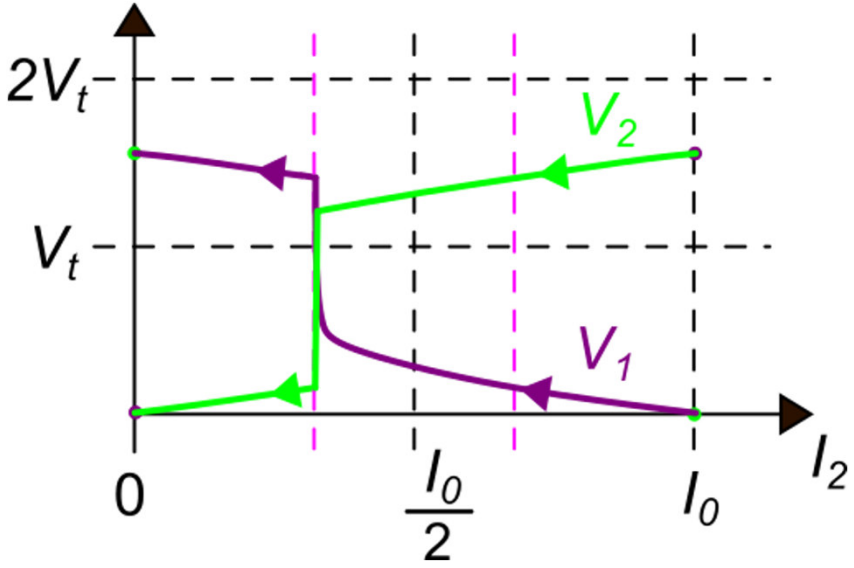
The two stable characteristics



Only one solution exists (stable)

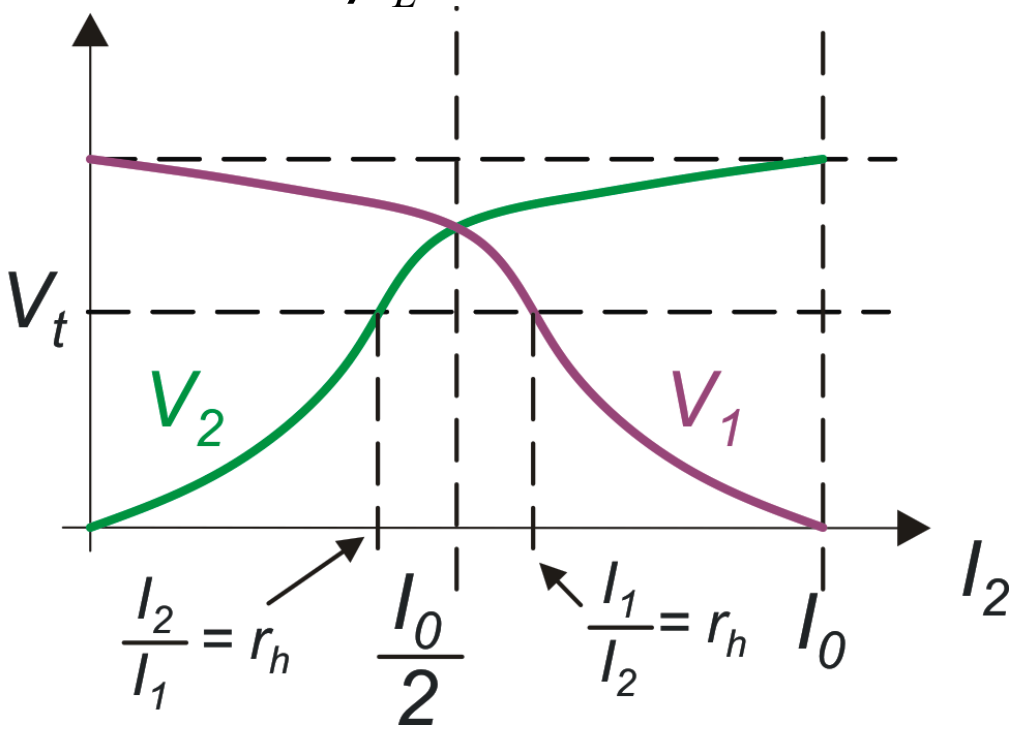
Three solutions exist:
2 stable
1 unstable (all devices are on)





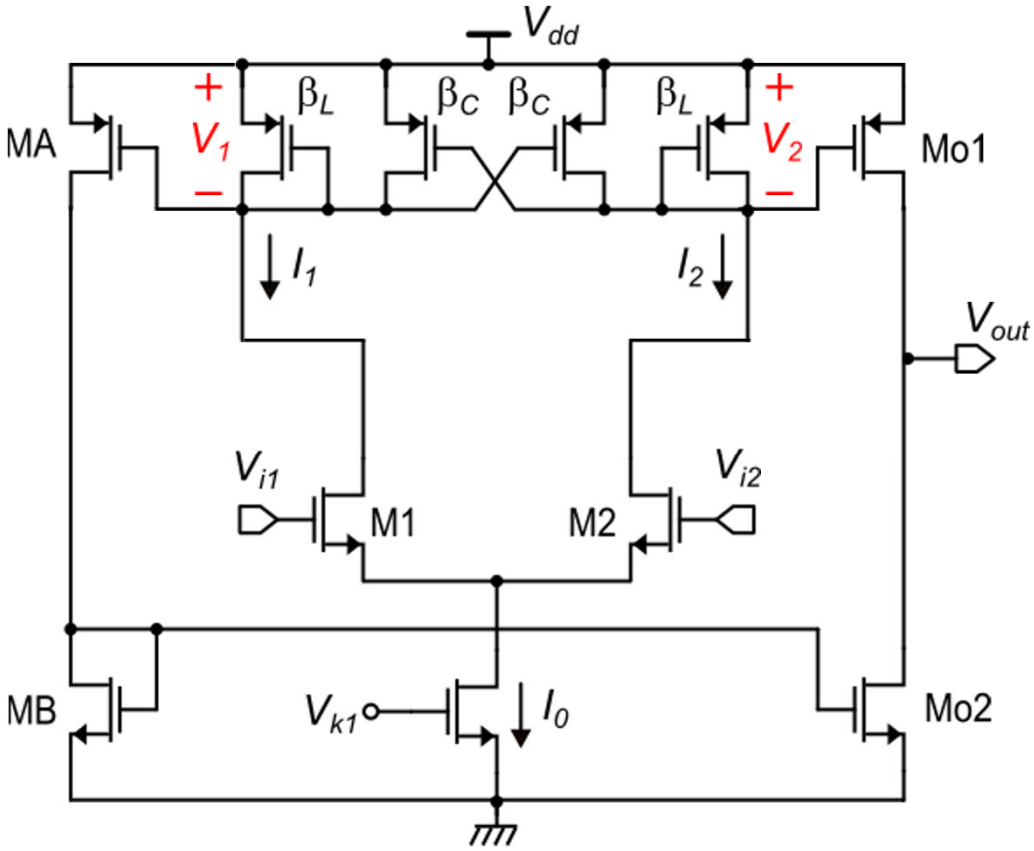
Non regenerative case (no hysteresis)

$$\frac{\beta_C}{\beta_L} = r_H < 1 \quad \Rightarrow \quad |\beta A| = \left(\frac{\beta_C}{\beta_L}\right)^2 < 1$$



In this case, the positive feedback is unable to cause a real abrupt transition
A hysteresis is not present

A simple comparator based on the 4-transistor hysteresis cell



$$V_{id} \equiv V_{i2} - V_{i1}$$

We start with a p-version of the hysteresis cell

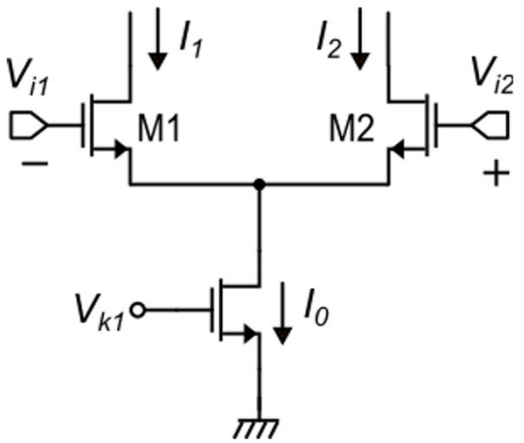
Currents I_1 and I_2 are derived from the input voltage $v_{id}=v_{i2}-v_{i1}$ by means of a differential pair

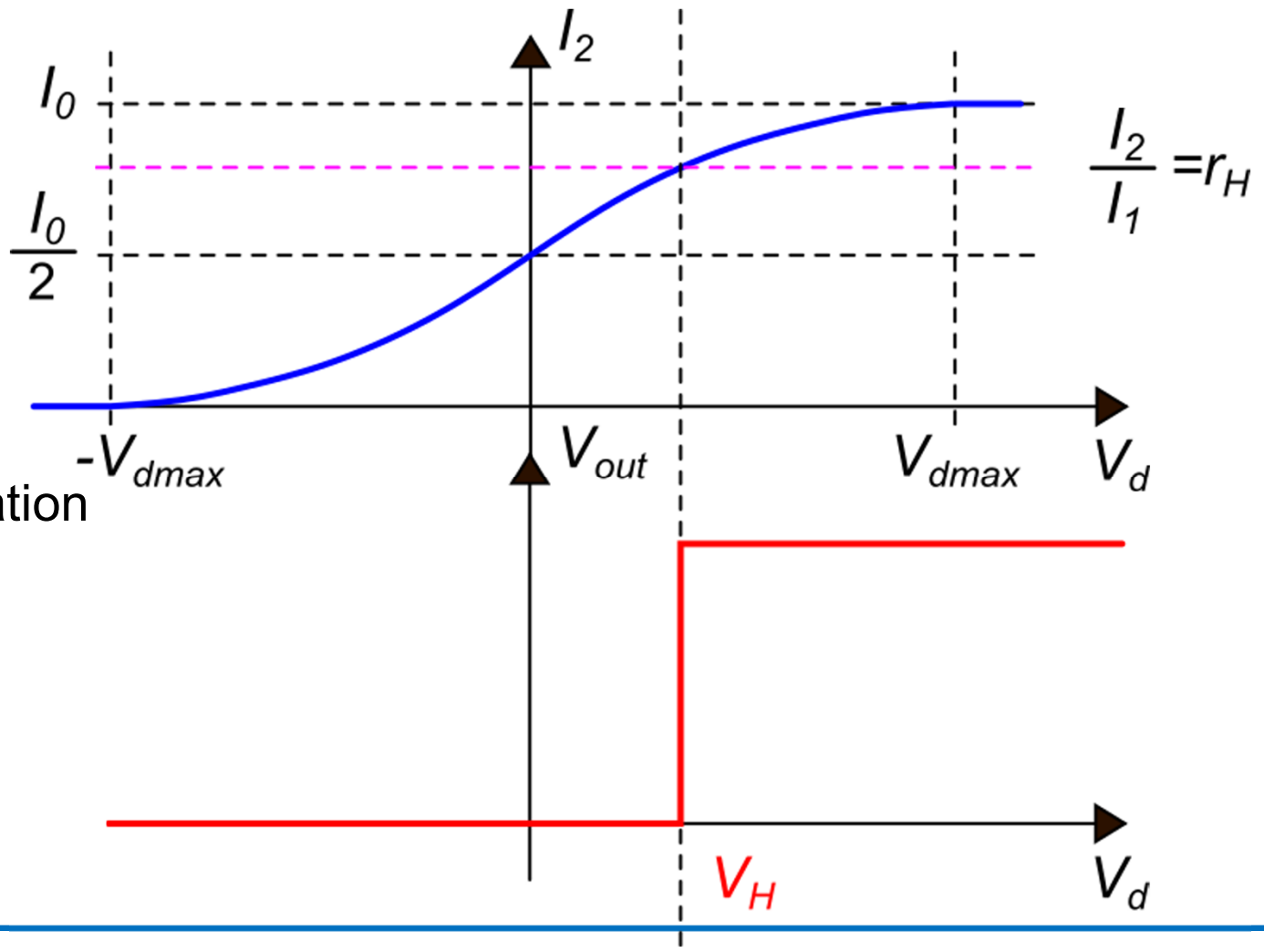
Only one at a time between V_1 and V_2 is greater than the p-mos threshold voltage.

If $V_1 > |V_{tp}|$, $V_2 < |V_{tp}|$ MA, MB and Mo2 are on, while Mo1 is off: $V_{out} = 0$

If $V_2 > |V_{tp}|$, $V_1 < |V_{tp}|$, only Mo1 is on: $V_{out} = V_{dd}$

Calculation of the comparator upper thresholds





Using a linear approximation of the differential pair:

$$\begin{cases} I_2 - I_1 = g_{m1} V_{id} \\ I_2 + I_1 = I_0 \end{cases}$$

Calculation of the comparator upper thresholds

$$\begin{cases} I_2 - I_1 = g_{m1} V_H \\ I_2 + I_1 = I_0 \\ \dfrac{I_2}{I_1} = r_H \end{cases}$$

$$I_2 - I_1 = I_1 (r_H - 1) = g_{m1} V_H$$

$$I_2 + I_1 = I_1 (r_H + 1) = I_0$$

$$\frac{r_H - 1}{r_H + 1} = \frac{g_{m1}}{I_0} V_H$$

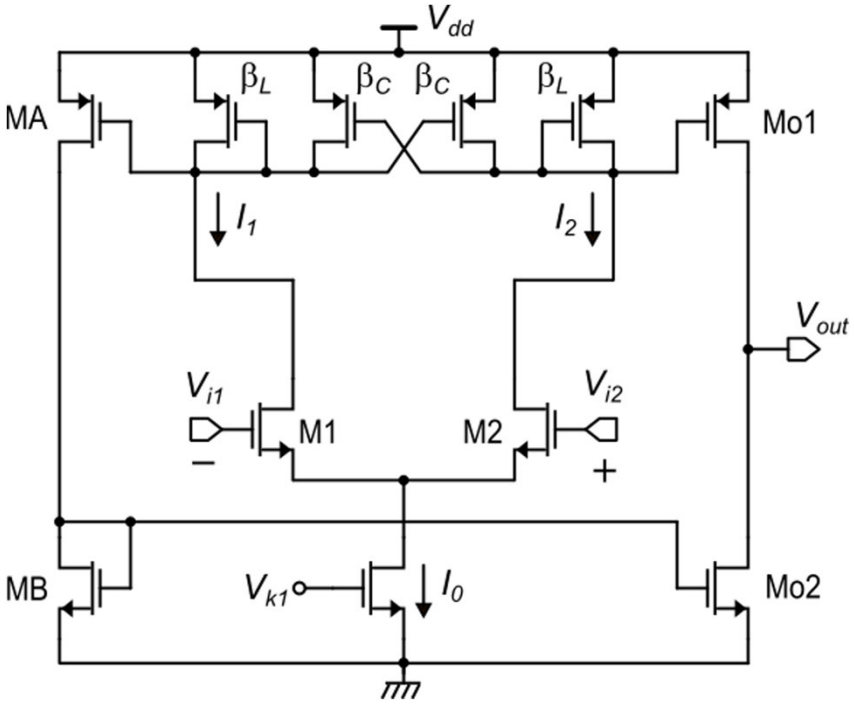
Dividing the upper equation by the lower one

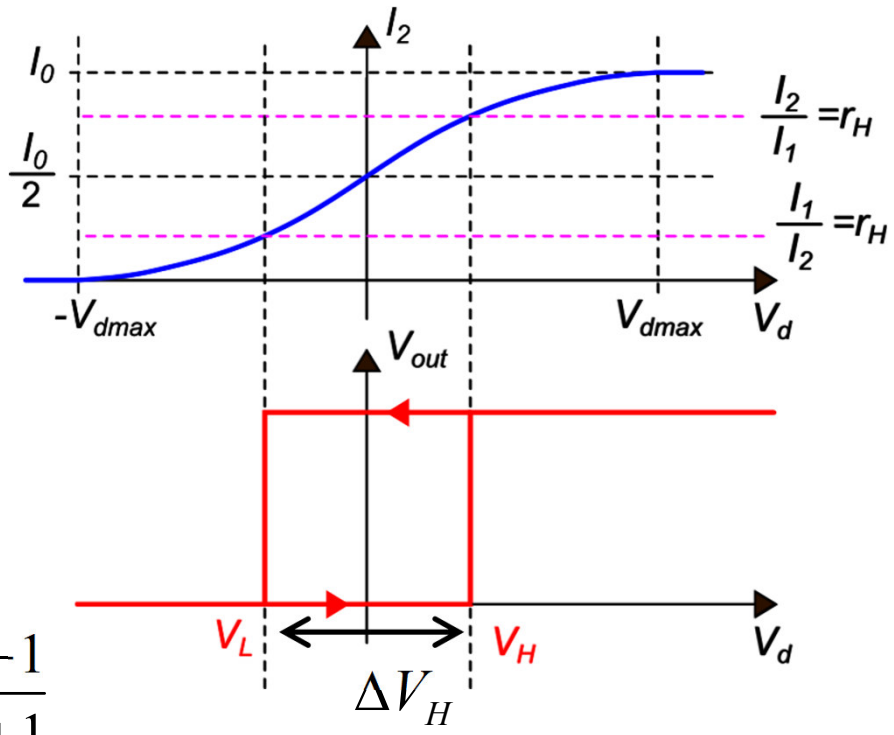
In quiescent conditions: $I_0 = 2 I_{D1-Q} = 2 V_{TE1} g_{m1}$

$$\frac{r_H - 1}{r_H + 1} = \frac{1}{2 V_{TE1}} V_H$$

$$V_H = 2 V_{TE1} \frac{r_H - 1}{r_H + 1}$$

Complete characteristics of the comparator





$$V_L = -V_H$$

$$V_H = 2V_{TE}\frac{r_H - 1}{r_H + 1}$$

$$\Delta V_H = V_H - V_L = 4V_{TE}\frac{r_H - 1}{r_H + 1}$$

In strong inversion: $\Delta V_H = 2\left(V_{GS} - V_t\right)_1 \frac{r_H - 1}{r_H + 1}$

Minimum achievable hysteresis

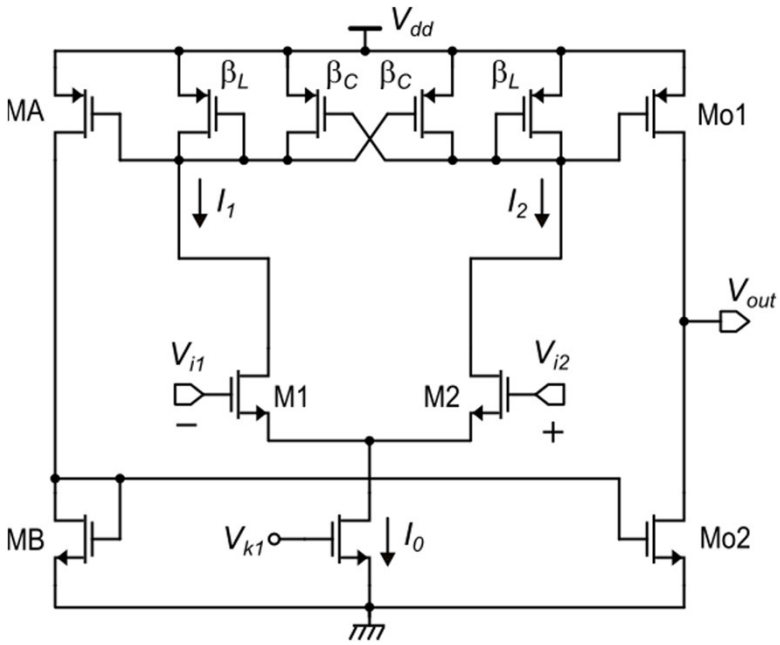
$$\Delta V_H = V_H - V_L = 4V_{TE}\frac{r_H - 1}{r_H + 1}$$

To obtain a small hysteresis

- Make V_{TE1} as small as possible
- Make r_H just slightly larger than 1

However, other requirements impose to make r_H significantly larger than 1, because:

1) The calculated $|\beta A|=(r_H)^2$ is overestimated, since we have neglected the r_d's
2) Process error can make r_H <1 if the margin to 1 is too small
3) The transition is faster with larger $|\beta A|$



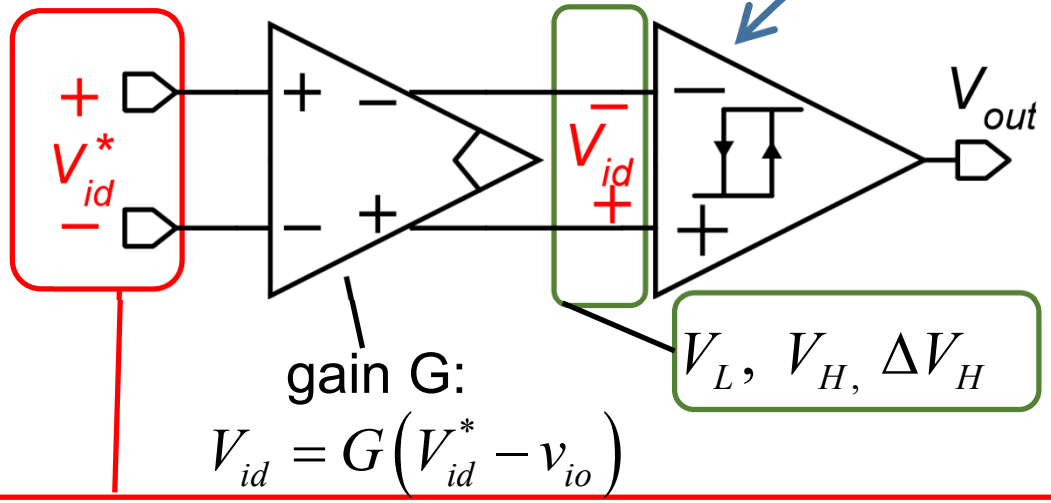
A typical robust choice:

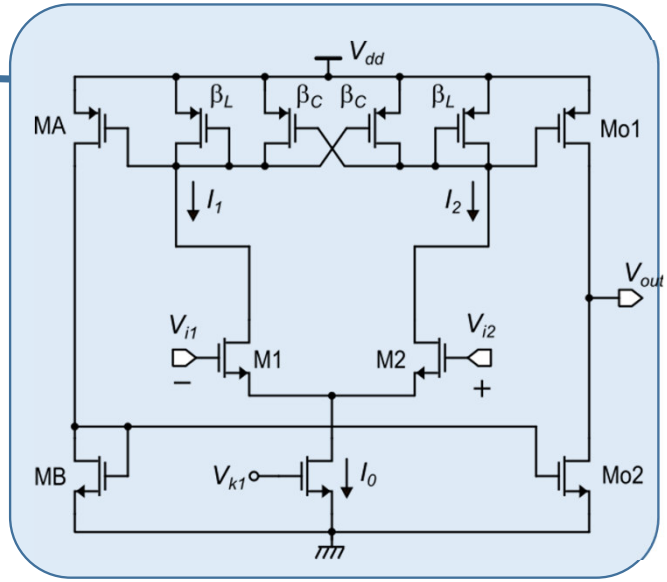
$$r_H = 2 \Rightarrow \Delta V_H = \frac{4}{3}V_{TE}$$

ΔV_H as small as **50 mV**

How to obtain a comparator with very low hysteresis

The simplest solution is using a pre-amplifier:





gain G:

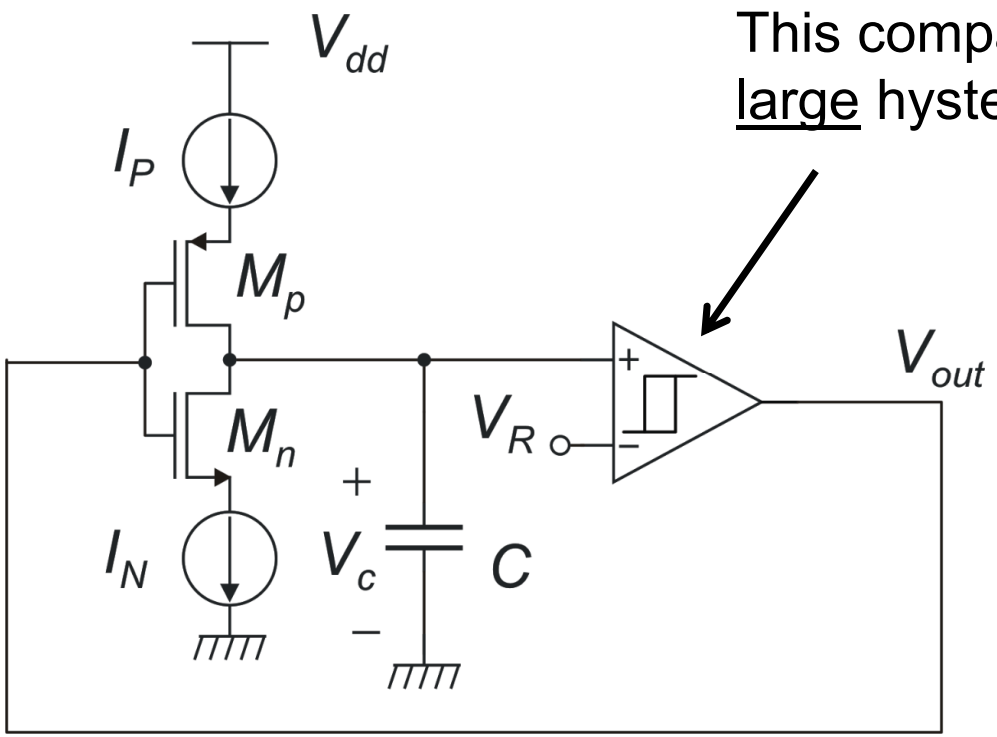
$$V_{id} = G\left(V^*_{id} - v_{io}\right)$$

$$V^*_{id} = \frac{V_{id}}{G} + v_{io} \quad V^*_H = \frac{V_H}{G} + v_{io}\ ,\ V^*_L = \frac{V_L}{G} + v_{io} \quad \Delta V^*_H = \frac{\Delta V_H}{G}$$

The hysteresis is divided by the preamplifier gain (G)

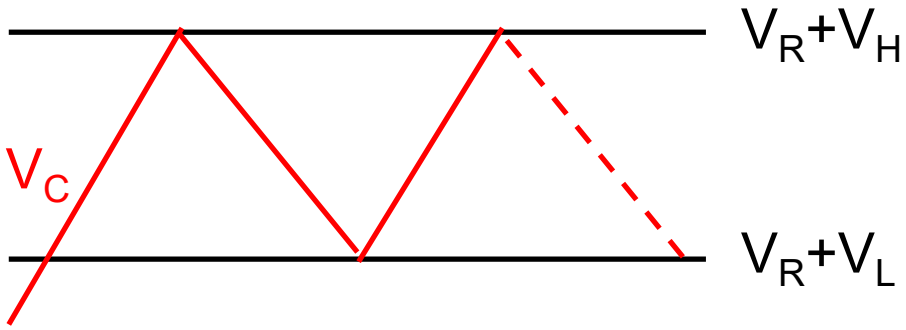
In discrete time systems the amplifier offset can be cancelled with CDS

A simple low-frequency VCO based on comparator hysteresis

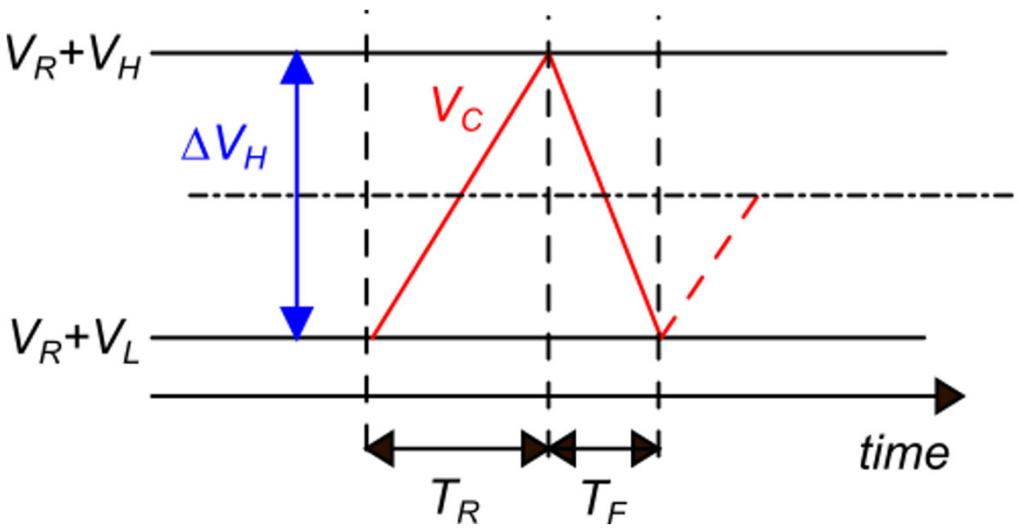


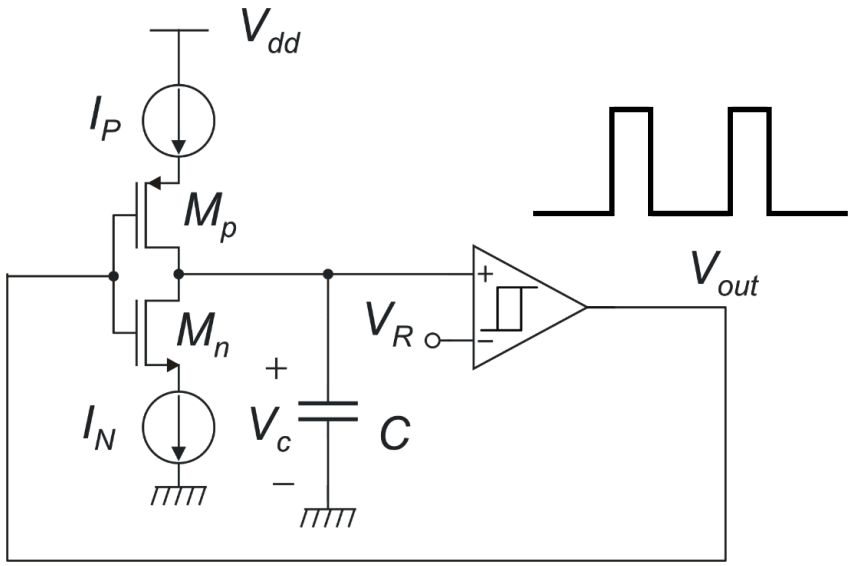
This comparator is designed to have a large hysteresis

- When V_{out}=0, the capacitor is charged by I_P
- When V_{out}=1, the capacitor is discharged by I_N



Calculation of the oscillator frequency



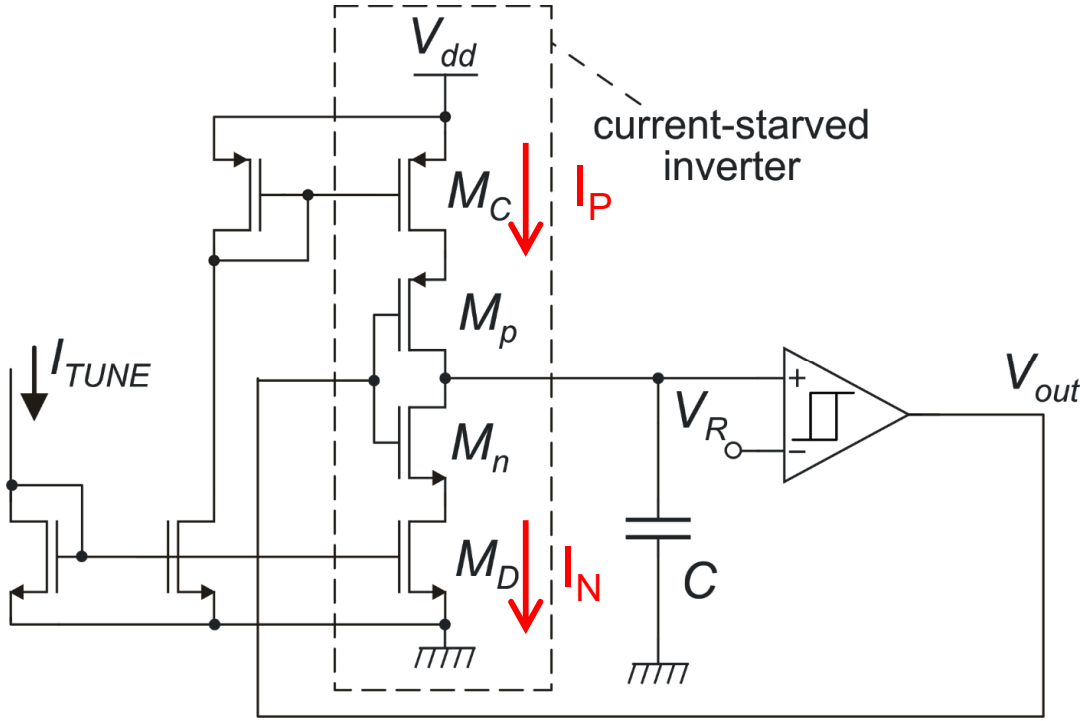


rise time = $T_R = \dfrac{\Delta V_H}{I_P / C} = C\dfrac{\Delta V_H}{I_P}$

fall time = $T_F = \dfrac{\Delta V_H}{I_N / C} = C\dfrac{\Delta V_H}{I_N}$

period = $T = T_R + T_F = C\Delta V_H\left(\dfrac{1}{I_p} + \dfrac{1}{I_N}\right)$

Implementation with "current starved" inverter



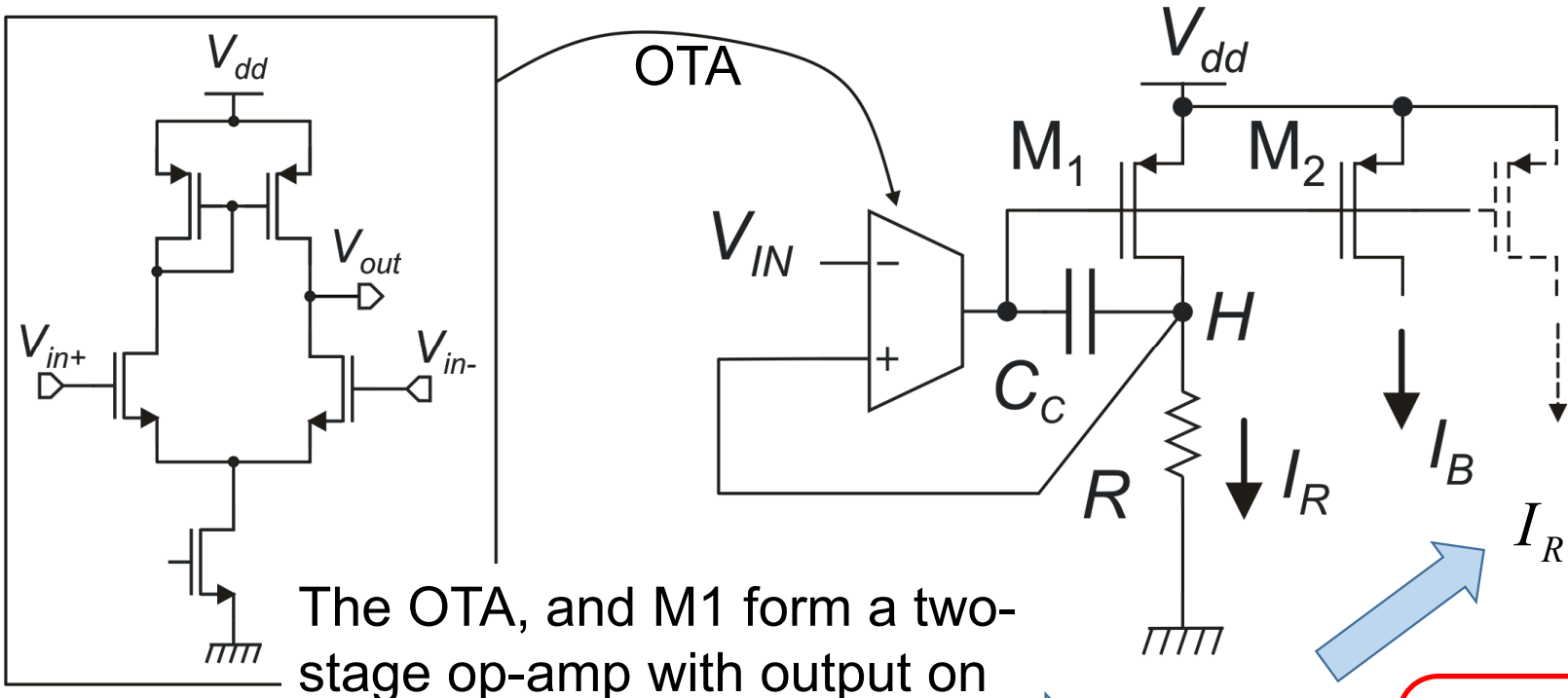
If $I_P = I_N = I_{tune}$:

$$T = 2\frac{C\Delta V_H}{I_{tune}} \qquad f = \frac{I_{tune}}{2C\Delta V_H}$$

The frequency is proportional to the tuning current (CCO)

Using a linear voltage to current converter it is possible to make I_{tune} to be proportional to a voltage, transforming the CCO into a VCO

A simple voltage-to-current converter



This circuit can be used also to produce constant currents from a single reference voltage

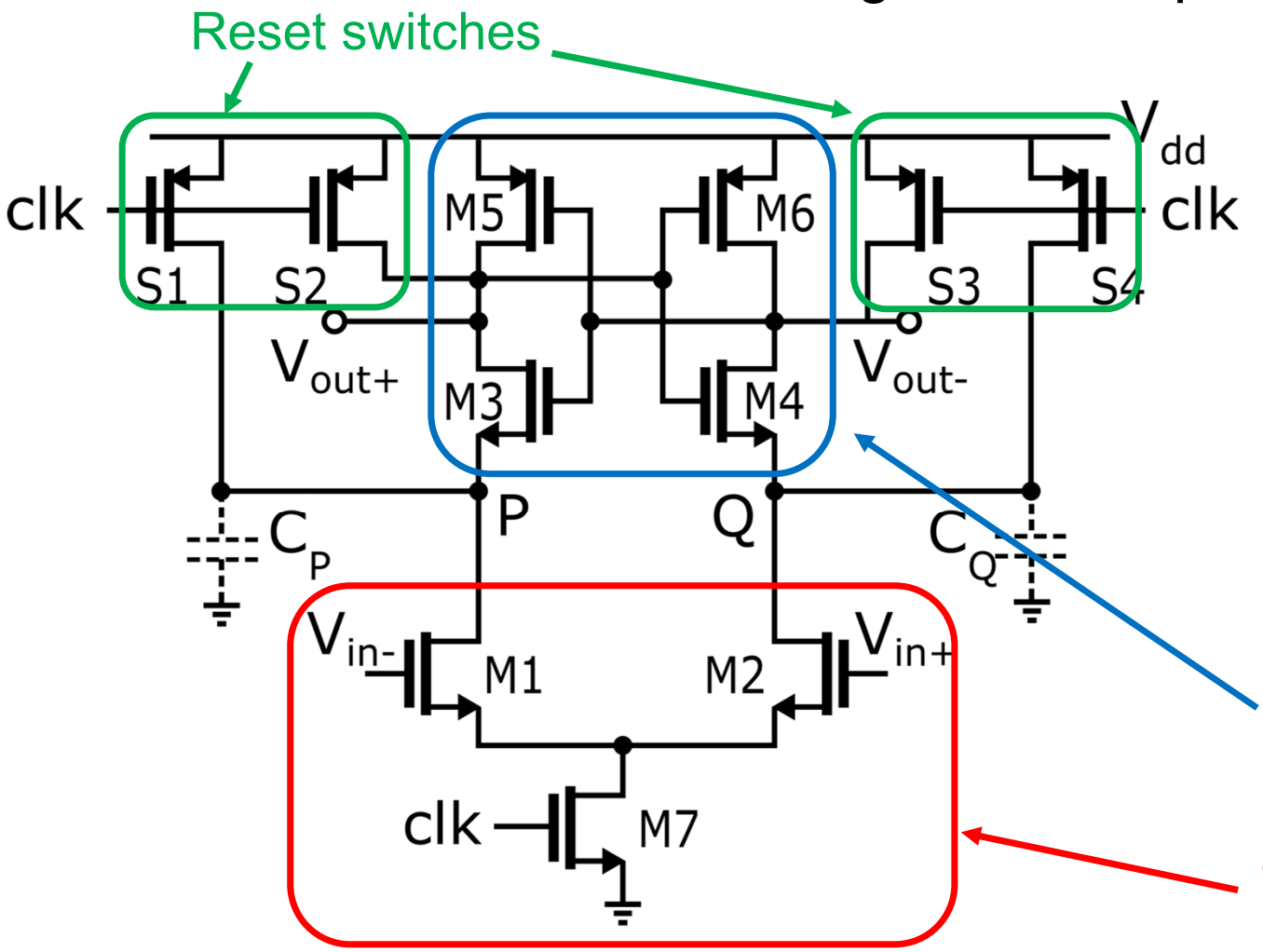
The OTA, and M1 form a two-stage op-amp with output on node H, stabilized by C_C (Miller compensation). The op-amp is closed as a buffer:

$$V_H = V_{IN}$$

$$I_R = I_{D1} = \frac{V_{in}}{R}$$

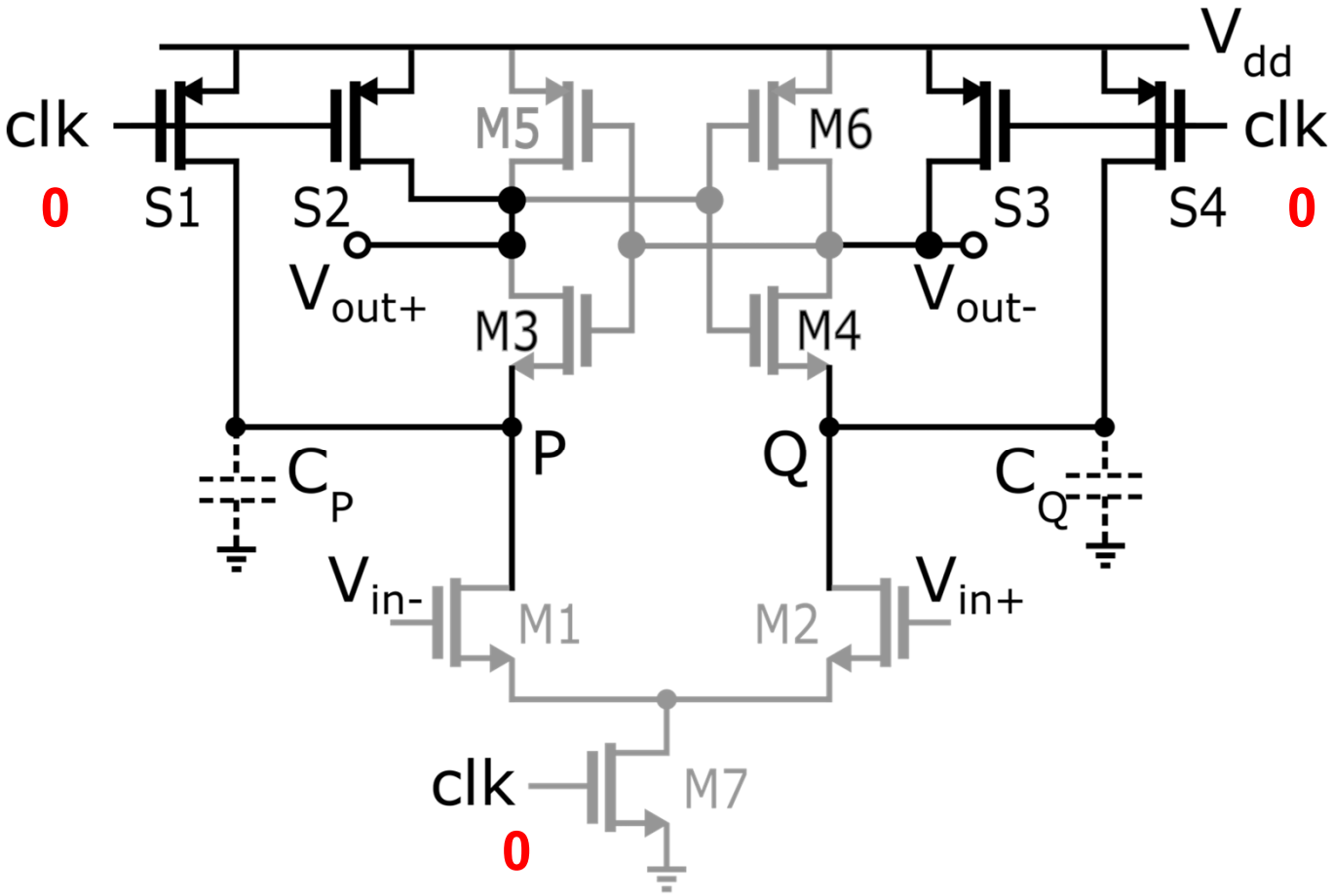
$$I_B = \frac{\beta_2}{\beta_1} I_{D1} = \frac{\beta_2}{\beta_1} \frac{V_{IN}}{R}$$

StrongARM Comparator



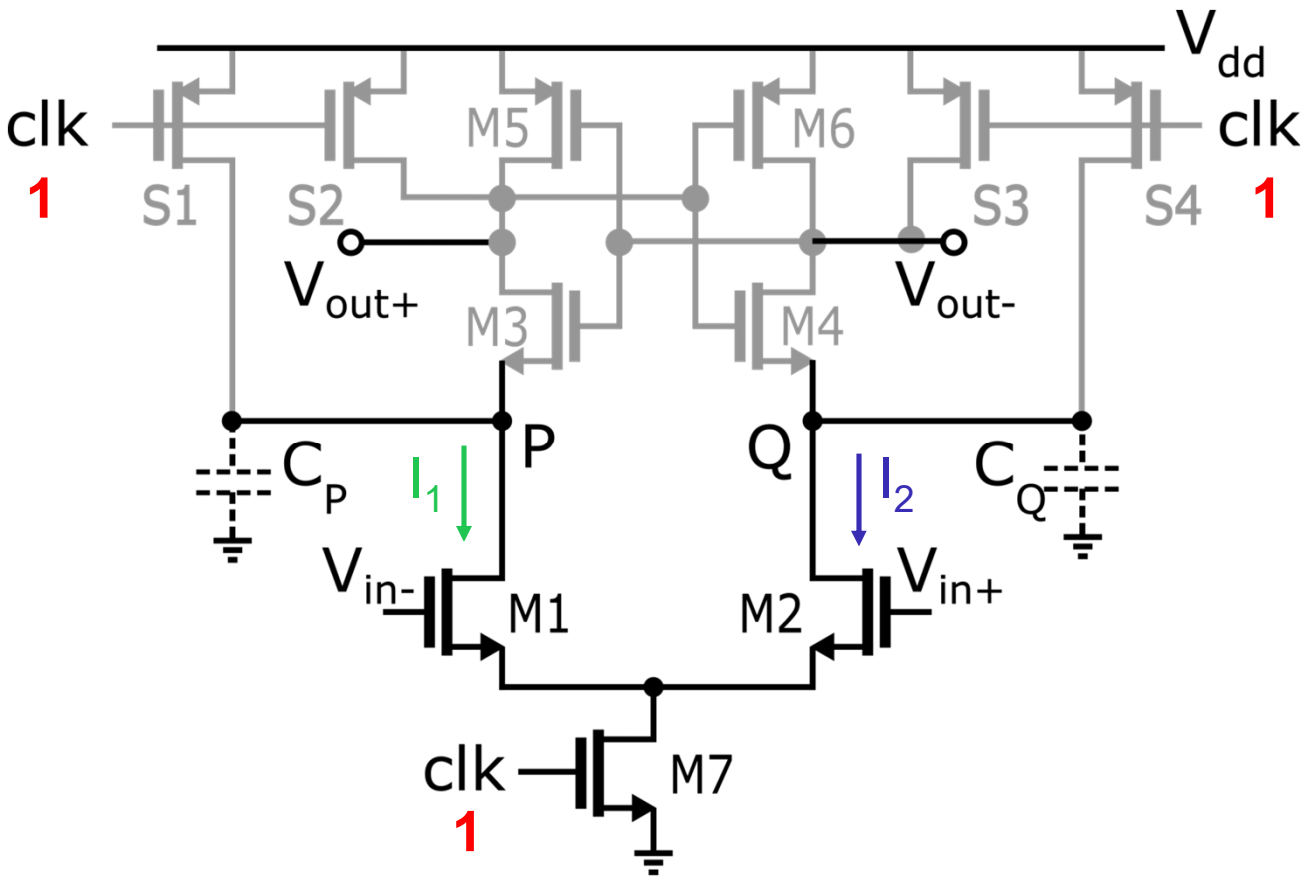
- First proposed as Sense Amplifier for SRAM (used in StrongARM microprocessor)
- No static power consumption
- Rail-to-rail outputs
- Compare $V_{id} = V_{in}^{+}-V_{in}^{-}$ on the rising edge of the clock signal

Reset Phase



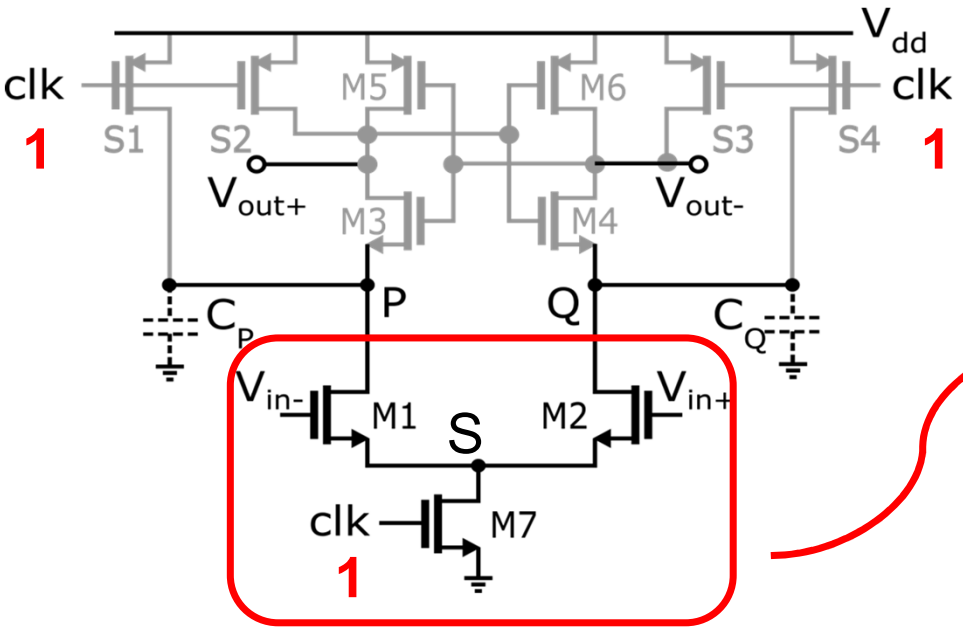
- Nodes P,Q, V_{out}^{+}, V_{out}^{-} are connected to V_{dd} through S1-S4
- The input pair is off
- Each reset phase, the comparator loses 'memory' of the previous cycle → No hystheresis

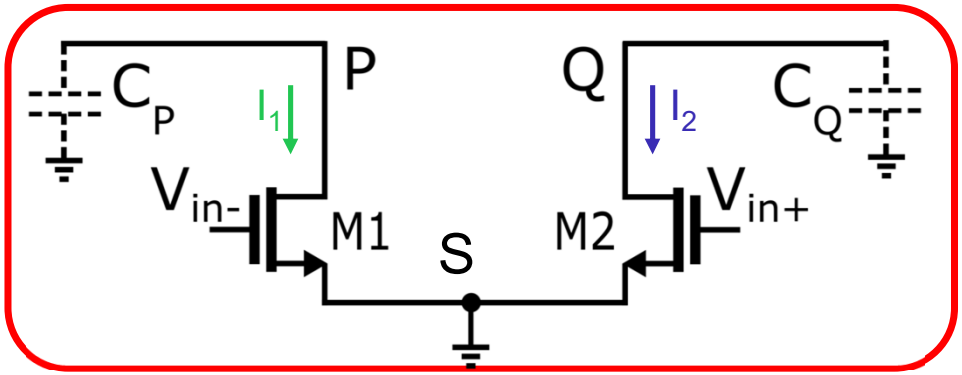
Amplification Phase



- S1-S4 go off, M7 goes on
- The input pair is on
- I_1, I_2 start discharging the parasitic capacitances C_P, C_Q at nodes P,Q
- Depending on $V_{id}=V_{in}^{+}-V_{in}^{-}$ node P is discharged faster/slower than node Q

Amplification Phase





Pseudo-differential pair (when clk=1, M7 connects node S to gnd)

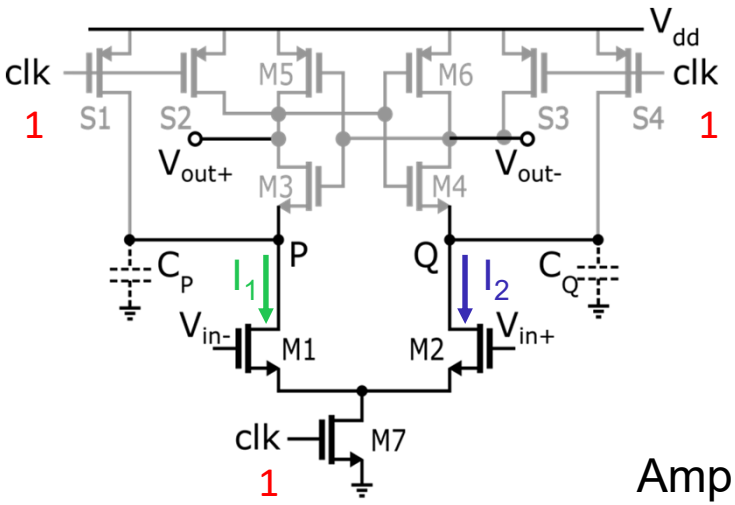
small V_{id}

I_{CM}

$\beta_{1,2}(V_{CMI} - V_{th})$

$$\begin{cases} I_1 = \frac{\beta_{1,2}}{2}(V_{in}^- - V_{thn})^2 \cong \frac{\beta_{1,2}}{2}(V_{CMI} - V_{thn})^2 - \frac{g_{m1}V_{id}}{2} \\ I_2 = \frac{\beta_{1,2}}{2}(V_{in}^+ - V_{thn})^2 \cong \frac{\beta_{1,2}}{2}(V_{CMI} - V_{thn})^2 + \frac{g_{m1}V_{id}}{2} \end{cases}$$

Amplification Phase



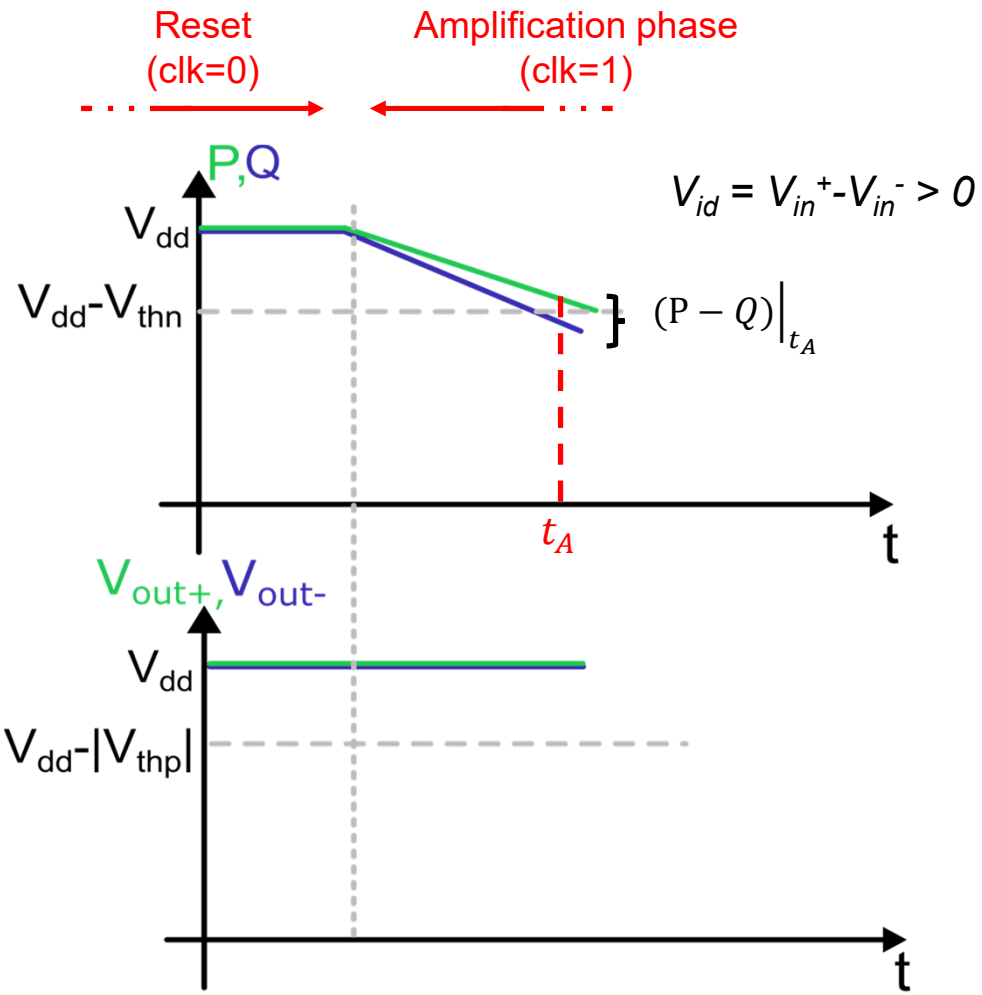
Amplification lasts until P,Q reaches V_{dd}-V_{thn}

$$\begin{cases} \dfrac{dP}{dt} = -\dfrac{I_1}{C_P} \\ \dfrac{dQ}{dt} = -\dfrac{I_2}{C_P} \end{cases}$$

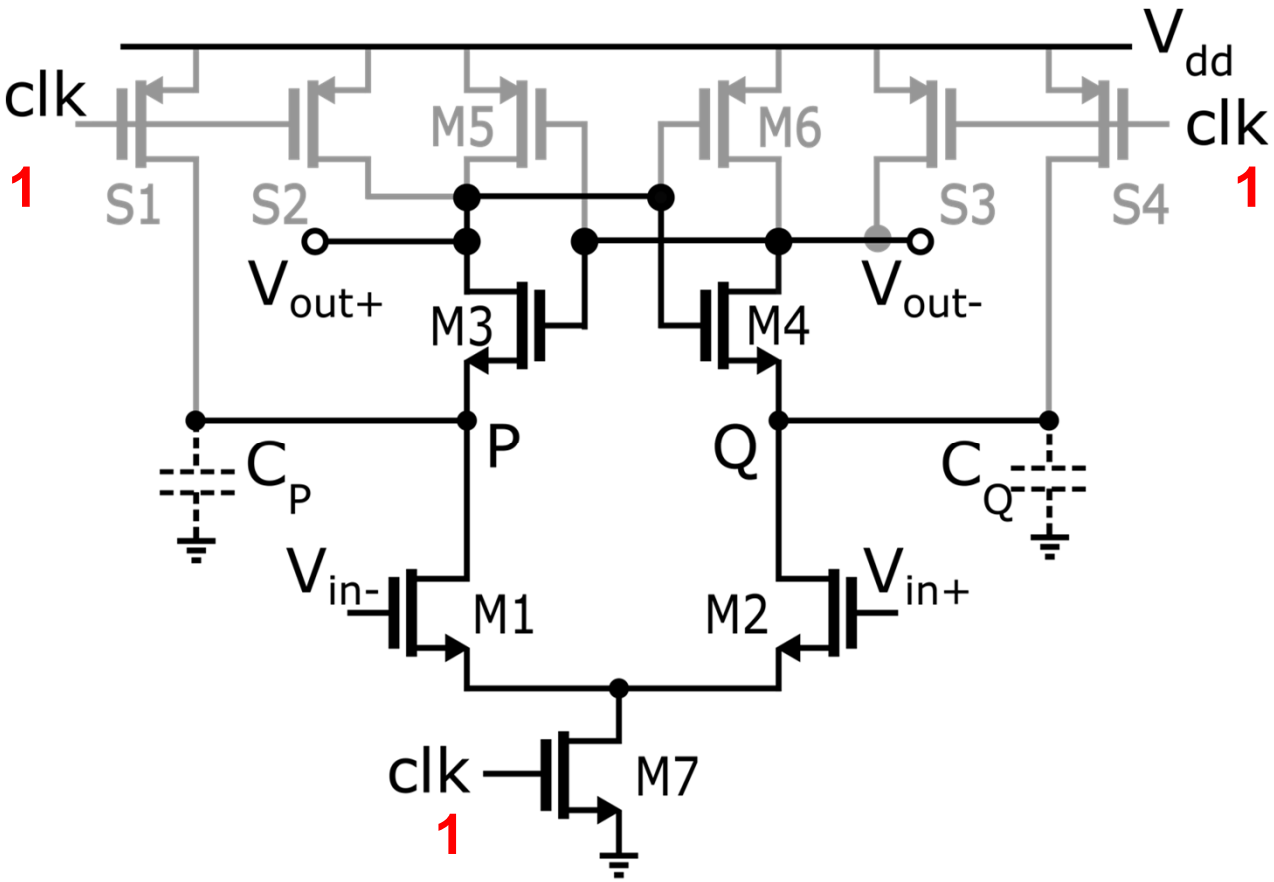
$$t_A \cong \frac{V_{thn}}{I_{CM}} C_{P,Q}$$

$$(\mathrm{P}-Q)\Big|_{t_A} \cong \frac{g_{m1}}{C_{P,Q}} t_A V_{id}$$

gain A

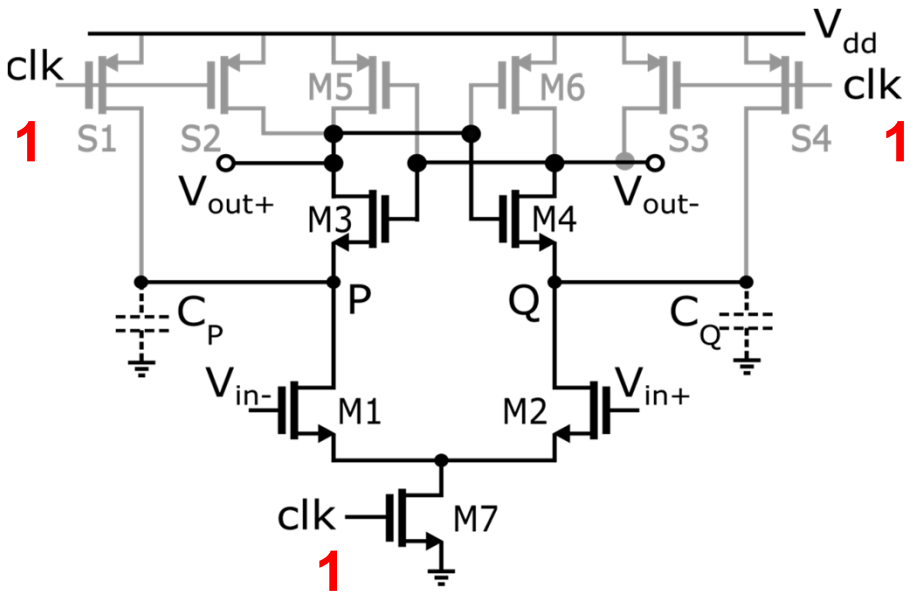


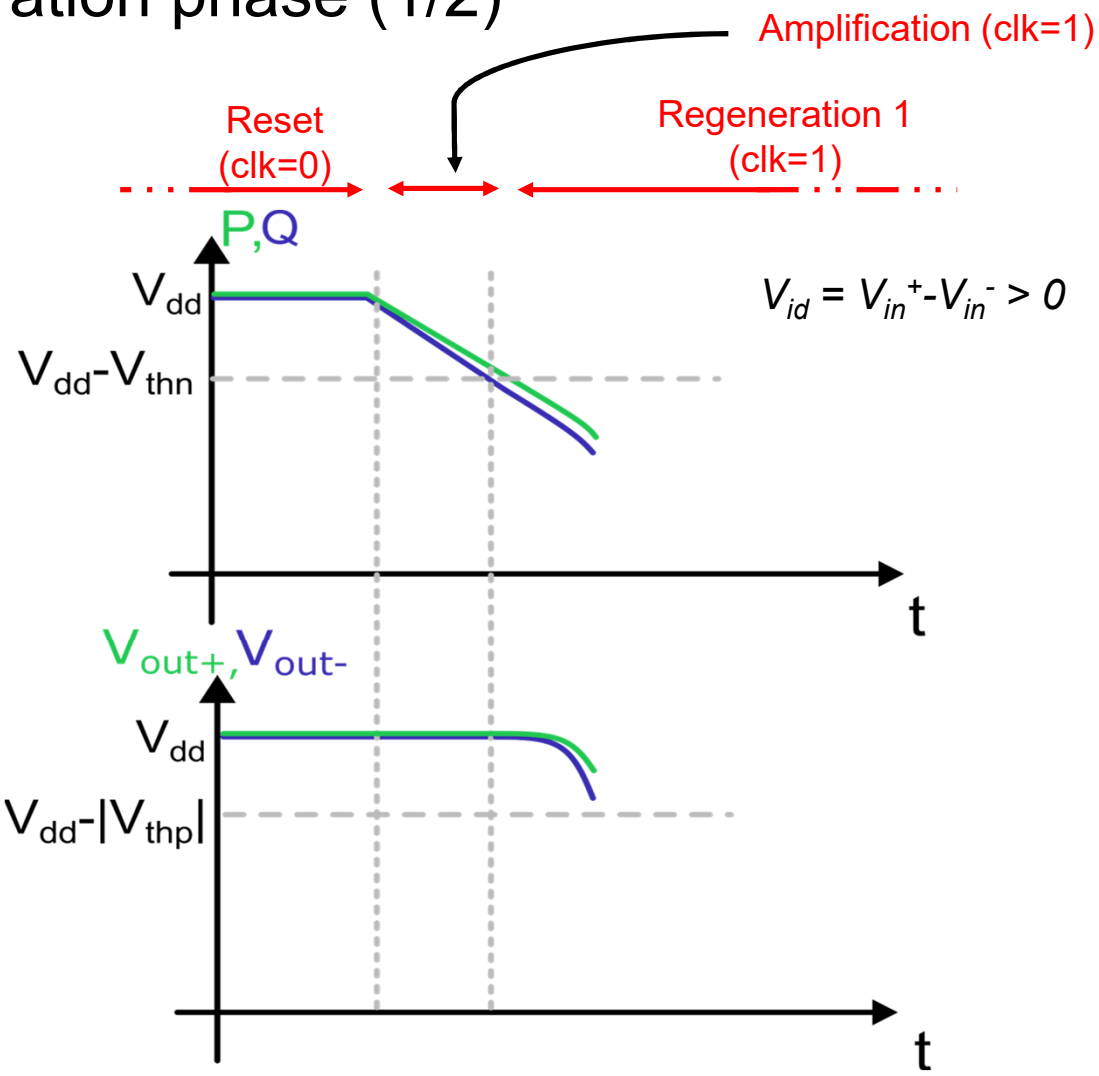
Regeneration phase (1/2)



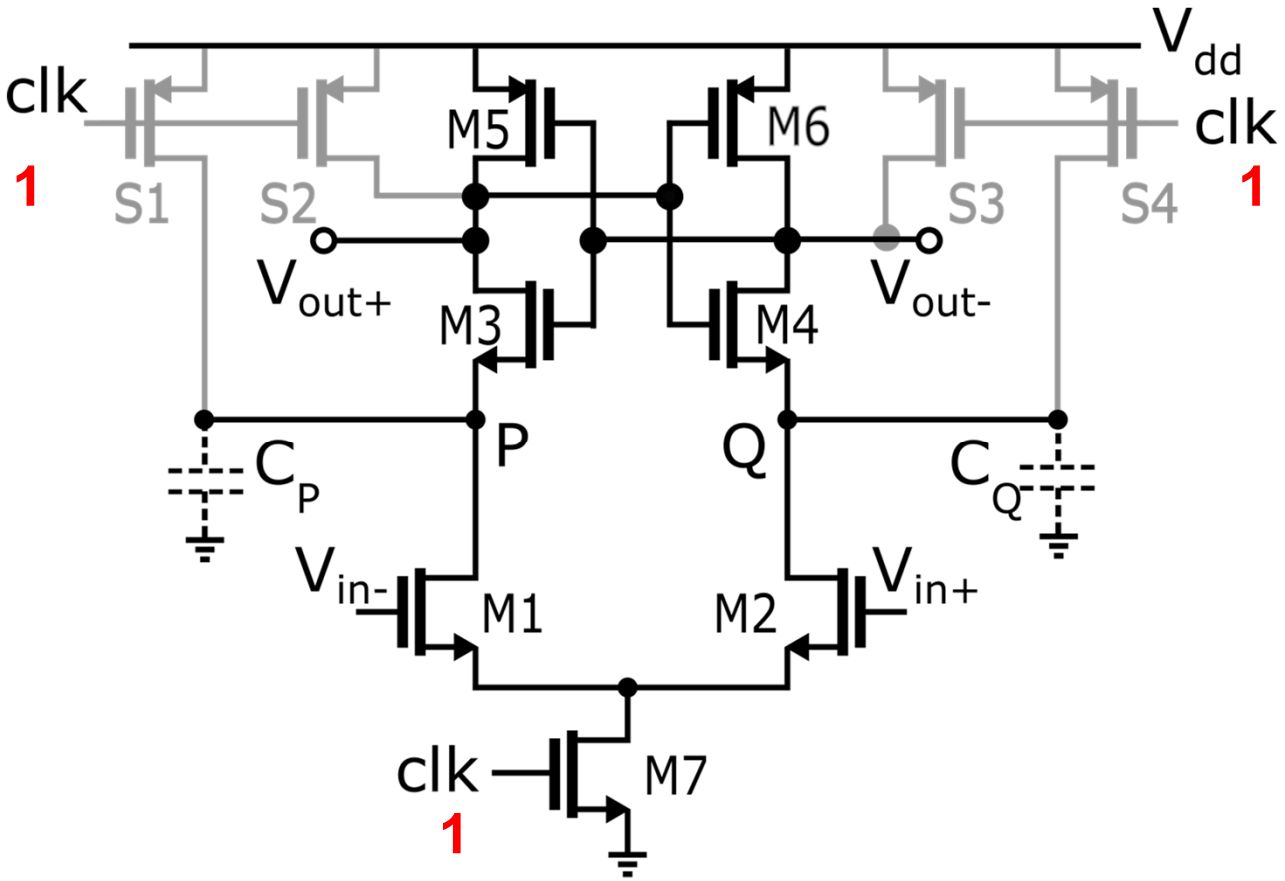
- When voltages at nodes P,Q go lower than V_{dd}-V_{thn}, M3-M4 turn on
- Cross-coupled pair M3-M4 introduces regeneration
- Nodes P,Q keep discharging and V_{out}^+, V_{out}^- start discharging differently according to the unbalance of P and Q

Regeneration phase (1/2)



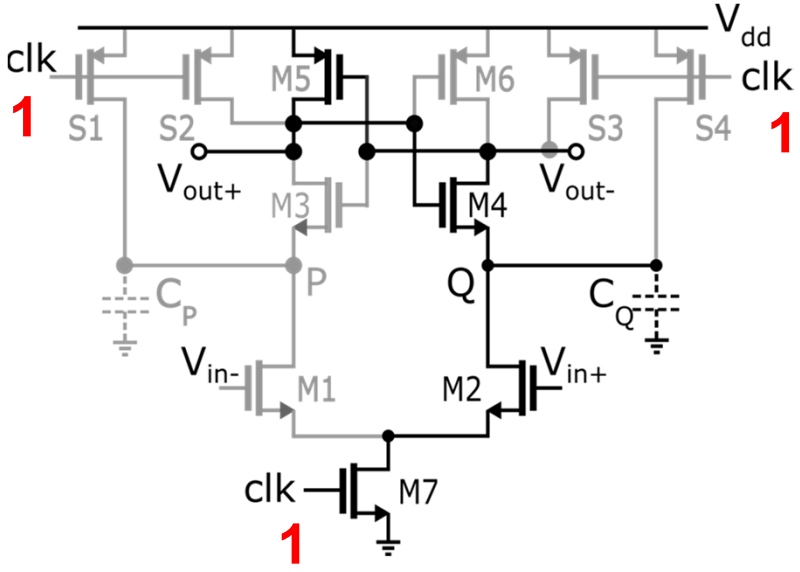


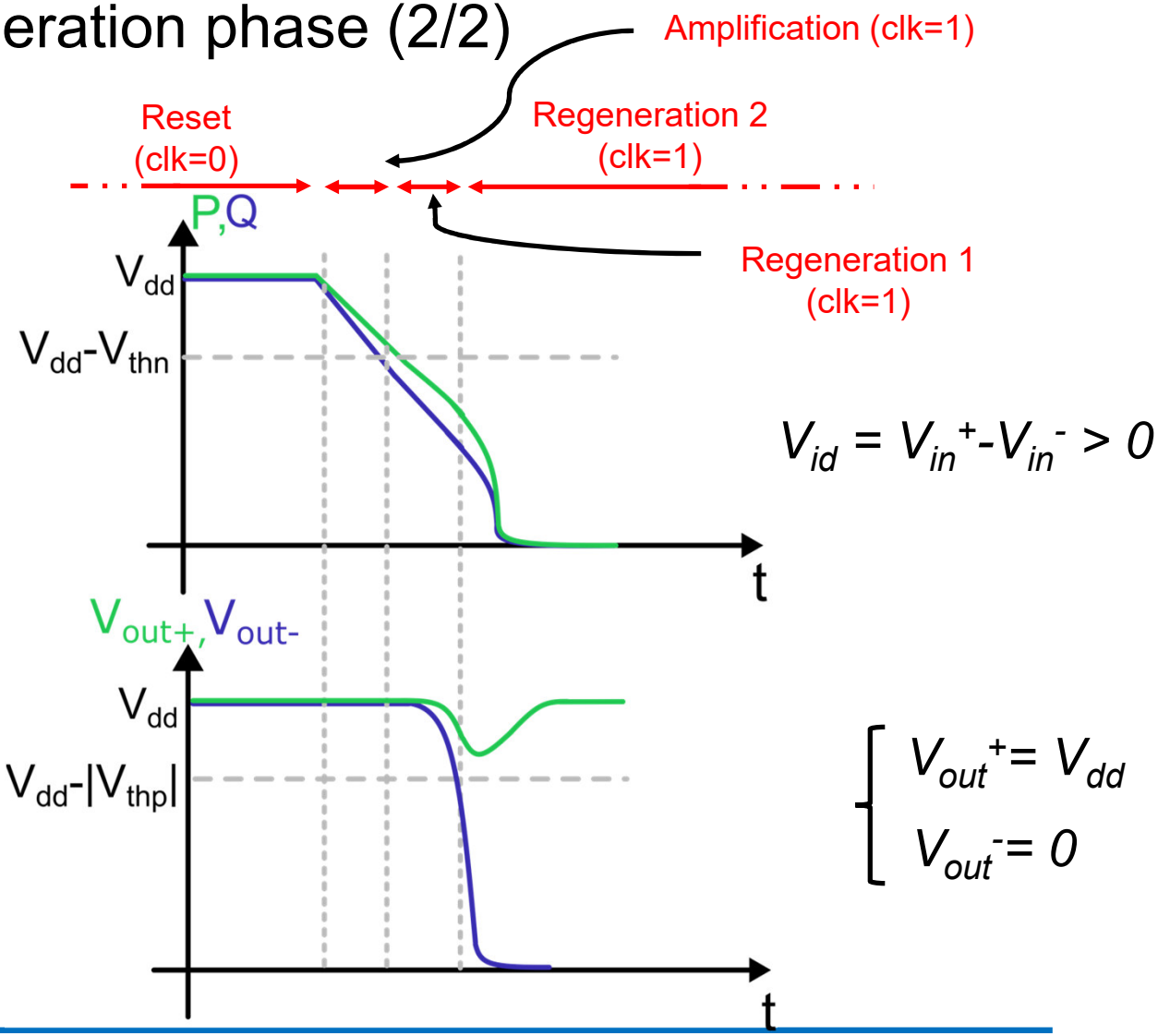
Regeneration phase (2/2)



- When V_{out}^{+} or V_{out}^{-} goes lower than V_{dd}-$|V_{thp}|$, one between M5 and M6 turns on
- Positive feedback of latch M3-M6 brings quickly one output to V_{dd} and the other to ground (rail-to-rail outputs)

Regeneration phase (2/2)



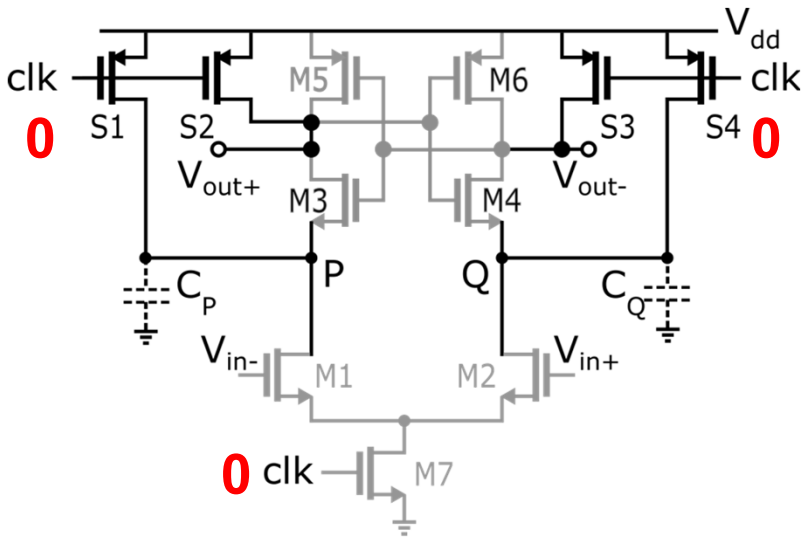


$V_{id} = V_{in}^{+}-V_{in}^{-} > 0$

$$\begin{cases} V_{out}^{+} = V_{dd} \\ V_{out}^{-} = 0 \end{cases}$$

No static power consumption (M3 cuts off the current path from V_{dd} to ground)

(Next) Reset Phase



- S1-S4 recharge node P,Q, V_{out}^+, V_{out}^- to V_{dd}
- Need of a latch to store the result of the comparison during the reset phase