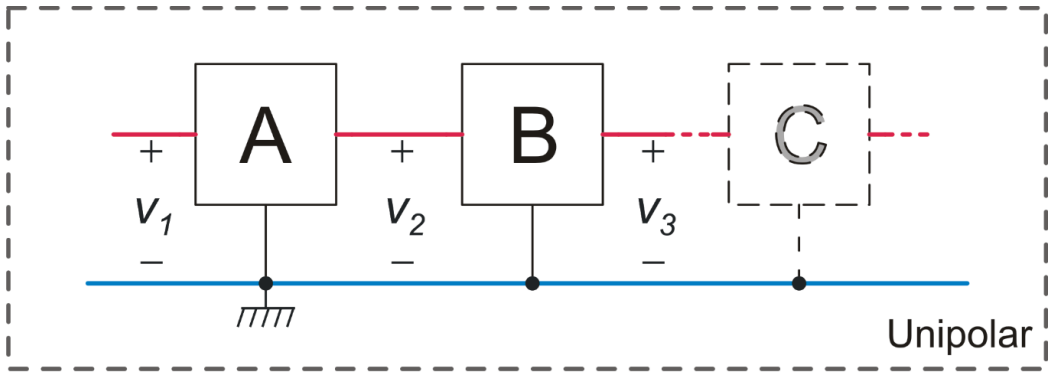
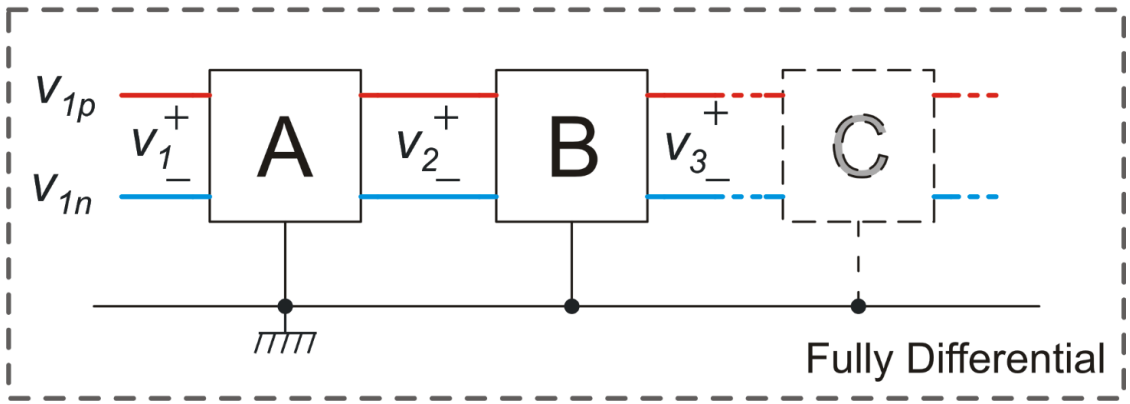
Fully differential and unipolar (single-ended) circuits



Each signal is carried by a **single wire**. Signals (v1, v2, ...) are voltages differences between the wires and a common node (usually gnd).



Each signal is carried by **a wire pair.** Signals (v1, v2 ...) are the voltage difference between the wires that form the pairs..

Fully differential systems: motivations

Advantages of fully differential circuit with respect to unipolar circuits

- Lower sensitivity to interference
- Wider output range
- Better linearity

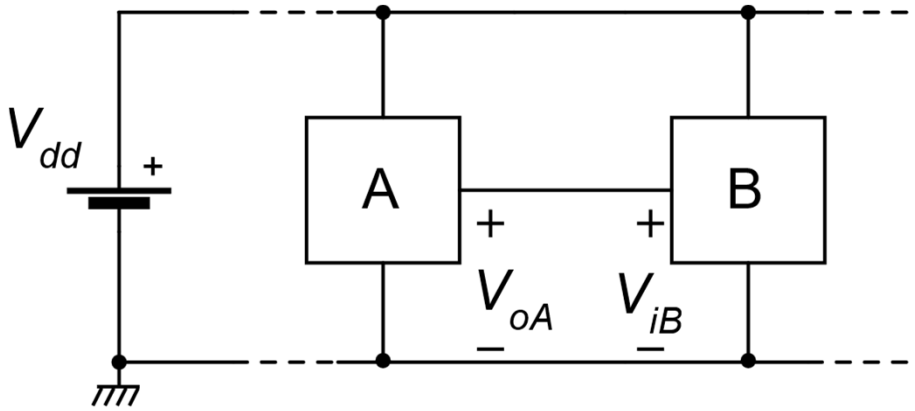
Drawbacks

- Greater complexity (e.g. the feedback networks are formed by twice the components as in the unipolar case).
- Require stabilization of common mode voltages.

Interference coupling mechanisms

- Ground currents (non-uniform gnd)
- Vdd variations
- Capacitive coupling
- Substrate noise

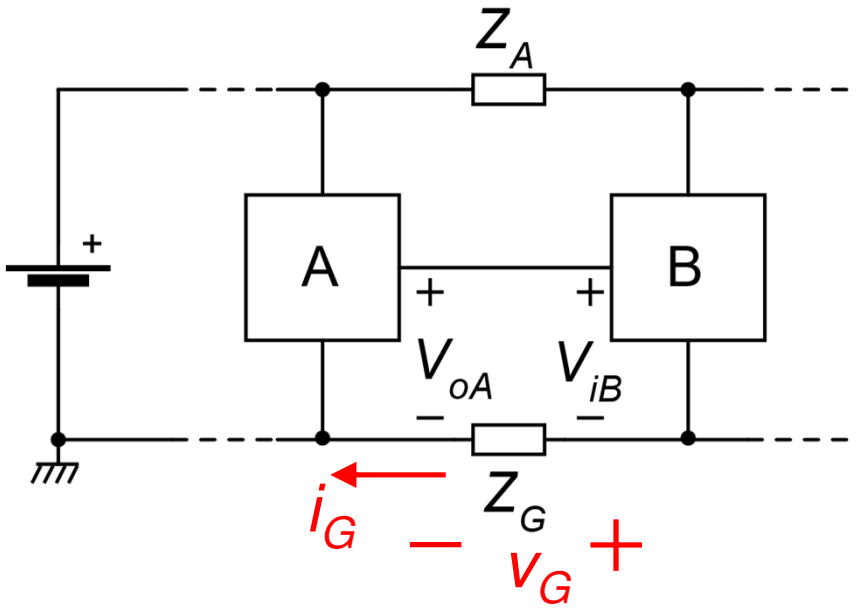
Ground currents: ideal case



All interconnections have null series impedance. Gnd and Vdd can be considered as single nodes.

$$V_{iB} = V_{oA}$$

Ground currents: real case



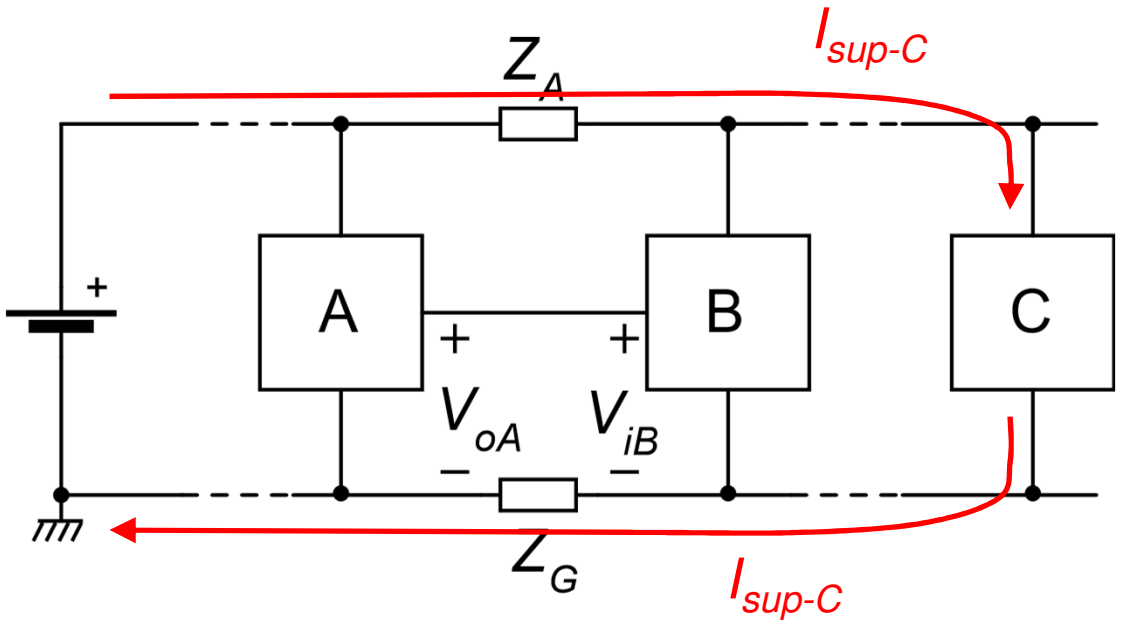
Physical interconnections have non-zero resistance and non-zero inductance

Gnd and Vdd conductors carry considerable currents since they distribute power to all blocks.

Current i_G flowing in the ground conductor creates a difference v_G between the two local grounds in the vicinity of blocks A and B.

$$v_G = Z_G i_G \qquad v_{iB} = v_{oA} - v_G$$

Critical cases



If block C is a digital circuit synchronized by a fast clock, its supply current $I_{sup\text{-}C}$, contains spectral components up to very high frequencies.

The resulting interference on the analog circuits can be difficult to reject since high frequency components can fold-back to low frequencies through sampling (ADCs, SC circuits) or non-linearities.

Origin of the Z_G impedance.

Integrated circuits

- Interconnect lines (tens of Ohm if gnd routing is not performed properly)
- Vias (typically 0.1 Ohm / via)
- Inductance is generally negligible up to several GHz

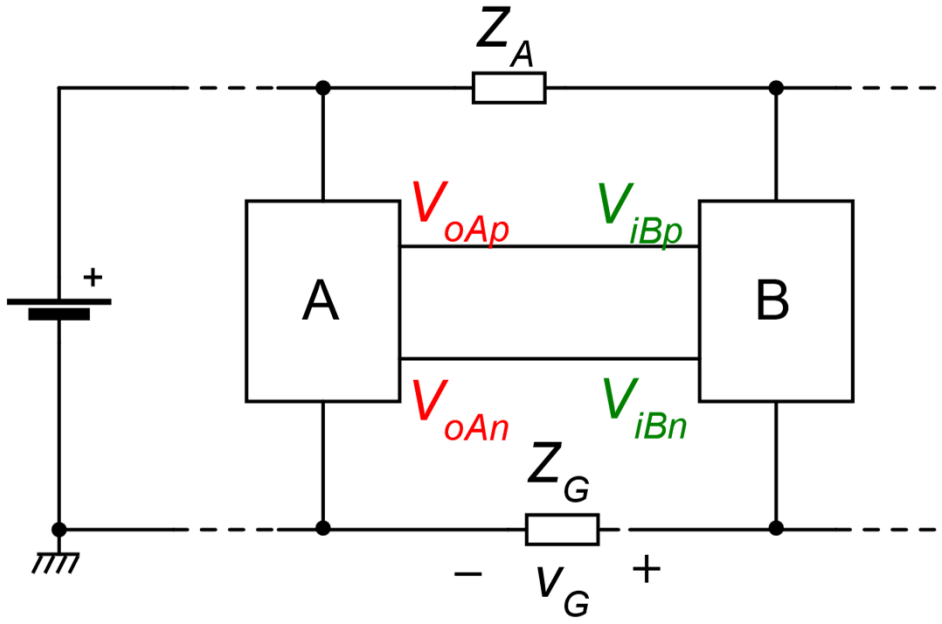
Printed Circuit Boards (PCBs)

- Interconnect resistances are generally the tens of mΩ range
- Inductances can be significant

Board-to-Board interconnections (connecting wires)

- Inductance is generally dominant
- Contact resistance in connectors can be important

Immunity of differential architectures to non-uniform gnd potential



The wires that carry the signals do not experience significant voltage drops, since the currents that pass through them is generally negligible.

$$v_{iBd} = v_{iBp} - v_{iBn}$$

Block B Diff. input

$$\begin{cases} v_{iBp} = v_{oAp} - v_G \\ v_{iBn} = v_{oAn} - v_G \end{cases}$$

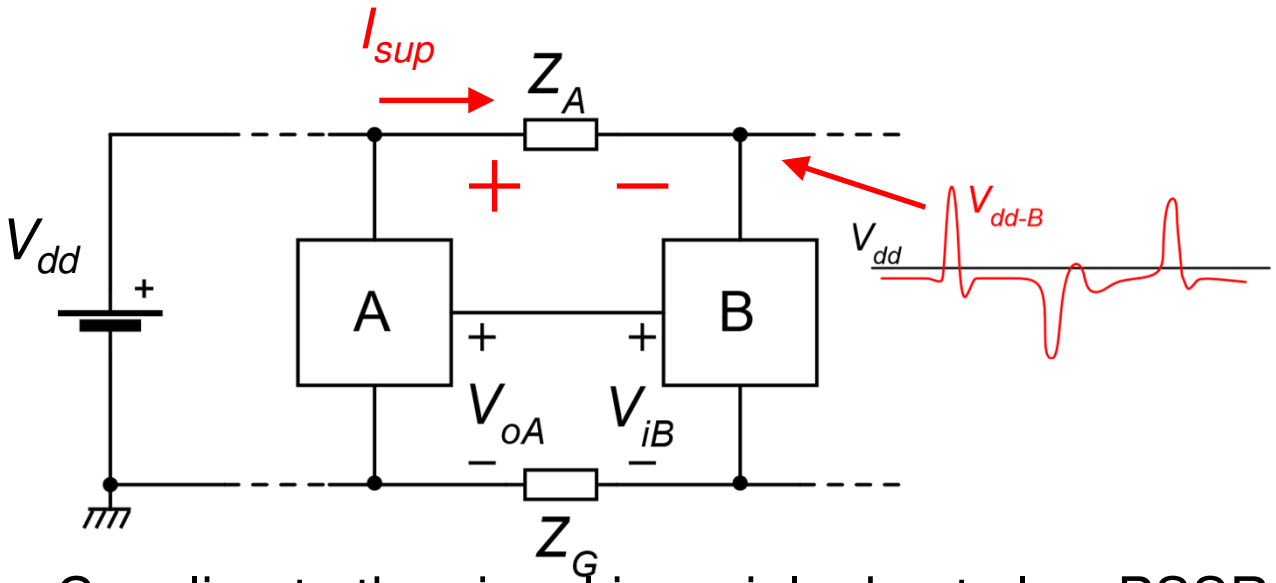
Differential components (signals)

$$v_{iBd} = v_{oAd}$$

Common mode components

$$v_{iBc} = v_{oAc} - v_G$$

V_{dd} variations



The cause of V_{dd} variation is the same that produces the *gnd* non-uniformity.
The effect on the signal is smaller, since V_{dd} is not commonly used as a reference for block-to-block signal transmission.

Coupling to the signal is mainly due to low PSSR. Single ended blocks have a PSSR that decreases steeply at high frequencies.

Note that the V_{dd} variation experienced by block B can be caused by the supply current of blocks A and B themselves. This initial V_{dd} variation can cause an additional supply current variation which, in turn, cause another V_{dd} variation, and so on. This effect may result in an **unstable feedback loop**.

Just a look to datasheets

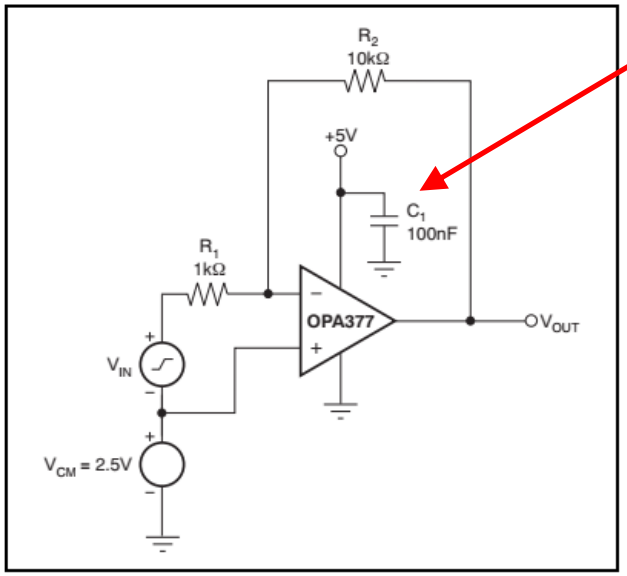
OPERATING CHARACTERISTICS

The OPA377 family of amplifiers has parameters that are fully specified from 2.2V to 5.5V (±1.1V to ±2.75V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are required. Low-loss, 0.1µF bypass capacitors must be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

BASIC AMPLIFIER CONFIGURATIONS

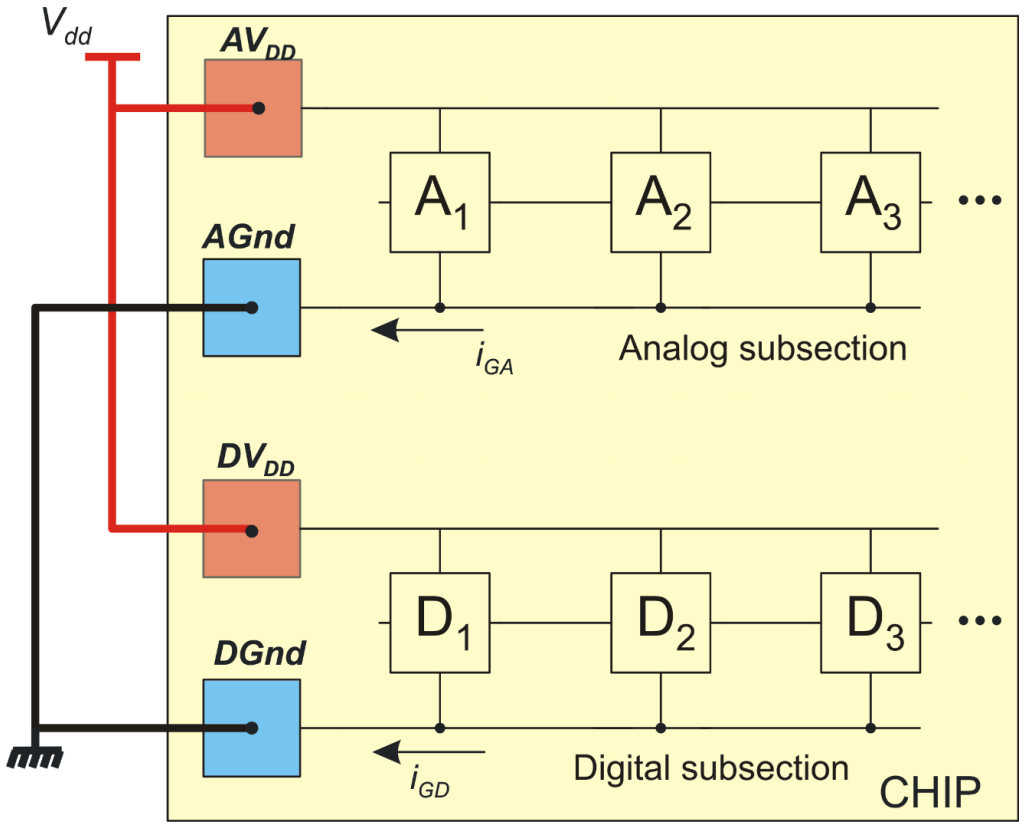


100 nF

Impulsive and high frequency currents (zero mean) are provided by the capacitor and do not run through the interconnections

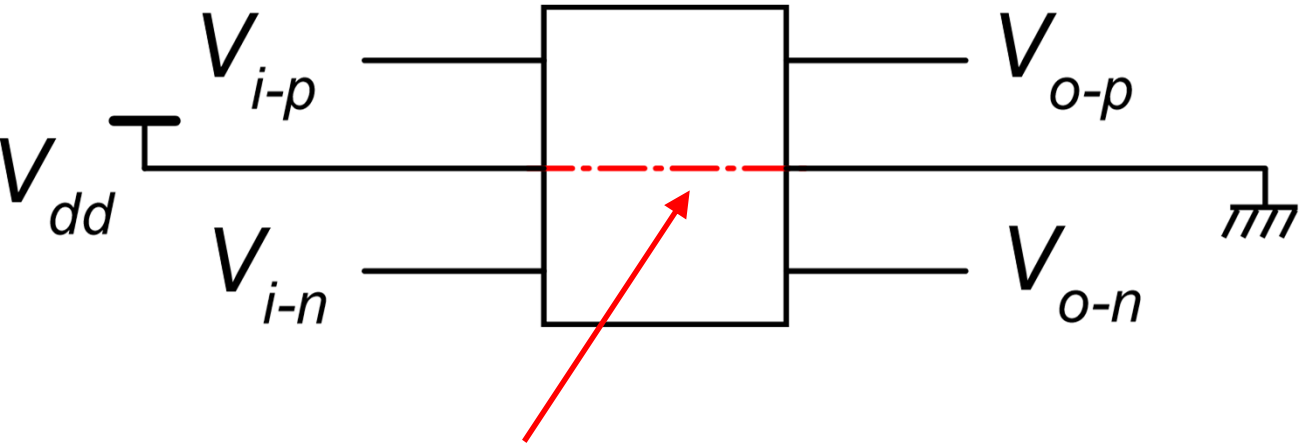
This practice can be also applied inside integrated circuits, but the small values of on-chip capacitors make it effective only for very high frequency components and comes at the expense of large area occupation.

Optimal ground and Vdd distribution in mixed signal ICs.



Sensitive cells, such as analog blocks and noisy circuits, such as digital sub-units should be provided of separate gnd and Vdd power buses. The AGnd (analog gnd) and DGnd (digital gnd) will be connected in a single point, as close as possible to the gnd pad. Even better, they may have separate pads and the connection is made on the PCB.

PSSR and CMRR characteristics of fully differential blocks



Symmetry axis

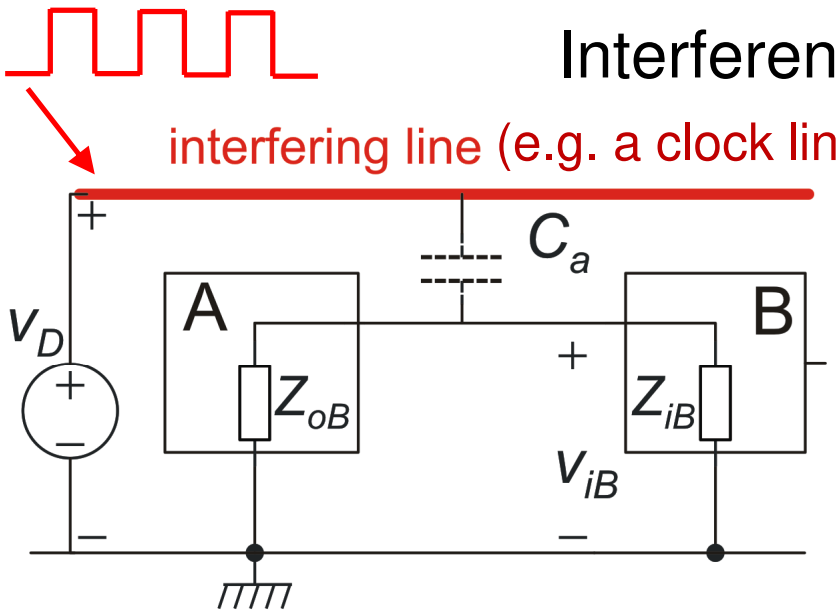
Symmetrical stimuli

- Gnd potential variations
- Vdd variations
- Common mode signals
- Global process errors

All types of symmetrical stimuli cannot produce any effect on the differential output voltage if the circuit is perfectly symmetric.

A reduced amount of leakage from symmetrical stimuli and differential quantities can be due to the unavoidable asymmetries caused by (1) process errors and (2) presence of large differential components due to large input signals.

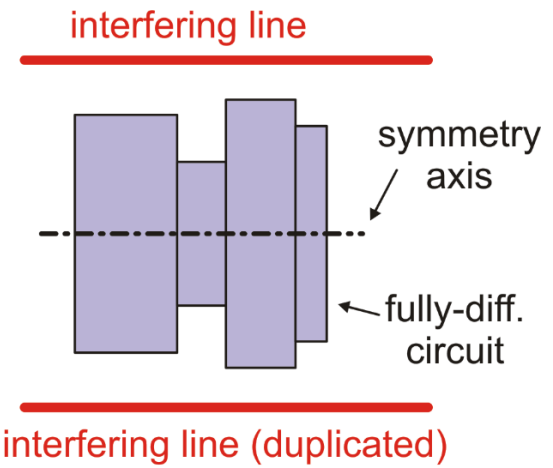
Interference capacitive coupling



$$Z_a = \frac{1}{j\omega C_a} \qquad \text{if } |Z_a| >> |Z_{oA}//Z_{iB}|$$

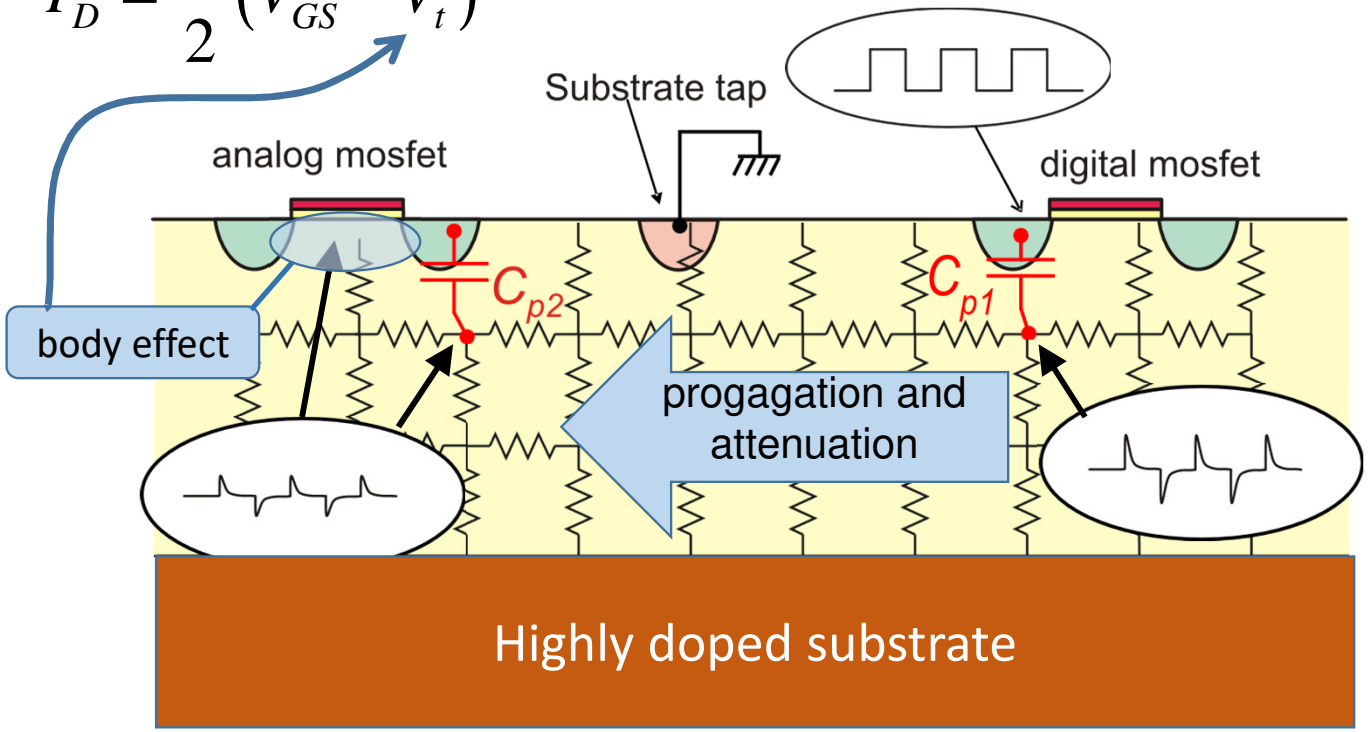
$$V_{iB} = V_D \frac{Z_{oA}//Z_{iB}}{Z_{oA}//Z_{iB} + Z_a} \cong V_D \frac{Z_{oA}//Z_{iB}}{Z_a}$$

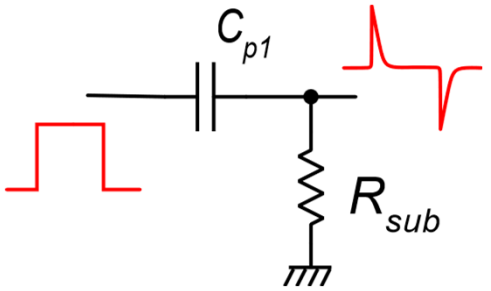
It is possible to exploit the symmetry of a fully-differential block to get same interference signals on the two wires that form the input and output ports. To obtain this a symmetrical layout and environment is essential.



The substrate noise

$$I_D = \frac{\beta}{2}(V_{GS} - V_t)^2$$

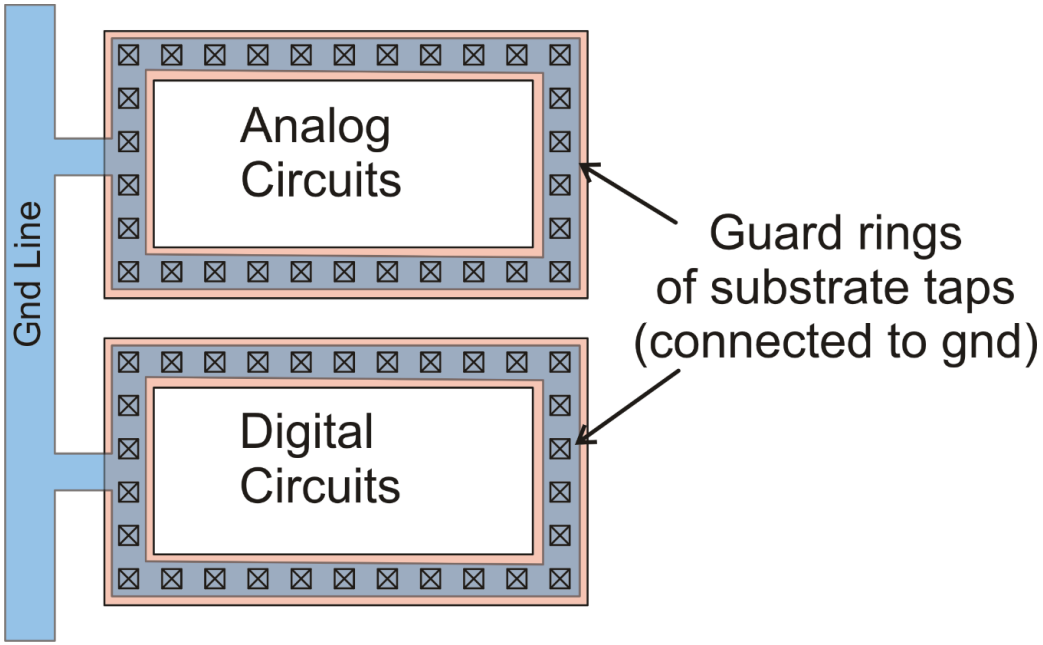




Lightly doped epi-layer

Approaches to reduce substrate noise

- Separate as much as possible the digital and analog circuit
- Use guard rings of substrate taps to reduce propagation

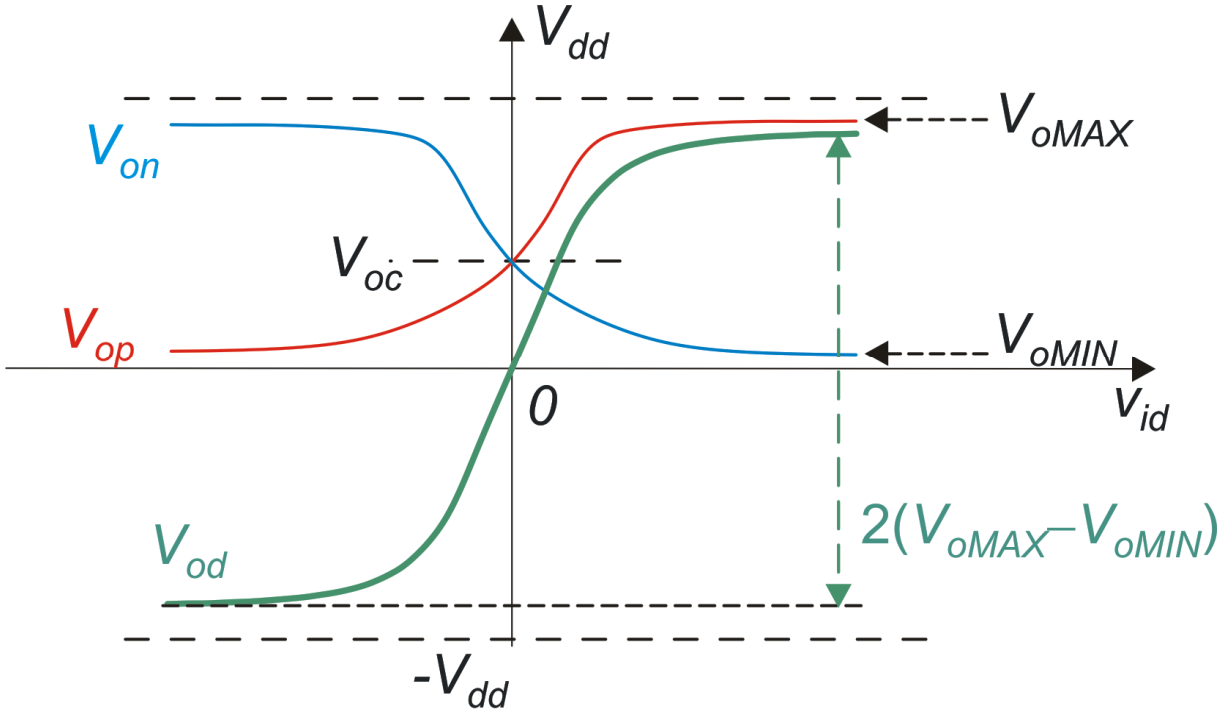


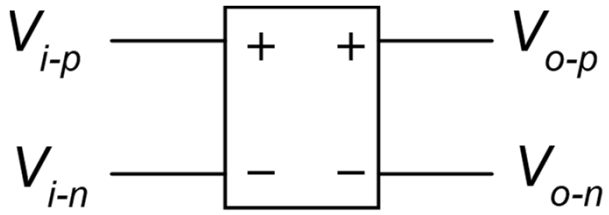
If the sensitive circuits (e.g. analog circuits) and the interference source (i.e. digital circuits) are sufficiently far apart, then substrate noise can be considered uniform over the area of the sensitive circuit.

In fully-differential architectures, it acts as a common mode interference and is rejected

Other advantages of fully-differential circuits: double output range

Let us consider a single supply case



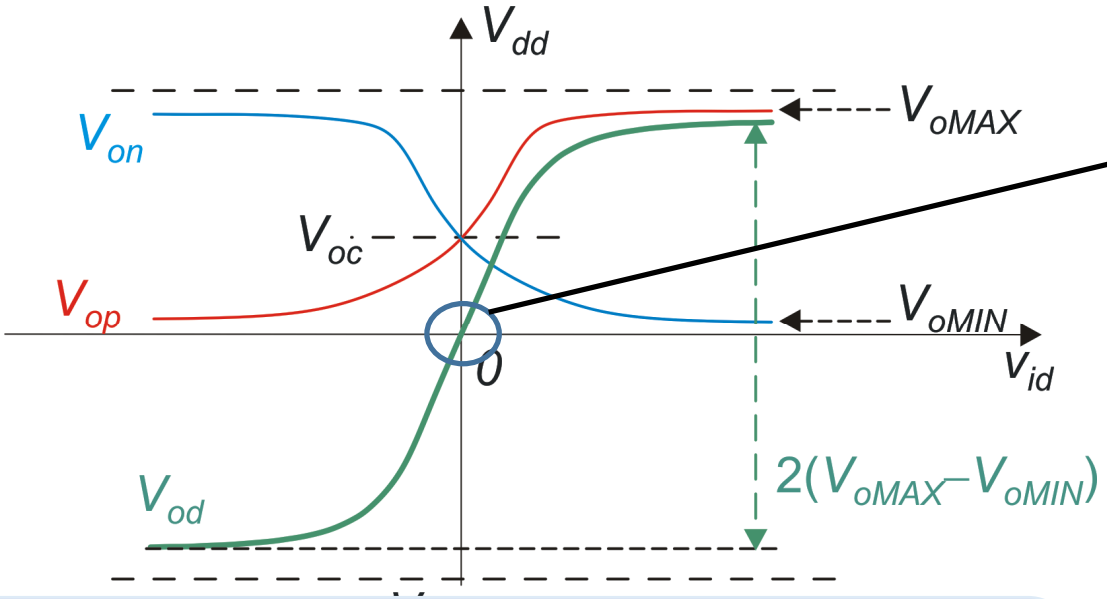


$$V_{od} = V_{op} - V_{on}$$

Each single output (V_{on}, V_{op}) has a range $\Delta V_{o-se} = V_{oMAX} - V_{oMNIN}$

The differentia output (V_{op}–V_{op}) has a range $\Delta V_{o-fd} = 2\left(V_{oMAX} - V_{oMNIN}\right)$

Other advantages of fully-differential circuits: increased linearity



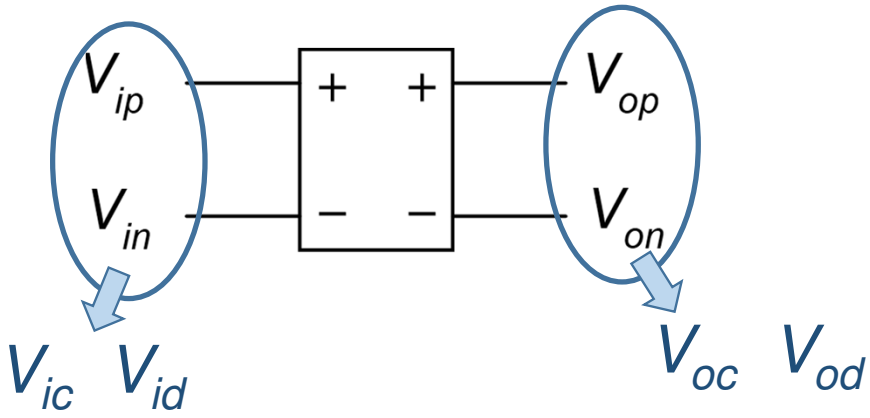
$$V_{od}(-V_{in}) = -V_{od}(V_{in})$$

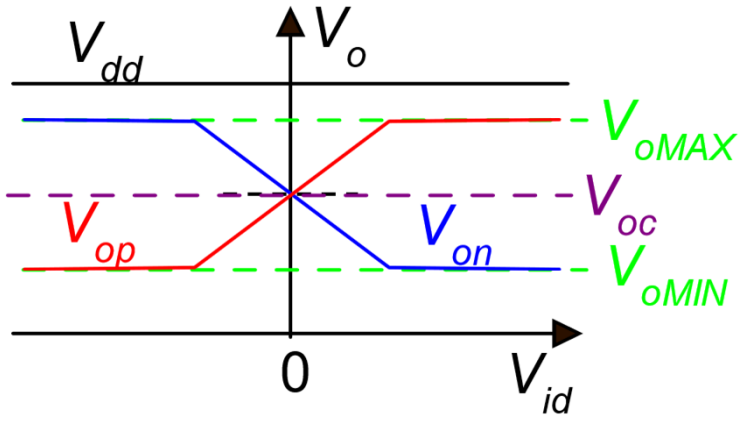
V_{od} has the odd symmetry, then its Taylor polynomial calculated from the origin has no even terms

Greater linearity, lower harmonic distortion (no even harmonics)

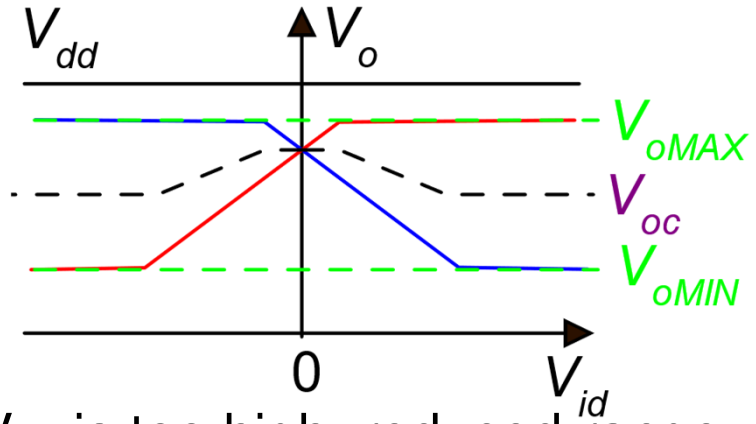
The single outputs (Von,Vop), in principle, have no symmetries, then all terms are generally present in the Taylor polynomial

Fully differential circuits: the need for a stabilized output common mode voltage

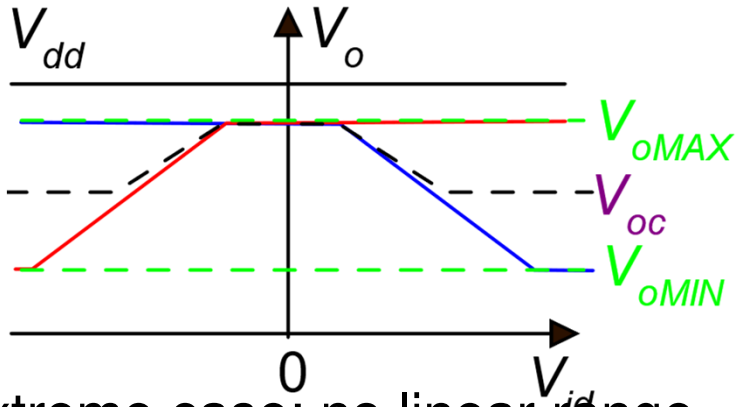




Ideal in-out relationship

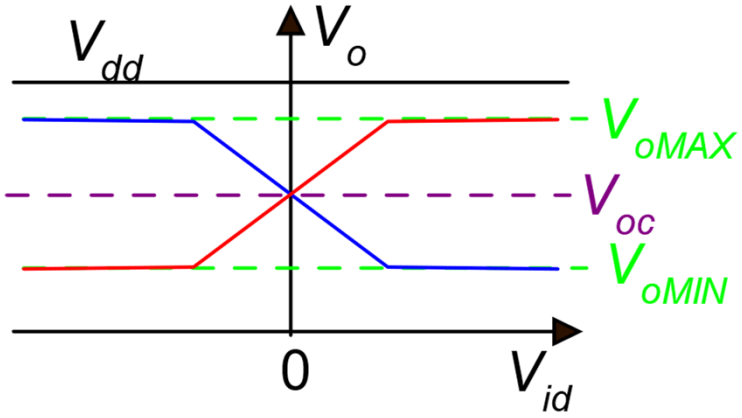


V_{oC} is too high: reduced range

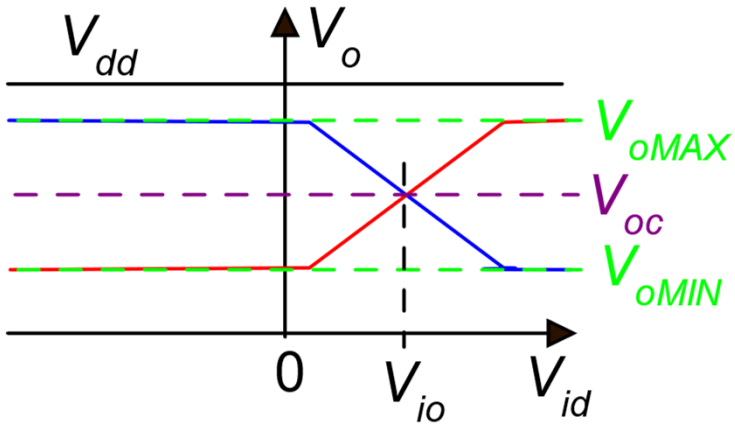


An extreme case: no linear range

Input output characteristics in a fully-differential circuit: the correct feasible case



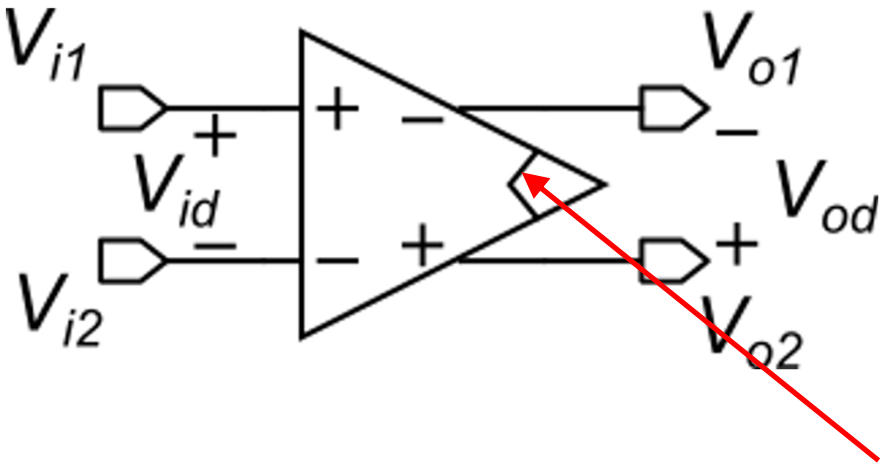
Ideal: zero input offset voltage (not possible, due to process errors)



Possible: there is an offset voltage, but the linearity range is still maximum

In the majority of fully-differential cells, the output common mode voltage should be stabilized and fixed to a convenient value.

The fully-differential operational amplifier: definitions

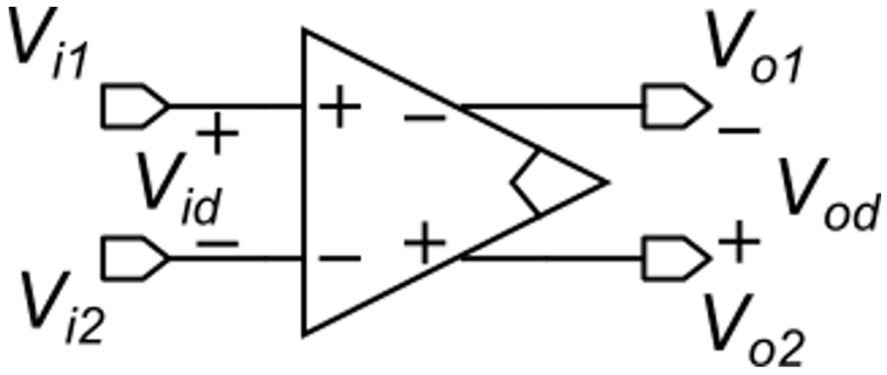


$$\begin{cases} V_{id} = V_{i1} - V_{i2} \\ V_{od} = V_{o2} - V_{o1} \end{cases} \qquad \begin{cases} V_{ic} = \dfrac{V_{i1} + V_{i2}}{2} \\ V_{oc} = \dfrac{V_{o2} + V_{o1}}{2} \end{cases}$$

The inverting output is placed on the same side of the non-inverting input to simplify drawing of closed loop configurations

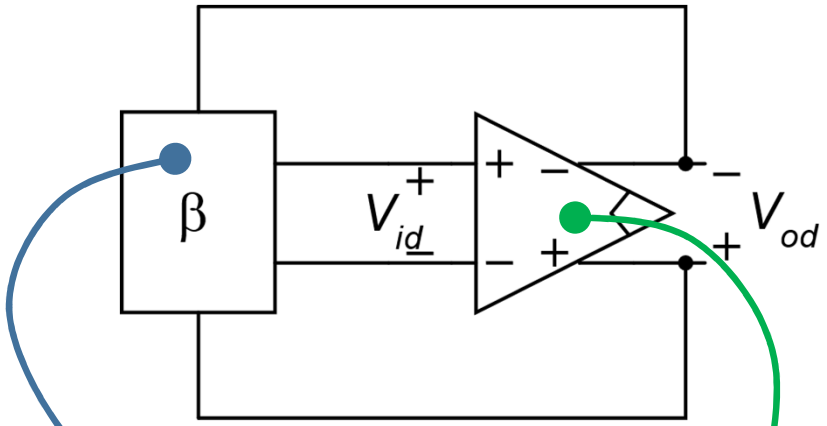
This symbol means that the amplifier includes a common mode stabilization circuit

The fully-differential operational amplifier: properties



$$\begin{cases} V_{od} = A\left(V_{id} - v_n\right) \; A > 0 \quad \left(\left|A\right| >> 1\right) \\ V_{oC} = V_{CMO} = constant \end{cases}$$

Closed loop configuration: V_{id}



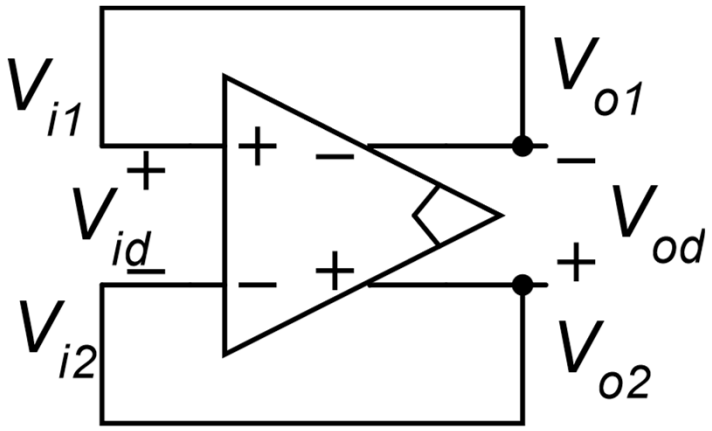
$$V_{id} = \beta V_{od} + V_k$$
$$V_{od} = A\left(V_{id} - v_n\right)$$

Contribution of noise to the input differential voltage in closed loop

$$V_{id} \cong v_n' \equiv \frac{\beta A}{\beta A - 1} v_n$$

Filtered version of the input noise voltage

The "unity-gain" configuration



It is common practice to indicate this configuration by "unity-gain".
This is improper because there is no available port to insert a signal.
However, this configuration is particularly useful in switched-capacitor circuits.

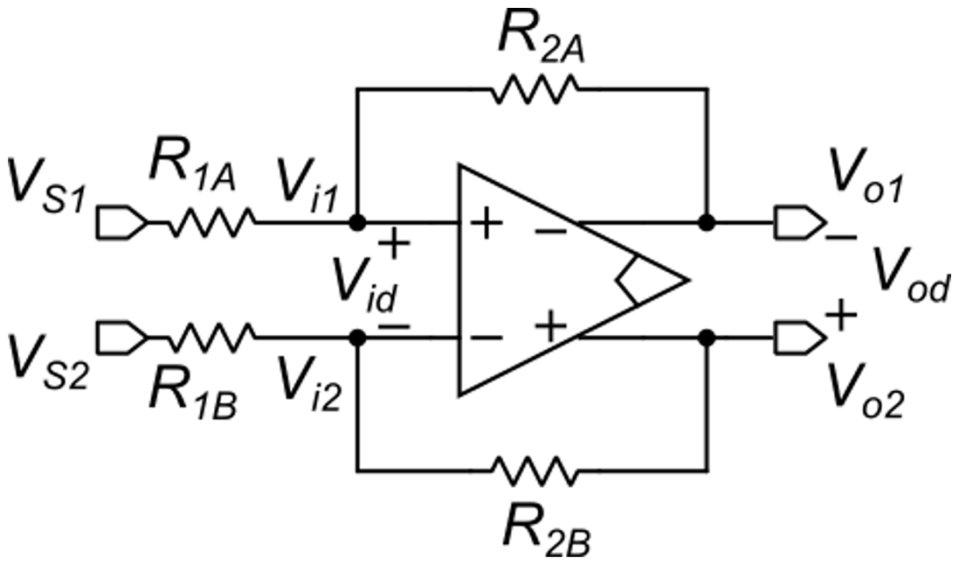
$$V_{id} = -V_{od} \qquad \beta = -1$$

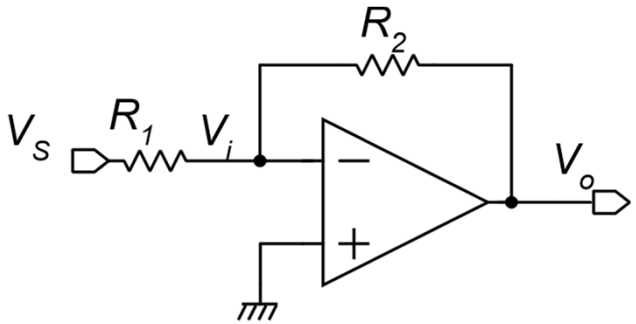
$$V_{id} \cong v_n \qquad V_{od} \cong -v_n$$

$$V_{ic} = V_{oc} = V_{CMO}$$

$$V_{i1} = V_{CMO} + \frac{v_n}{2}; \qquad V_{i2} = V_{CMO} - \frac{v_n}{2}$$

Fully differential amplifier with resistive feedback

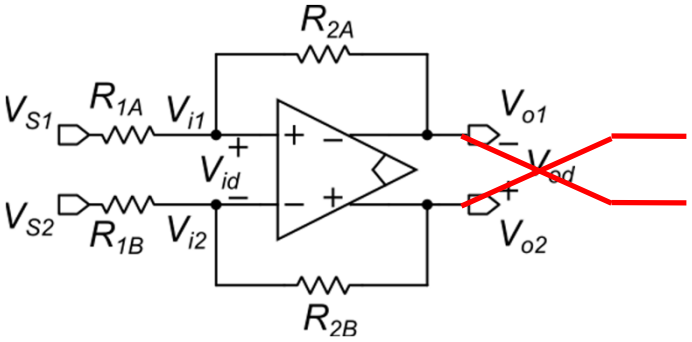




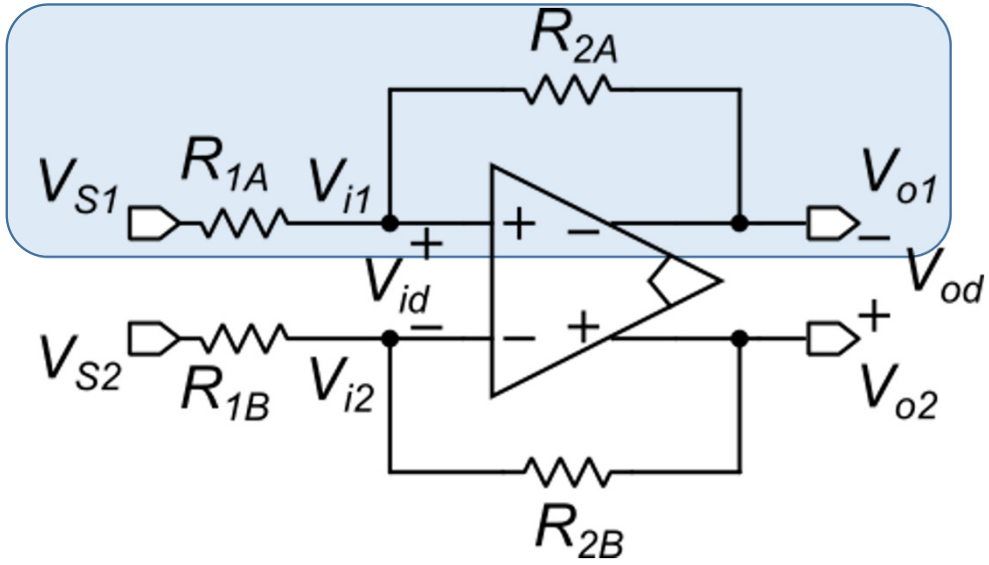
Analogous S/E configuration: inverting amplifier.

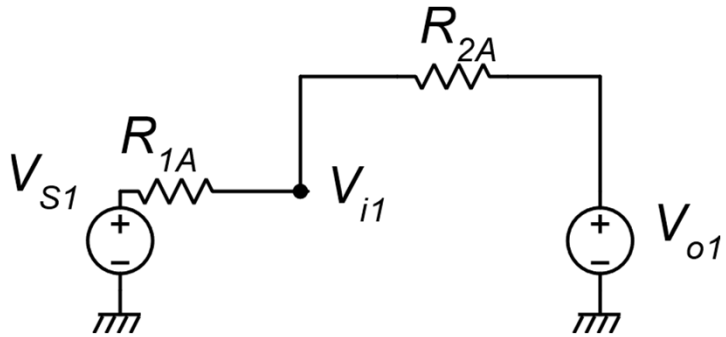
The fully-diff. version needs twice the passive components

In fully-differential architecture, speaking of inverting and non-inverting topologies is meaningless, since a sign change can be obtained by simply swapping the wires



Fully differential amplifier with resistive feedback





$$V_{i1} = V_{o1}\frac{R_{1A}}{R_{1A}+R_{2A}} + V_{S1}\frac{R_{2A}}{R_{1A}+R_{2A}}$$

β_1 $\qquad$ $1-\beta_1$

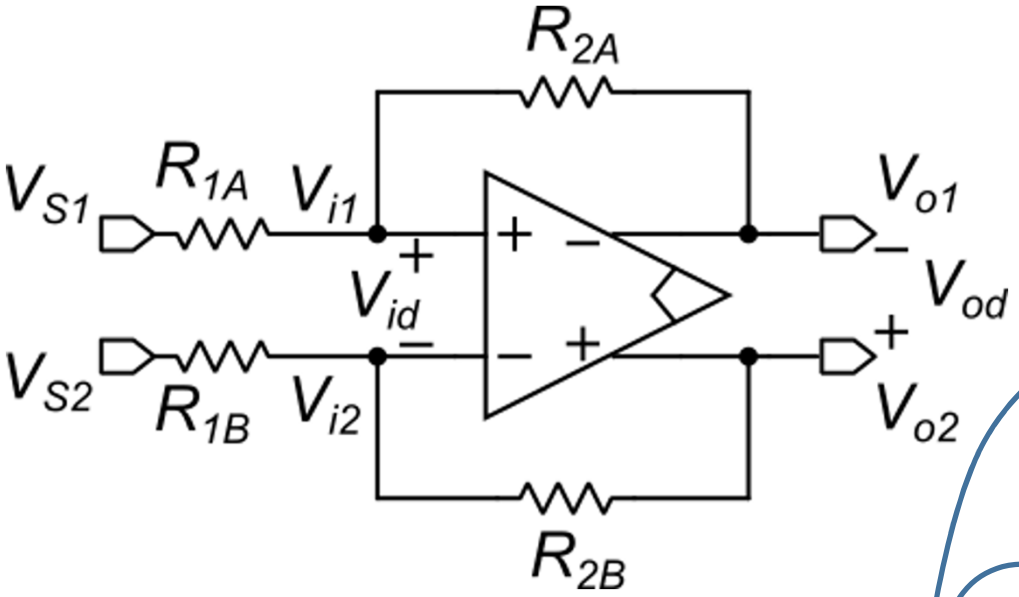
$$V_{i1} = V_{o1}\beta_1 + V_{S1}(1-\beta_1)$$

$$V_{i2} = V_{o2}\beta_2 + V_{S2}(1-\beta_2)$$

$$\beta_1 = \frac{R_{1A}}{R_{1A}+R_{2A}}$$

$$\beta_2 = \frac{R_{1B}}{R_{1B}+R_{2B}}$$

Fully differential amplifier with resistive feedback



$$\beta_1 = \frac{R_{1A}}{R_{1A}+R_{2A}} \qquad \beta_2 = \frac{R_{1B}}{R_{1B}+R_{2B}}$$

Nominally $\beta_1=\beta_2$, but unavoidable process errors (local errors) make them different

It is convenient to split the two coefficients as a mean value and a difference:

$$\beta_1 = \beta_m + \frac{\Delta\beta}{2}; \quad \beta_2 = \beta_m - \frac{\Delta\beta}{2}$$

$$\begin{cases} V_{i1} = V_{o1}\beta_1 + V_{S1}(1-\beta_1) \\ V_{i2} = V_{o2}\beta_2 + V_{S2}(1-\beta_2) \end{cases}$$

$$\begin{cases} V_{i1} = V_{o1}\left(\beta_m + \frac{\Delta\beta}{2}\right) + V_{S1}\left(1-\beta_m - \frac{\Delta\beta}{2}\right) \\ V_{i2} = V_{o2}\left(\beta_m - \frac{\Delta\beta}{2}\right) + V_{S2}\left(1-\beta_m + \frac{\Delta\beta}{2}\right) \end{cases}$$

Fully differential amplifier with resistive feedback

Differential mode analysis

$$\begin{cases} V_{i1} = V_{o1}\left(\beta_m + \dfrac{\Delta\beta}{2}\right) + V_{S1}\left(1-\beta_m - \dfrac{\Delta\beta}{2}\right) & - \\ V_{i2} = V_{o2}\left(\beta_m - \dfrac{\Delta\beta}{2}\right) + V_{S2}\left(1-\beta_m + \dfrac{\Delta\beta}{2}\right) & + \end{cases}$$

$$\begin{cases} V_{Sd} = V_{S2} - V_{S1} \\ V_{Sc} = \dfrac{V_{S1}+V_{S2}}{2} \end{cases}$$

$$V_{i2} - V_{i1} = \left(V_{o2} - V_{o1}\right)\beta_m - \left(\frac{V_{o1}+V_{o2}}{2}\right)\Delta\beta + \left(V_{S2}-V_{S1}\right)\left(1-\beta_m\right) + \frac{V_{S1}+V_{S2}}{2}\Delta\beta$$

$$\underbrace{V_{i2} - V_{i1}} = V_{od}\beta_m - V_{oc}\Delta\beta + V_{Sd}\left(1-\beta_m\right) + V_{Sc}\Delta\beta$$

$$-V_{id} \cong -v_n$$

Fully differential amplifier with resistive feedback

$$-v_n = V_{od}\beta_m - V_{oc}\Delta\beta + V_{Sd}(1-\beta_m) + V_{Sc}\Delta\beta$$

$$-V_{od}\beta_m = +v_n + V_{Sd}(1-\beta_m) + (V_{Sc}-V_{oc})\Delta\beta$$

$$V_{od} = -\frac{v_n}{\beta_m} - V_{Sd}\frac{(1-\beta_m)}{\beta_m} - (V_{Sc}-V_{oc})\frac{\Delta\beta}{\beta_m}$$

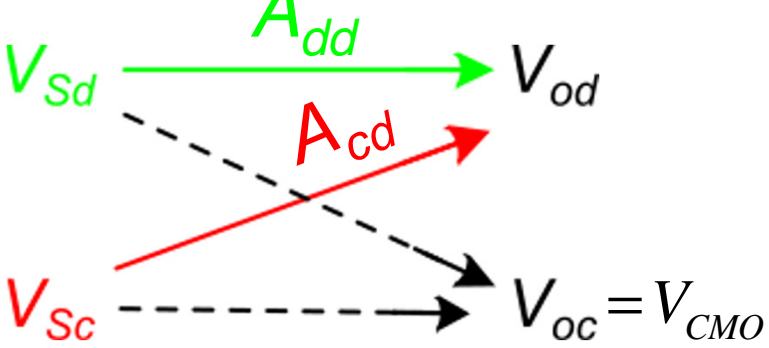
V_{CMO}

$$v_{od-noise} = -\frac{v_n}{\beta_m}$$

$$A_{dd} = -\frac{(1-\beta_m)}{\beta_m}$$

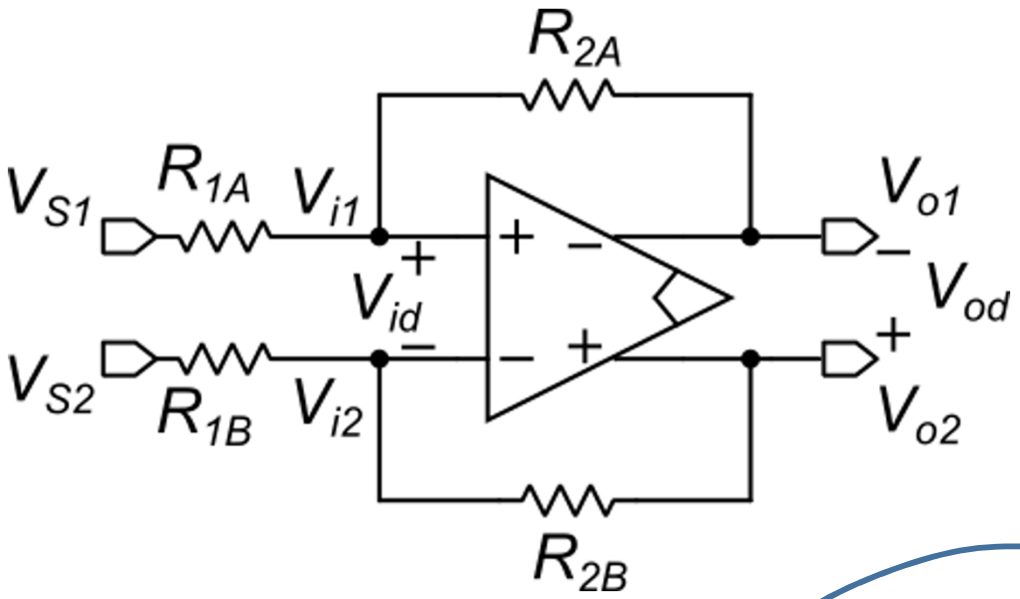
$$A_{cd} = -\frac{\Delta\beta}{\beta_m}$$

relative matching error



$$CMRR = \left|\frac{A_{dd}}{A_{cd}}\right| = |A_{dd}| \cdot \left|\frac{\Delta\beta}{\beta_m}\right|^{-1}$$

Fully differential amplifier with resistive feedback



$$A_{dd} = -\frac{(1-\beta_m)}{\beta_m} \qquad \beta_m = \frac{\beta_1 + \beta_2}{2}$$

$$\beta_1 = \frac{R_{1A}}{R_{1A} + R_{2A}} \qquad \beta_2 = \frac{R_{1B}}{R_{1B} + R_{2B}}$$

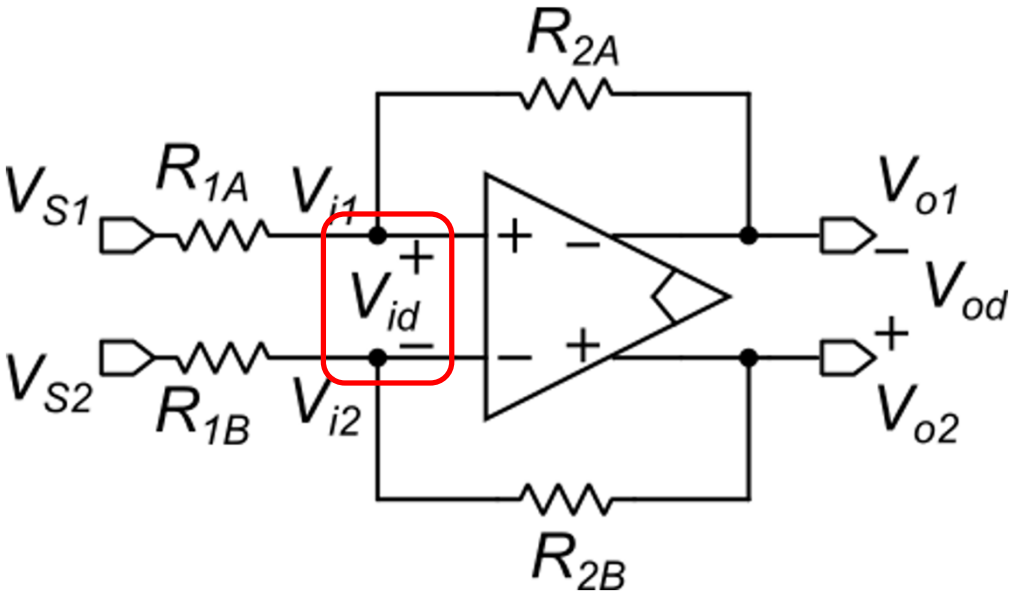
Nominal case:

$$\left.\begin{aligned} R_{1A} &= R_{1B} = R_1 \\ R_{2A} &= R_{2B} = R_2 \end{aligned}\right\}$$

$$\beta_1 = \beta_2 = \beta_m = \frac{R_1}{R_1 + R_2} \equiv \beta$$

$$A_{dd} = -\frac{(1-\beta)}{\beta} = -\frac{R_2}{R_1 + R_2}\frac{R_1 + R_2}{R_1} = -\frac{R_2}{R_1}$$

Fully differential amplifier with resistive feedback



$$\begin{cases} v_{i1} = v_{o1}\left(\beta_m + \dfrac{\Delta\beta}{2}\right) + v_{S1}\left(1 - \beta_m - \dfrac{\Delta\beta}{2}\right) \times \dfrac{1}{2} \\ v_{i2} = v_{o2}\left(\beta_m - \dfrac{\Delta\beta}{2}\right) + v_{S2}\left(1 - \beta_m + \dfrac{\Delta\beta}{2}\right) \times \dfrac{1}{2} \end{cases}$$

We do not know the input common mode voltage

$$V_{ic} = \beta V_{CMO} + (1-\beta) v_{Sc}$$

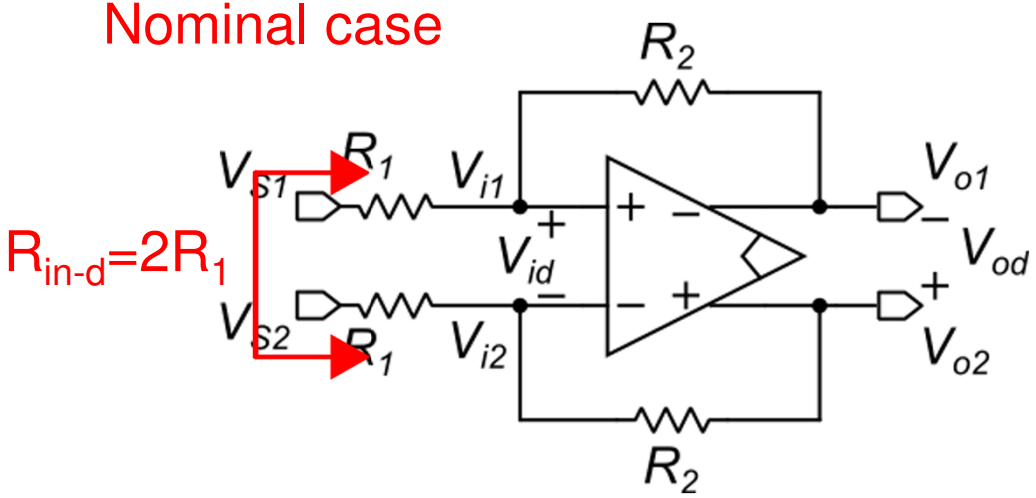
Generally, determination of the common mode voltage does not require high accuracy. We can use the nominal case.

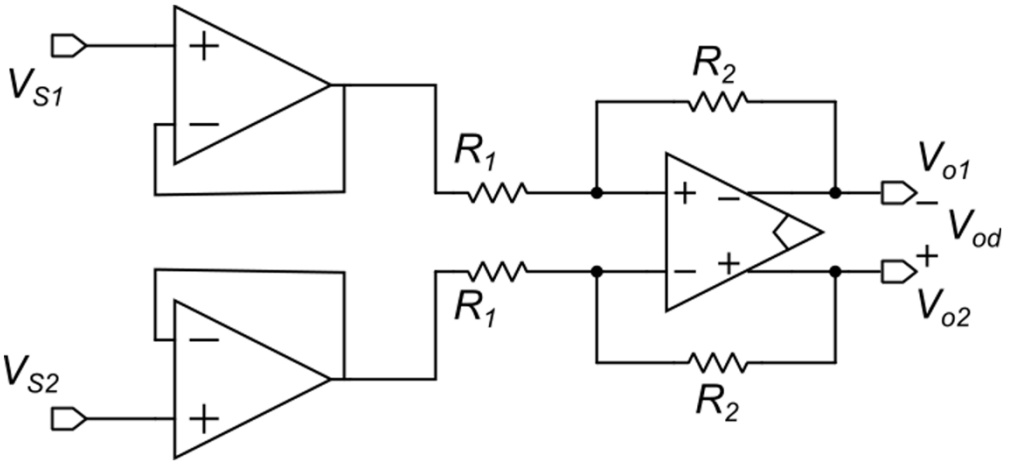
$$\begin{cases} \beta_m = \beta \\ \Delta\beta = 0 \end{cases}$$

We have to check that for all possible values of v_{SC}, the input common mode voltage does not exceed the amplifier input CM range

3-op-amp fully-differential instrumentation amplifier

Nominal case

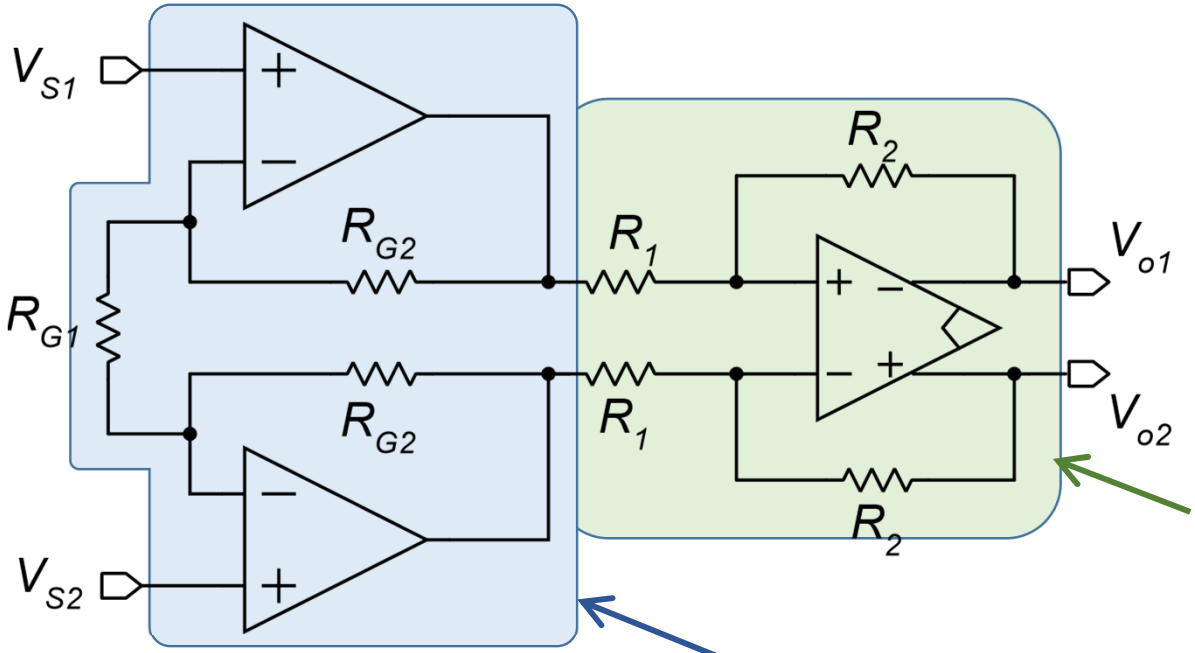




This circuit alone cannot be used as an instrumentation amplifier since it has too low an input resistance

We could use input buffers built with single-ended operational amplifiers. But there is a more versatile option ...

3-op-amp fully-differential instrumentation amplifier



$$A_{dd-tot} = -\left(1+2\frac{R_{G2}}{R_{G1}}\right)\frac{R_2}{R_1}$$

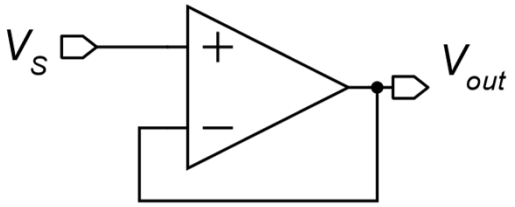
$$A_{dd1} = 1+2\frac{R_{G2}}{R_{G1}} \qquad A_{cc1} = 1$$

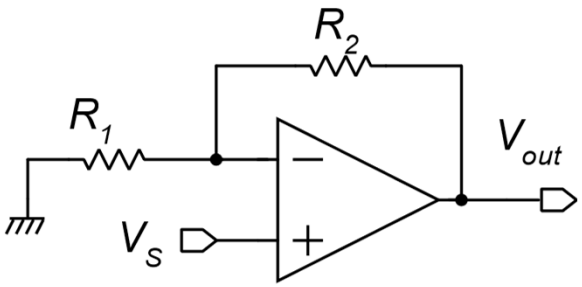
$$A_{cd1} \cong 0$$

First stage: is identical to the first stage of the single-ended in-amp

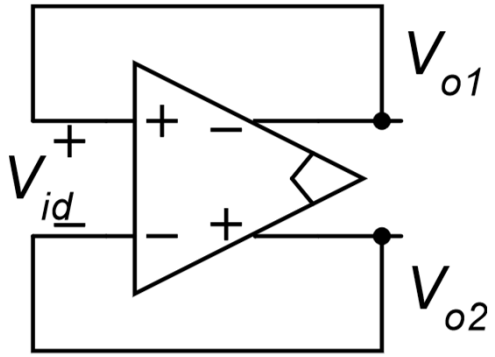
Second stage: reject the input common mode voltage and produces a stabilized output common mode voltage. Often its gain is set to 1

Versatility limits of the fully-differential operational amplifier





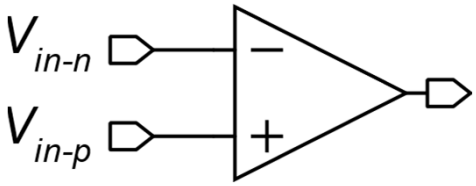
These are topologies that present a high input resistance. They cannot be implemented in the fully differential domain using a FD op-amp.

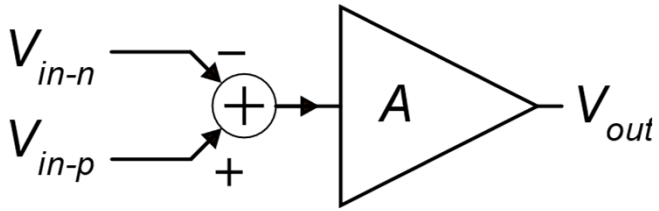


For example, the fully-differential unity-gain configuration, differently from its S/E counterpart, cannot work as a buffer. There is not an input port available for the signal.

Versatility limits of the fully-differential operational amplifier

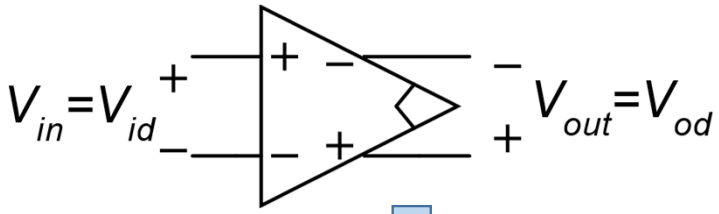
Single ended op-amp
(electrical symbol)

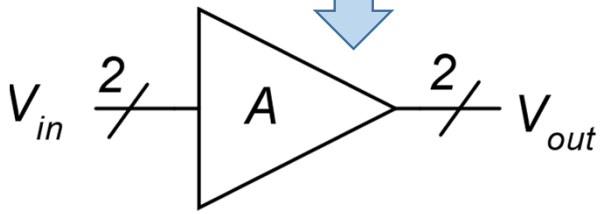




Functional representation

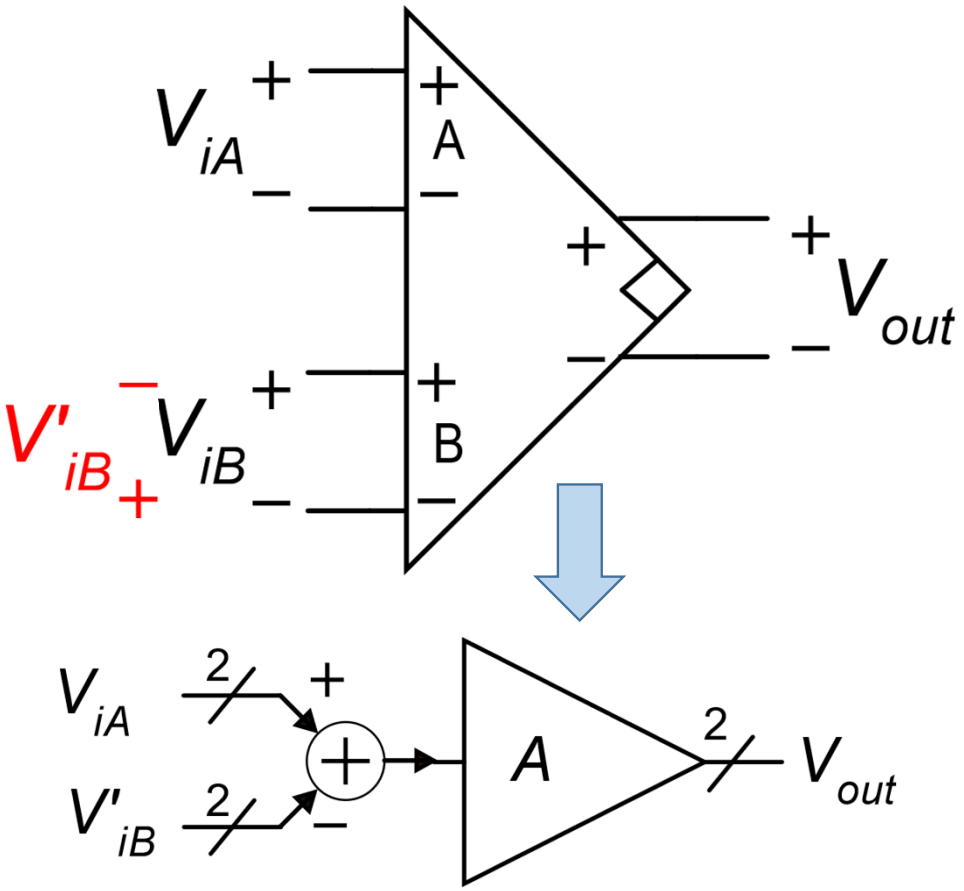
Fully-differential op-amp
(electrical symbol)





Functional representation: in fully differential architectures every wire pair is a single signal

The DDA: Difference Differential Amplifier



$$V_{out} = A\left(V_A + V_B\right)$$

$$V_{out} = A\left(V_{iA} - V'_{iB}\right)$$

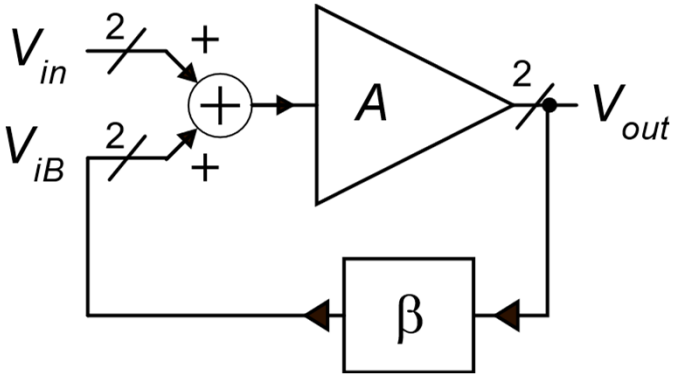
$$\frac{V_{out}}{A} = \left(V_{iA} - V'_{iB}\right)$$

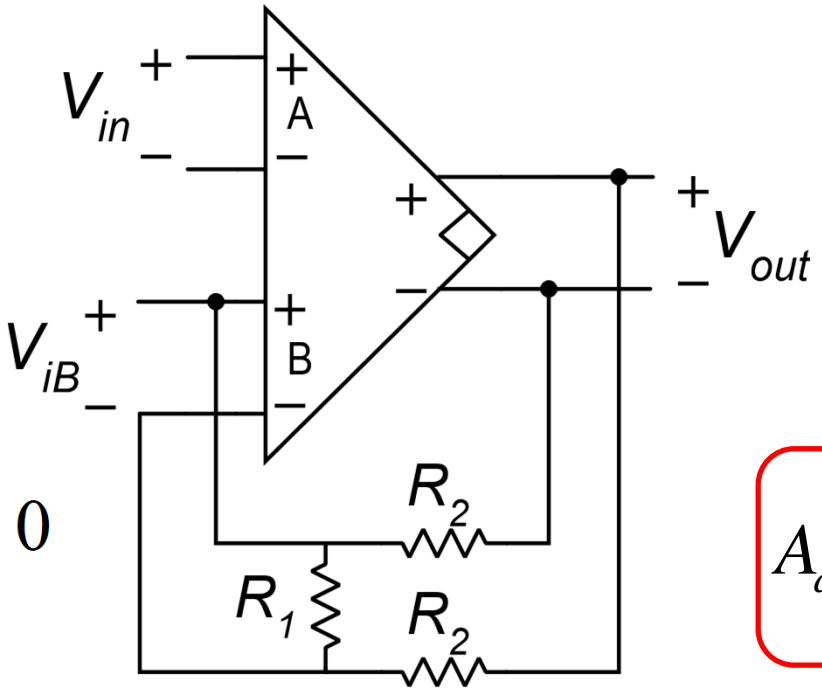
In a closed loop configuration, if the circuit is stable and the amplifier is in its linearity range (A>>1):

$$V_{iA} \cong V'_{iB} = -V_{iB}$$

This is the equivalent of the virtual short circuit in DDAs. Note that, individually V_{iA} and V_{iB} can be large

DDA-based instrumentation amplifier





$$V_{iB} = -\frac{R_1}{R_1 + 2R_2} V_{out}$$

$$\beta = -\frac{R_1}{R_1 + 2R_2}$$

$$V_{iB} = \beta V_{out} \quad \text{with} \quad \beta < 0$$

$$V_{iA} = V_{in}$$

$$A_{dd} = \frac{V_{out}}{V_{in}} = \frac{R_1 + 2R_2}{R_1}$$

$$V_{iA} = -V_{iB} \Rightarrow V_{in} = -\beta V_{out} \qquad V_{out} = -\frac{1}{\beta} V_{in} \qquad A_{dd} = -\frac{1}{\beta}$$