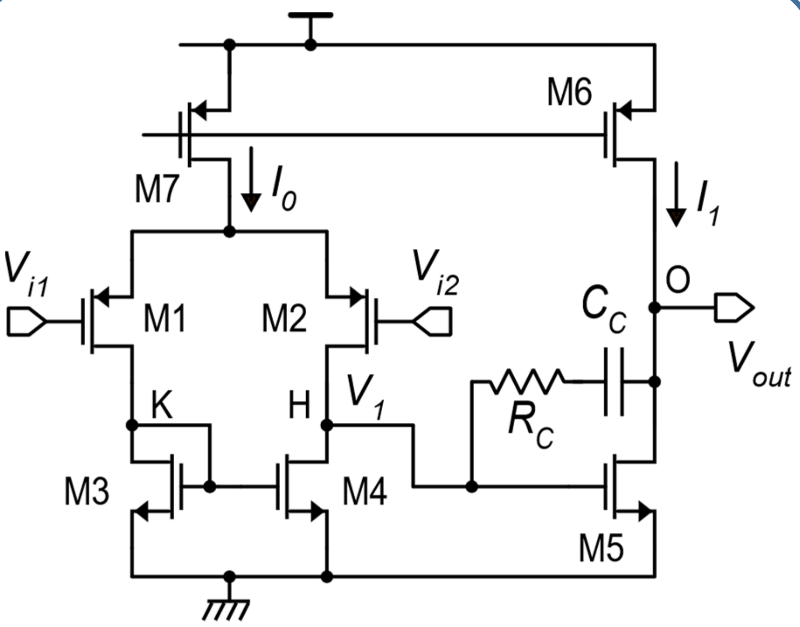
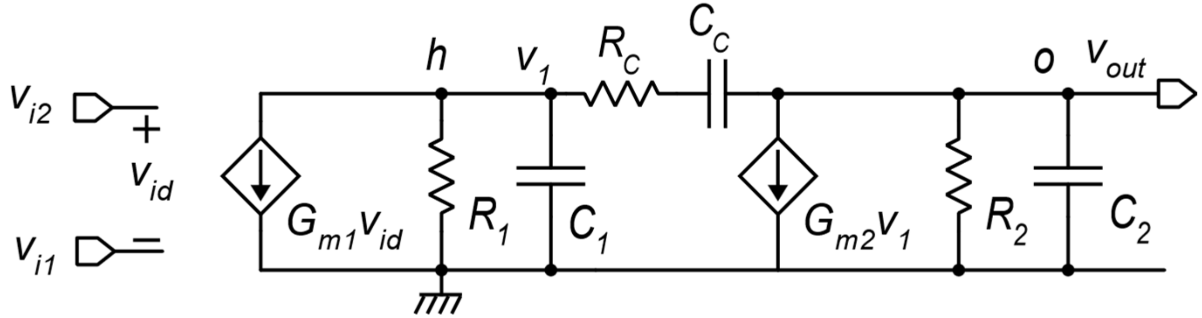
Two-stage op-amp: design for *GBW* and Phase Margin



Topology



Small signal equivalent circuit

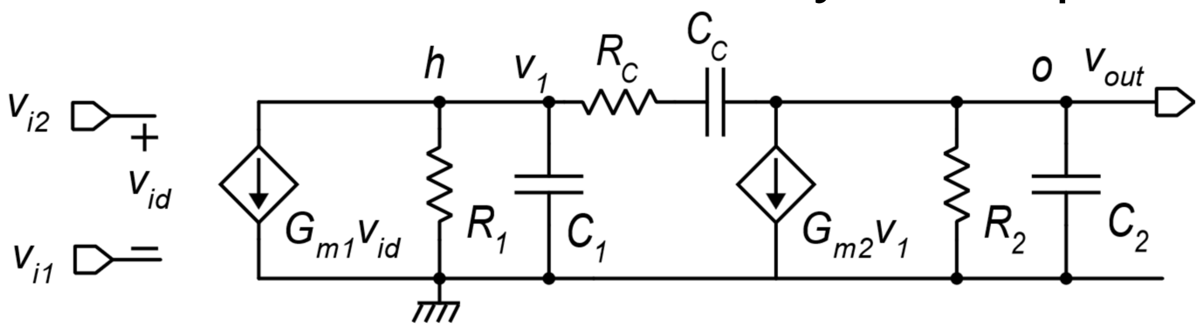
Singularities

$$\omega_p \cong \frac{1}{R_1 G_{m2} R_2 C_C}$$

$$\omega_2 \cong \frac{G_{m2}}{(C_1 + C_2)}\left(1 + \frac{C_S}{C_C}\right)^{-1} \qquad C_S = \frac{C_1 C_2}{C_1 + C_2}$$

$$\omega_3 \cong \frac{1}{R_C\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_C}\right)^{-1}} \qquad s_z = \frac{-1}{C_C\left(R_C - \frac{1}{G_{m2}}\right)}$$

Preliminary assumptions



$$s_z = \frac{-1}{C_C\left(R_C - \frac{1}{G_{m2}}\right)}$$

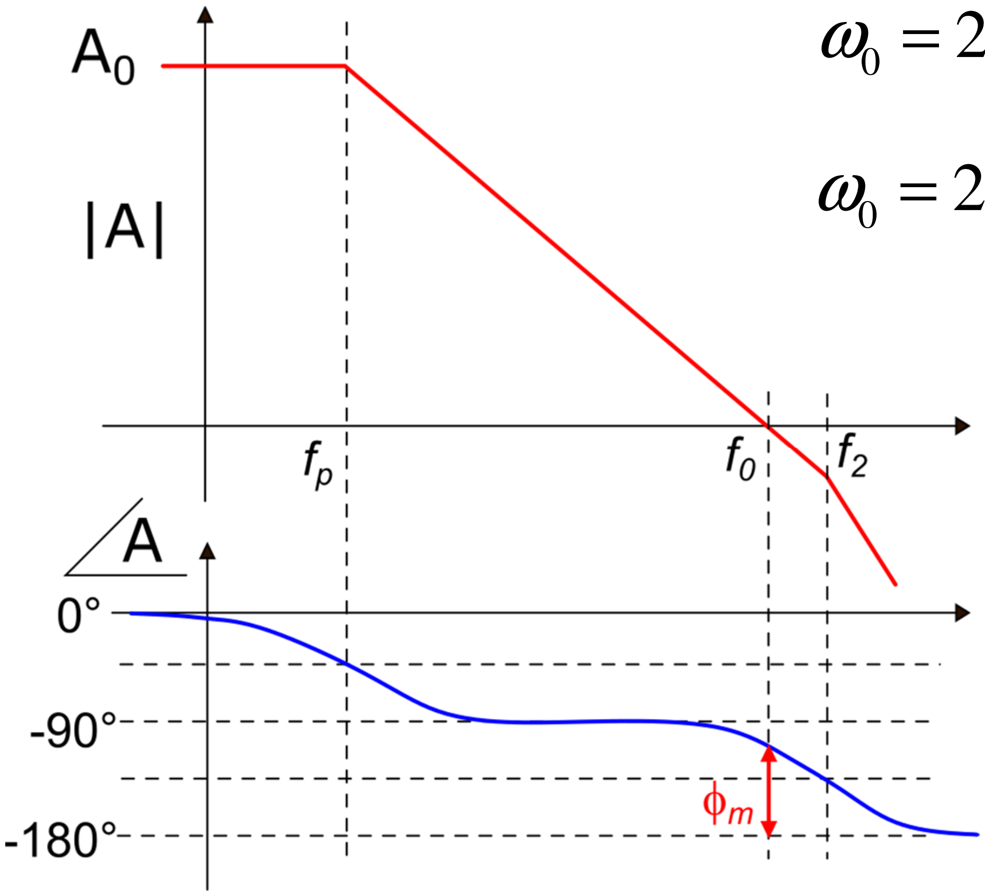
In this design procedure, we decide to cancel the zero:

$$\boxed{R_C = \frac{1}{G_{m2}}}$$

We consider that the *GBW* and phase margin can be estimated by using a two-pole approximation of the frequency response, with a dominant pole (ω_p):

$$\omega_p << \omega_2 \qquad \omega_2 << \omega_3,\ \omega_{tail},\ \omega_{mirror}$$

GBW and unity-gain angular frequency (ω_0)



$$\omega_0 = 2\pi f_0 \qquad f_0 \cong GBW = A_0 f_p$$

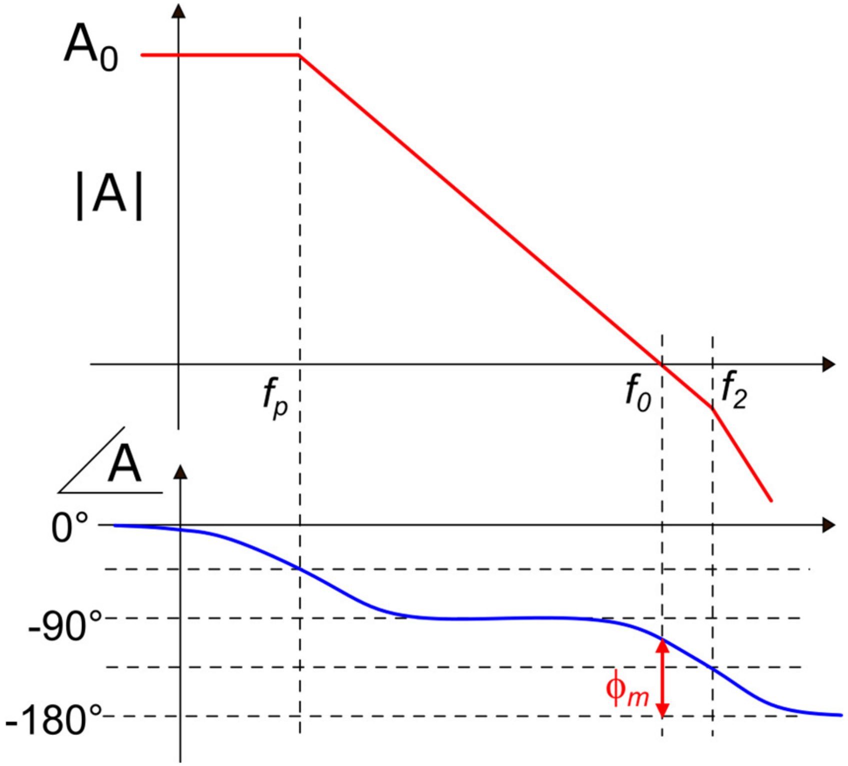
$$\omega_0 = 2\pi A_0 f_p \longrightarrow \omega_0 = A_0 \omega_p$$

$$\omega_p \cong \frac{1}{R_1 G_{m2} R_2 C_C}$$

$$A_0 \cong G_{m1} R_1 G_{m2} R_2$$

$$\boxed{\omega_0 \cong \frac{G_{m1} R_1 G_{m2} R_2}{R_1 G_{m2} R_2 C_C} = \frac{G_{m1}}{C_C}}$$

GBW and stability specifications



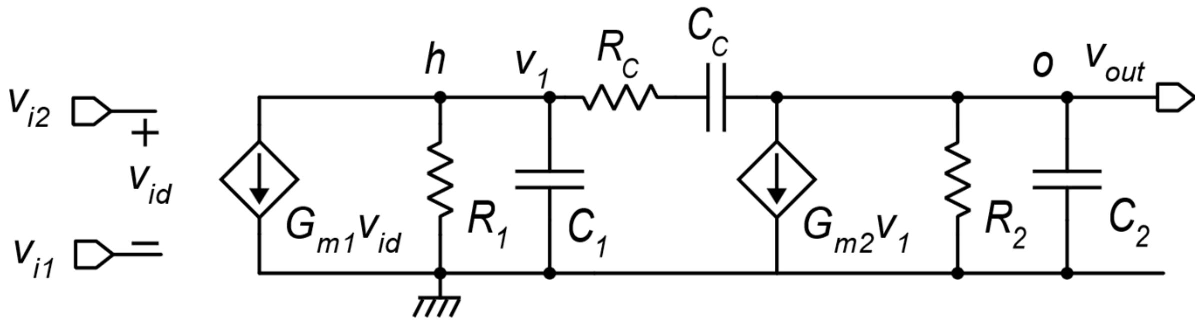
$$\omega_0 \cong \frac{G_{m1}}{C_C} \qquad GBW = \frac{\omega_0}{2\pi}$$

$$\varphi_m \cong 70° \Rightarrow \sigma = \frac{f_2}{f_0} = 3$$

Then, we impose: $\omega_2 = \sigma\omega_0$

$$\omega_2 \cong \frac{G_{m2}}{(C_1 + C_2)}\left(1 + \frac{C_S}{C_C}\right)^{-1}$$

An approximate approach: Hypothesis 1



Hypothesis 1: C_1 is much smaller than C_2 and C_C:

$$C_2 >> C_1$$

$$C_C >> C_1$$

$$C_S < C_1 << C_C$$

Motivation:
C_2 includes the load capacitance, C_L
C_C can be made arbitrarily large to satisfy the hypothesis

$$\omega_2 = \frac{G_{m2}}{(C_1 + C_2)}\left(1 + \frac{C_S}{C_C}\right)^{-1} \cong \frac{G_{m2}}{(C_1 + C_2)}$$

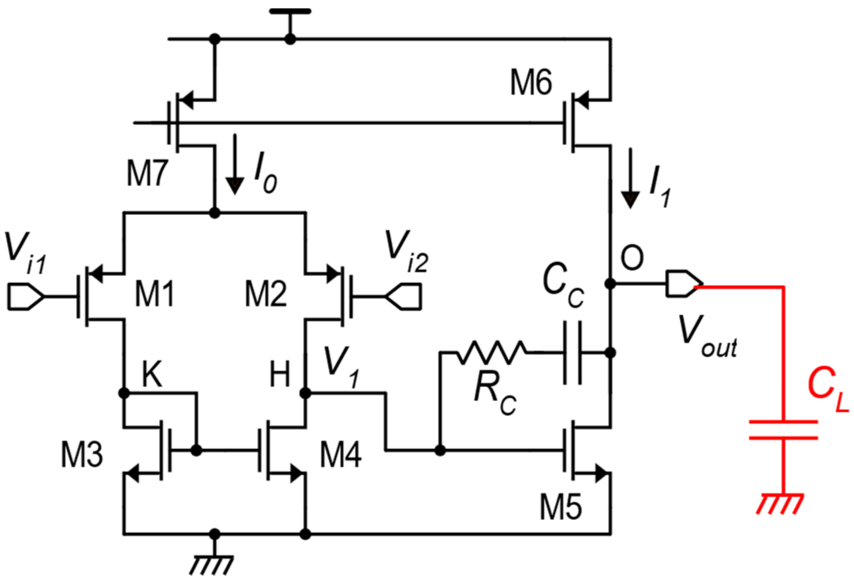
$$\boxed{\omega_2 \cong \frac{G_{m2}}{C_2}}$$

An approximate approach: Hypothesis 2

Hypothesis 2: The parasitic component C_2' is much smaller than C_L:

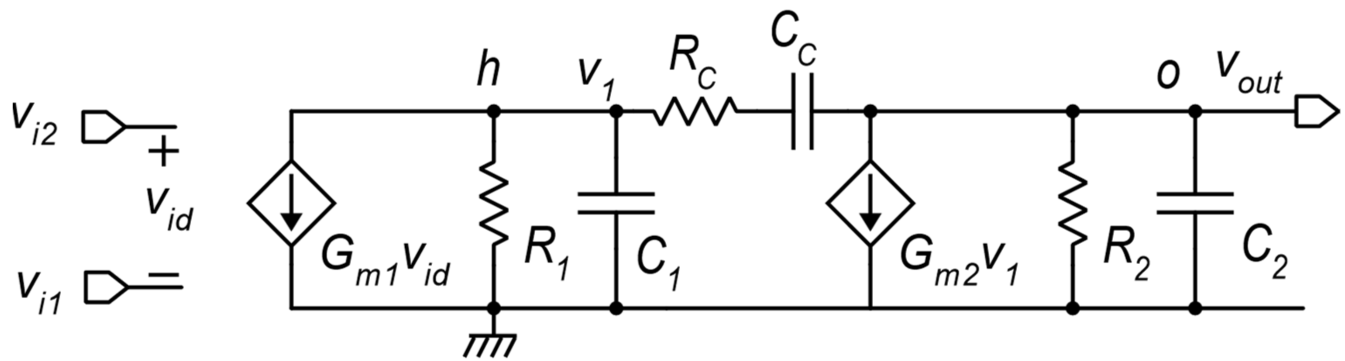
$$C_2 = C'_2 + C_L \cong C_L \qquad \omega_2 \cong \frac{G_{m2}}{C_2} \cong \frac{G_{m2}}{C_L}$$

Now the expression of ω_2 is strongly simplified



Hypotheses 1 and 2 correspond to consider that all parasitic capacitances of the amplifier are negligible with respect to C_L and C_C, which are external to the amplifier (C_L) or are purposely placed devices (C_C).

The *GBW* specification shapes the second stage (G_{m2})



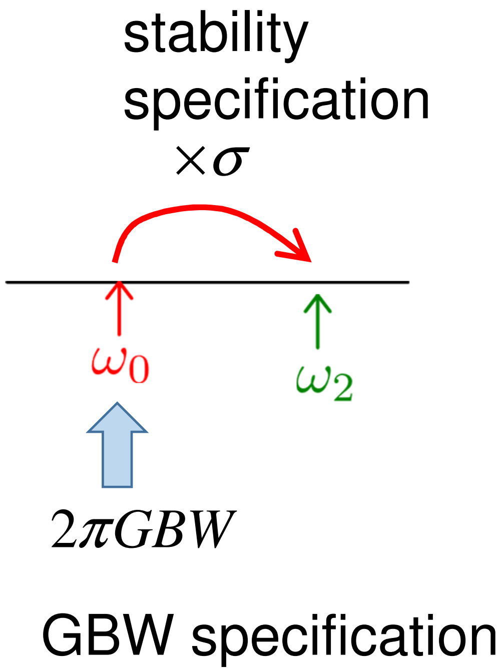
$$\omega_2 \cong \frac{G_{m2}}{C_L}$$

For the stability requirement: $\omega_2 = \sigma\omega_0$

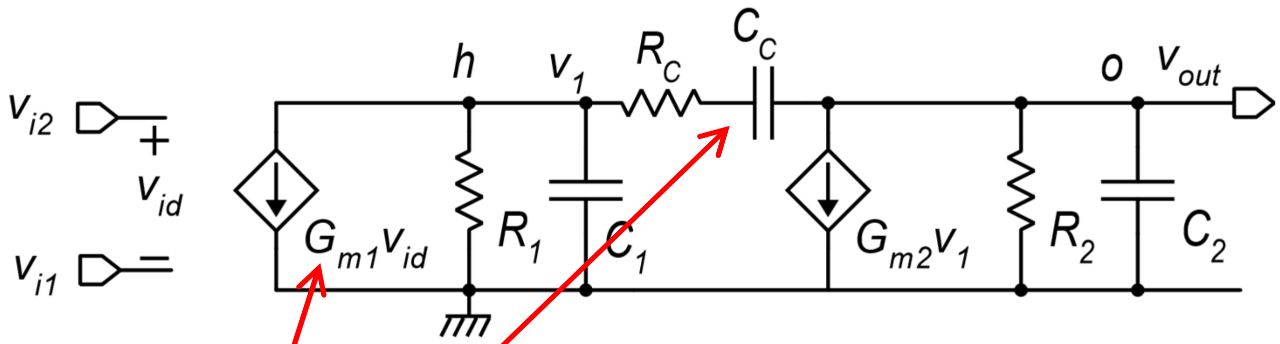
$$\omega_2 = \sigma \cdot 2\pi f_0 \cong \sigma \cdot 2\pi GBW$$

$$\frac{G_{m2}}{C_L} \cong \sigma \cdot 2\pi GBW$$

$$\boxed{G_{m2} \cong 2\pi\sigma \cdot GBW \cdot C_L}$$



Back to the first stage



$$G_{m2} \cong 2\pi\sigma \cdot GBW \cdot C_L$$

$$R_C = \frac{1}{G_{m2}}$$

$$\omega_0 \cong \frac{G_{m1}}{C_C}$$

We have two degrees of freedom, G_{m1} and C_C: a smaller G_{m1} would allow for a smaller C_C value, saving area. However, C_C cannot get too small, otherwise hypothesis 1 risks to fail.

To guide the choice, it is convenient to relate C_C to C_L and to the G_{m1}/G_{m2} ratio, through the stability condition

$$\omega_2 = \sigma\omega_0$$

stability condition

$$\frac{G_{m2}}{C_L} = \sigma\frac{G_{m1}}{C_C}$$

$$\boxed{\frac{G_{m1}}{G_{m2}} = \frac{1}{\sigma}\frac{C_C}{C_L}}$$

C_C and C_L, the "rule of thumb" and its limits

$$\frac{G_{m1}}{G_{m2}} = \frac{1}{\sigma}\frac{C_C}{C_L}$$

$$\left.\begin{array}{ll} \text{(a)} & C_2 \cong C_L >> C_1 \\ \text{(b)} & C_C >> C_1 \end{array}\right\} \text{Hypothesis 1}$$

If we make C_C=C_L, validity of condition (a) makes also condition (b) automatically true. Making C_C even larger than C_L does not add validity to hypothesis 1 and requires more area.

Rule of thumb: $C_C = C_L$

$$G_{m1} = \frac{1}{\sigma} G_{m2}$$

With σ=3 ($\varphi_m \cong 70°$)

We have determined both G_{m1} and G_{m2}

$$G_{m1} = \frac{1}{3} G_{m2}$$

Limits of the rule of thumb

Rule of thumb: $C_C = C_L$

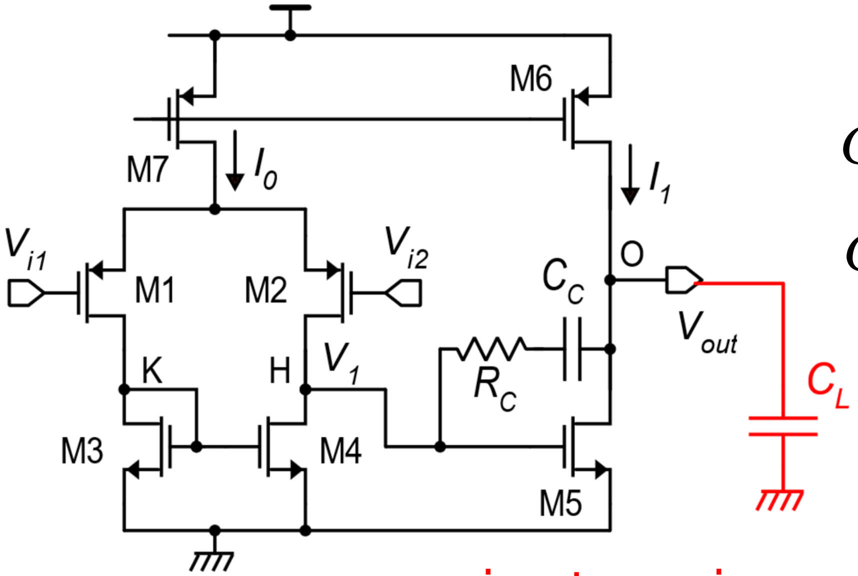
Often, it is convenient to apply a different choice

Case of large C_L: If the maximum load capacitance is particularly large (> tens pF), using the rule of thumb can result in too large a compensation capacitance, and then, in non-acceptable chip area occupation. In those cases, the C_C/C_L can be made smaller than one ($C_C<C_L$) in order to make C_C easily integrable.

For example: with C_L=100 pF,
I choose: C_C=10 pF

$$\frac{G_{m1}}{G_{m2}} = \frac{1}{\sigma}\frac{C_C}{C_L} = \frac{1}{10\sigma} \cong \frac{1}{30}$$

Application of the design procedure to our simple two-stage op-amp



$$G_{m2} = g_{m5} \cong 2\pi\sigma \cdot GBW \cdot C_L$$

$$G_{m1} = g_{m1} = G_{m2}\frac{1}{\sigma}\frac{C_C}{C_L} = g_{m5}\frac{1}{\sigma}\frac{C_C}{C_L}$$

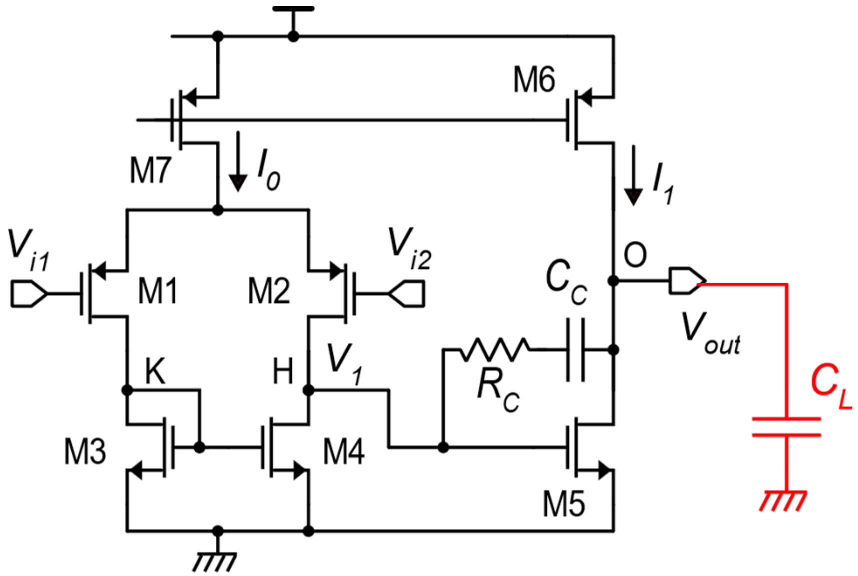
in strong inversion

$$g_{m1} = \mu_p C_{OX}\frac{W_1}{L_1}\left|V_{GS}-V_t\right|_1 \quad \Rightarrow \quad \boxed{\frac{W_1}{L_1} = \frac{g_{m1}}{\mu_p C_{OX}\left|V_{GS}-V_t\right|_1}}$$

$$g_{m5} = \mu_n C_{OX}\frac{W_5}{L_5}\left(V_{GS}-V_t\right)_5 \quad \Rightarrow \quad \boxed{\frac{W_5}{L_5} = \frac{g_{m5}}{\mu_n C_{OX}\left(V_{GS}-V_t\right)_5}}$$

Once the M1 and M5 overdrive voltages have been chosen, the *GBW* specification determines the aspect ratios (*W*/*L*) of both MOSFETs

GBW and supply current



$$I_{supply} = 2I_{D1} + I_{D5}$$

$$g_m = \frac{I_D}{V_{TE}} \Rightarrow I_D = g_m V_{TE}$$

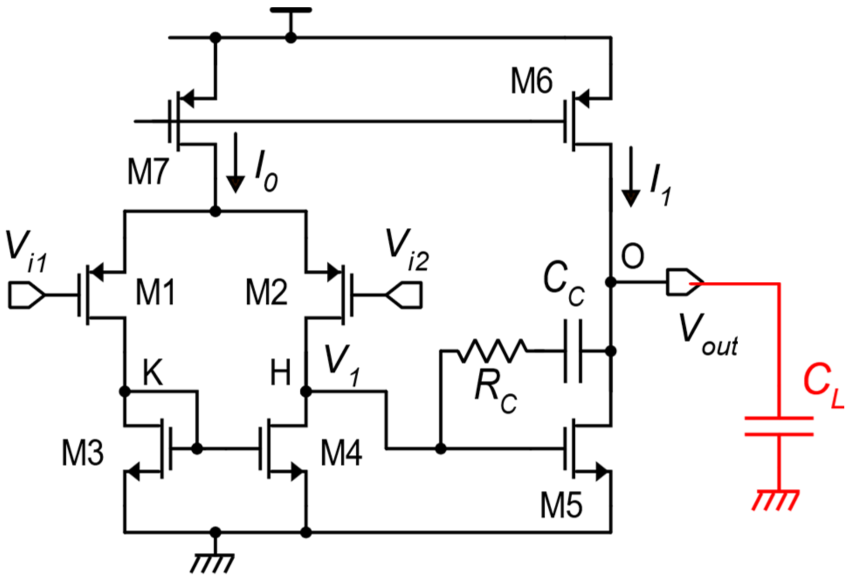
$$I_{supply} = 2g_{m1}V_{TE1} + g_{m5}V_{TE5}$$

$$I_{supply} = g_{m5}\left(V_{TE5} + 2\frac{g_{m1}}{g_{m5}}V_{TE1}\right)$$

$$g_{m5} \cong 2\pi\sigma \cdot GBW \cdot C_L$$

$$I_{supply} = 2\pi\sigma \cdot GBW \cdot C_L \cdot \left(V_{TE5} + 2\frac{g_{m1}}{g_{m5}}V_{TE1}\right)$$

GBW, C_L and supply current

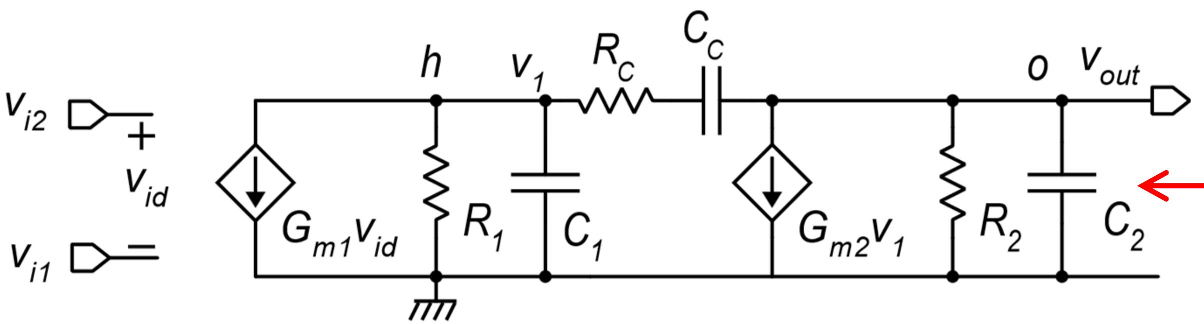


$$I_{supply} = 2\pi\sigma \cdot GBW \cdot C_L \cdot \left(V_{TE5} + 2\frac{g_{m1}}{g_{m5}} V_{TE1} \right)$$

$$\frac{g_{m1}}{g_{m5}} = \frac{G_{m1}}{G_{m2}} = \frac{1}{\sigma}\frac{C_C}{C_L}$$

- The higher the *GBW and load capacitance* C_L, the higher the supply current and then the power consumption
- For the same *GBW* and C_L specifications, lower supply currents can be obtained with the lowest V_{TE5} and V_{TE1}.

Robustness against C_L variations



$C_2' + C_L$

We have designed the op-amp for the maximum C_L. It must be stable also for smaller values

If we **reduce** C_L, then C_2 reduces and hypothesis 1 may be no more valid. Then we have to use the complete expression for ω_2:

$$\omega_2 = \frac{G_{m2}}{\boxed{(C_1 + C_2)}} \cdot \frac{1}{\boxed{1 + \frac{C_S}{C_C}}}$$

ω_2 increases!

Both denominators reduces

Effects of C_2 reduction:

$$C_S = \left(\frac{1}{C_1} + \frac{1}{C_2}\right)^{-1}$$ gets smaller

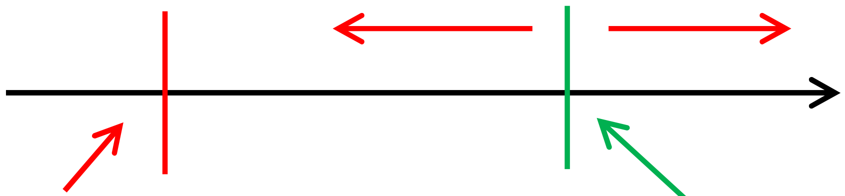
$$\frac{C_S}{C_C}$$ gets smaller

Robustness against C_L variations

$$\varphi_m \cong \arctan\left(\frac{\omega_2}{\omega_0}\right)$$

C_L increases: smaller phase margin

C_L decreases: greater phase margin



$$\omega_0 \cong \frac{G_{m1}}{C_C}$$ Is nearly unaffected by C_L

$$\omega_2 = \frac{G_{m2}}{(C_1 + C_2)} \cdot \frac{1}{1 + \frac{C_S}{C_C}}$$

In a two-stage amplifier:

- <u>Reducing</u> (or even removing) the load capacitance <u>improves</u> stability
- Increasing the load capacitance reduces stability and eventually causes instability

Limits of the simplified design procedure

Given a *GBW* specification, the procedure can be summarized in the following way

1. Find the required G_{m2} value from the equation: $$\omega_2 \cong \sigma \cdot 2\pi GBW = \frac{G_{m2}}{C_L}$$

2. Choose a proper C_C/C_L ratio, depending on the value of C_L

3. Find the required G_{m1}: $$G_{m1} = \frac{1}{\sigma}\frac{C_C}{C_L}G_{m2}$$

It seems that using the required current to set G_{m2} and G_{m1} to the correct value, we can reach an arbitrarily high GBW, independently of the process being used. This is clearly not reasonable.

Limits of the simplified design procedure

The problem stands in the hypotheses the procedure is based on.

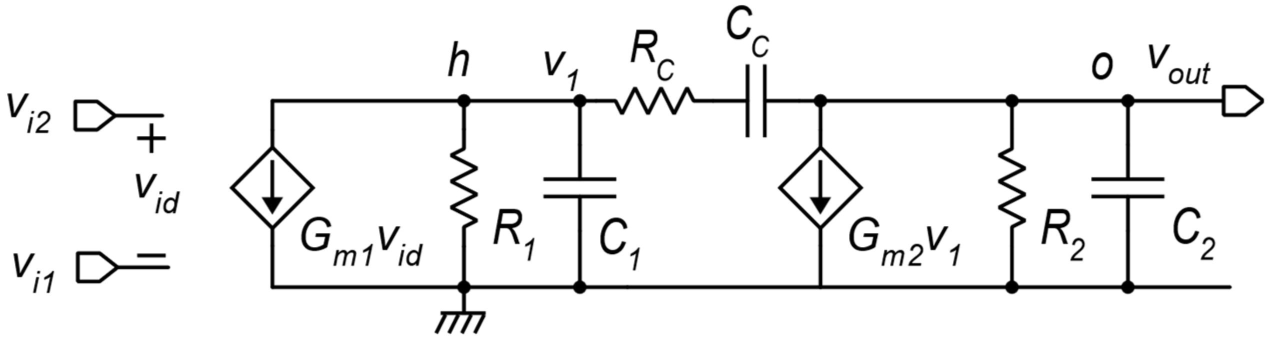
The hypotheses derive from the fact that C_L is generally prevalent over the parasitic capacitances:

Hyp. 1

$C_2 >> C_1 \Leftarrow C_L >> C_1, C_2' \Rightarrow C_2 = C'_2 + C_L \cong C_L$ Hyp. 2

$C_C >> C_1 \Leftarrow$ can be satisfied choosing a large enough C_C.

Trying to get larger and larger G_{m2} and G_{m1} increases also the size of the MOSFETs in the first and second stage, causing violation of the hypotheses



Limits of the simplified design procedure

$$\omega_2 = \sigma \cdot 2\pi f_0 \cong \sigma \cdot 2\pi GBW$$

$$GBW = \frac{1}{2\pi\sigma}\omega_2$$

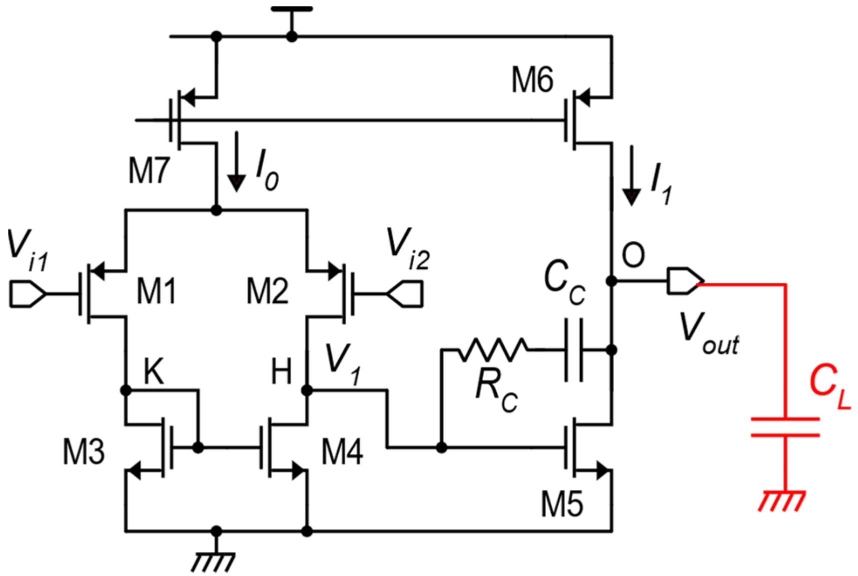
$$\omega_2 = \frac{G_{m2}}{(C_1 + C_2)} \cdot \frac{1}{1 + \dfrac{C_S}{C_C}}$$

I can still set C_C as large as to make C_S/C_C <<1

$$\omega_2 \cong \frac{G_{m2}}{(C_1 + C_2)}$$

$$GBW = \frac{1}{2\pi\sigma}\frac{G_{m2}}{(C_1 + C_2)} = \frac{1}{2\pi\sigma}\frac{G_{m2}}{(C_1 + C_2' + C_L)}$$

Limits of the simplified design procedure



$$GBW = \frac{1}{2\pi\sigma}\frac{G_{m2}}{\left(C_1 + C_2' + C_L\right)}$$

$$C_1 = C_{GS5} + C_{DB2} + C_{DB4} \cong C_{GS5}$$

$$C_2' = C_{DB5} + C_{DB6} << C_{GS5}$$

$$GBW \cong \frac{1}{2\pi\sigma}\frac{g_{m5}}{\left(C_{GS5} + C_L\right)}$$

$$GBW \cong \frac{1}{2\pi\sigma}\frac{g_{m5}}{C_{GS5}}\frac{1}{\left(1 + \frac{C_L}{C_{GS5}}\right)}$$

$$\frac{1}{2\pi}\frac{g_{m5}}{C_{GS5}} \cong f_{T5}$$

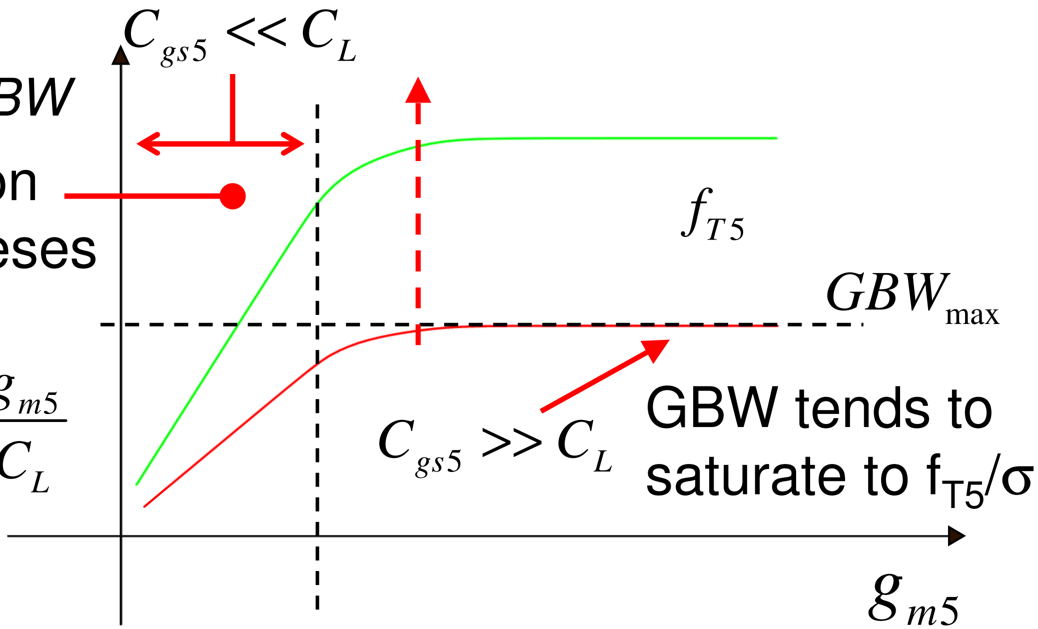
$$GBW \cong \frac{f_{T5}}{\sigma}\frac{1}{\left(1 + \frac{C_L}{C_{GS5}}\right)}$$

Maximum achievable *GBW*

$$C_{gs5} = \frac{g_{m5}}{2\pi f_{T5}}$$

Increasing g_{m5} for a given f_{T5}, increases C_{gs5} proportionally

$$GBW \cong \frac{f_{T5}}{\sigma}\frac{1}{\left(1+\dfrac{C_L}{C_{GS5}}\right)} \begin{cases} \dfrac{1}{2\pi\sigma}\dfrac{g_{m5}}{C_L} & C_{gs5} << C_L \\ \dfrac{f_{T5}}{\sigma} & C_{gs5} >> C_L \end{cases}$$



In this region the hypotheses are valid

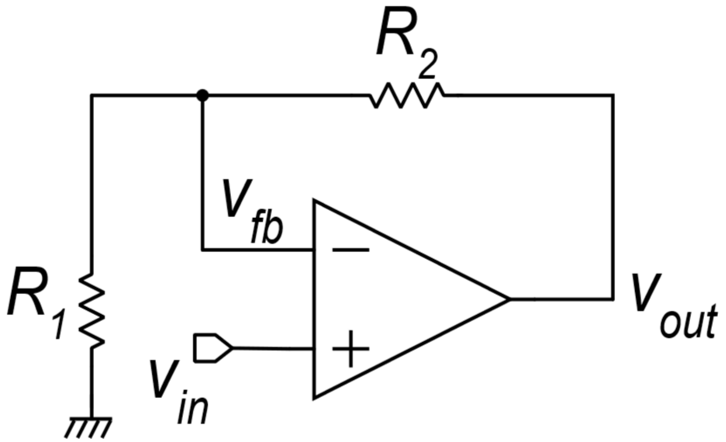
$$GBW = \frac{1}{2\pi\sigma}\frac{g_{m5}}{C_L}$$

In strong inversion

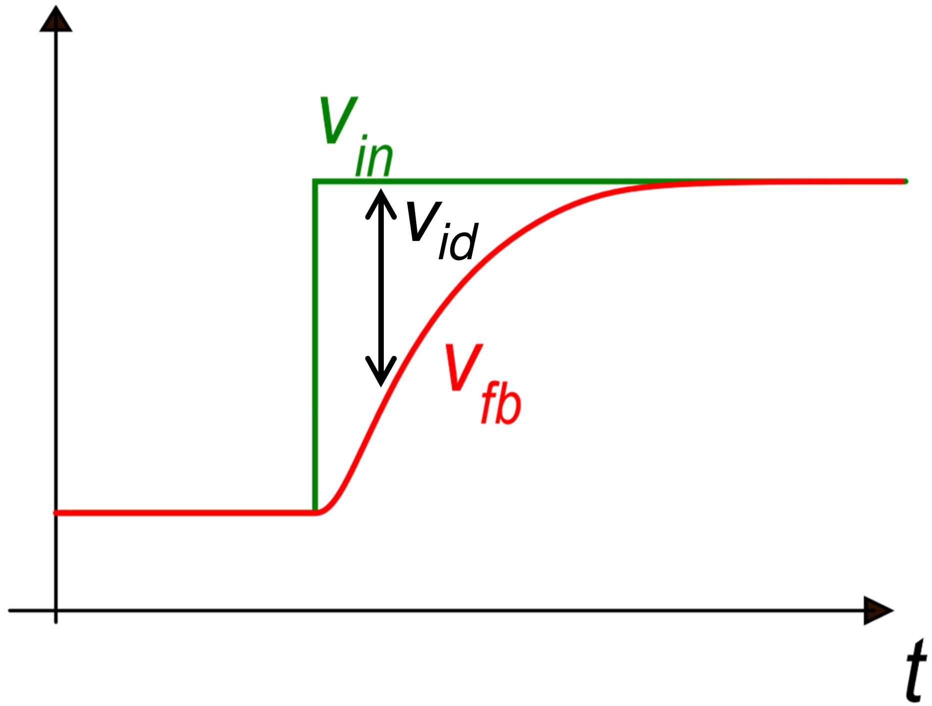
L_5 $(V_{GS}-V_t)_5$

$$f_{T5} \cong \frac{3}{4\pi}\mu_n\frac{1}{L_5^2}\left(V_{GS}-V_t\right)_5$$

The slew rate problem

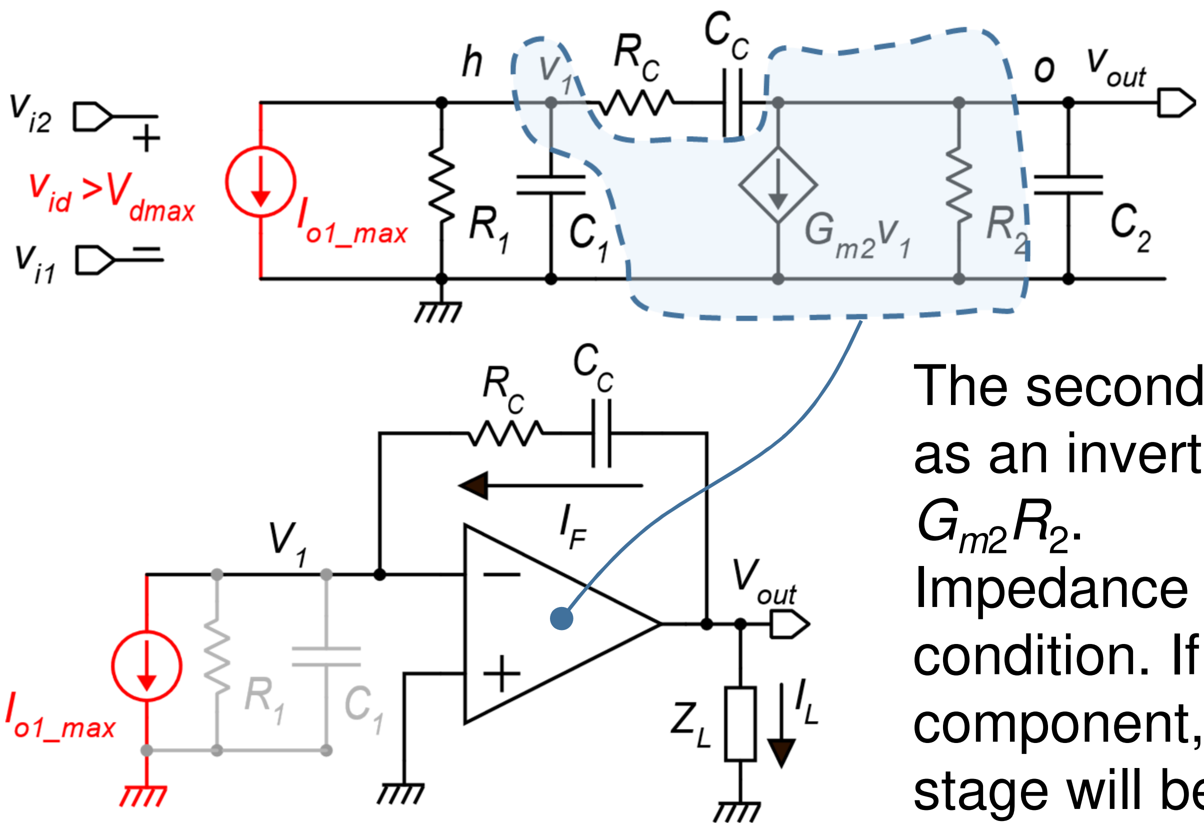


If the input step is large enough, the input stage saturates



Just after a step variation of the input voltage, the feedback voltage, derived by the output voltage, cannot change instantaneously and the input differential voltage of the op-amp can be driven out of the linearity region of the first stage

Slew rate in Miller-compensated two-stage op-amps

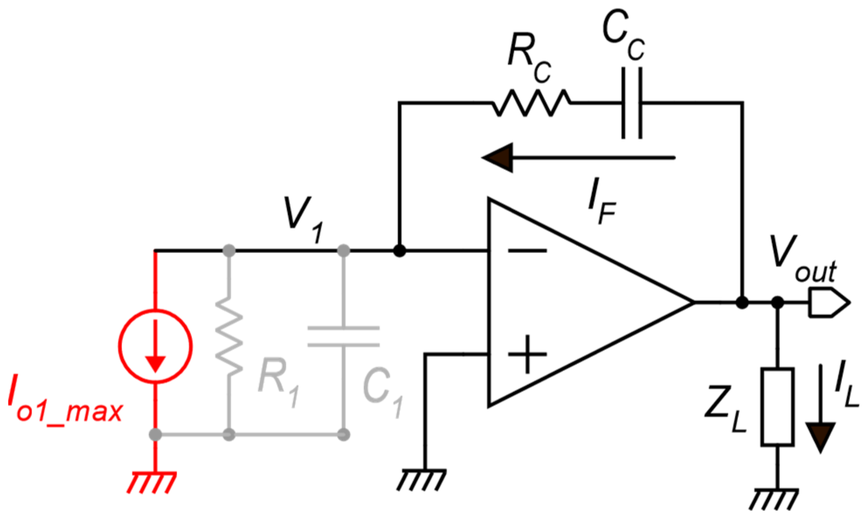


The second stage can be represented as an inverting amplifier with gain $G_{m2}R_2$.

Impedance Z_L represents the load condition. If Z_L has a resistive component, the gain of the second stage will be smaller than $G_{m2}R_2$.

Z_L includes the load capacitance

Slew rate in Miller-compensated two-stage op-amps



$$I_F \cong I_{o1-\max}$$

$$v_{out} = v_1 + I_{o1-\max} R_C + \frac{1}{C_C} \int I_{o1-\max} dt$$

$$\text{since } V_1 \cong constant \qquad \frac{dv_{out}}{dt} \cong \frac{I_{o1-\max}}{C_C}$$

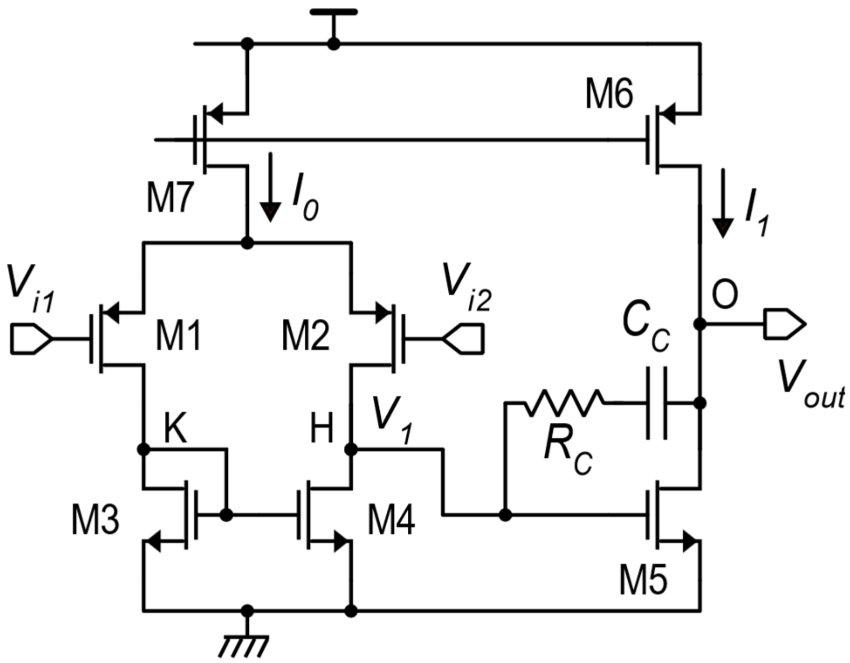
($I_{o1\text{-}max}$ can be either negative or positive)

$$s_R = \max \left| \frac{dv_{out}}{dt} \right| = \frac{\left| I_{01-\max} \right|}{C_C}$$

If the gain of the second stage is high enough, we can consider virtual gnd at input v_1.

Note that current I_F flows also through the output terminal of the amplifier. Then, the analysis shown above is applicable if the second stage (output stage) is capable of producing the total current $I_F + I_L$

Slew rate of the simple class-A, two stage op-amp.



$$s_R = \frac{\left|I_{01-\max}\right|}{C_C}$$

From simple inspection of the first stage:

$$\left|I_{01-\max}\right| = I_0$$

$$s_R = \frac{I_0}{C_C} = \frac{2I_{D1}}{C_C} \qquad I_{D1} = V_{TE1} g_{m1}$$

$$\boxed{s_R = 2V_{TE1}\frac{g_{m1}}{C_C} = 2V_{TE1}\omega_0}$$

$$\underline{s_R = GBW \cdot 4\pi V_{TE1}}$$

For a given *GBW*, the higher V_{TE1} , the higher the slew rate