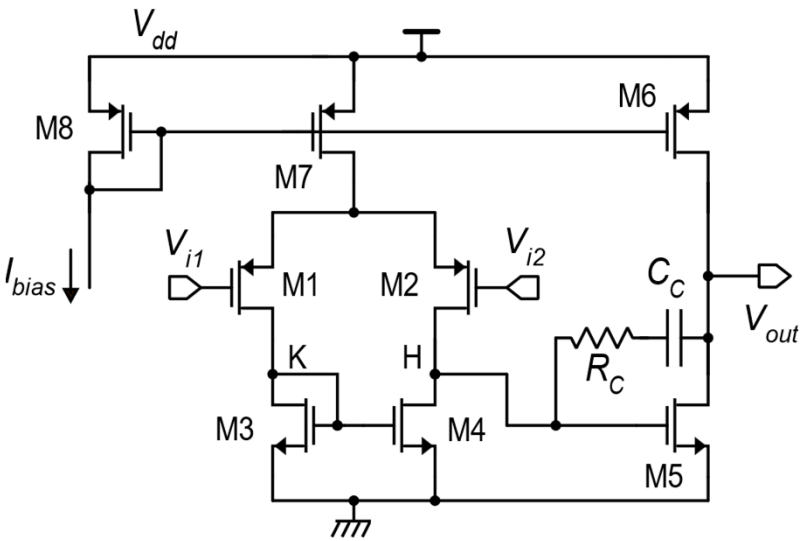
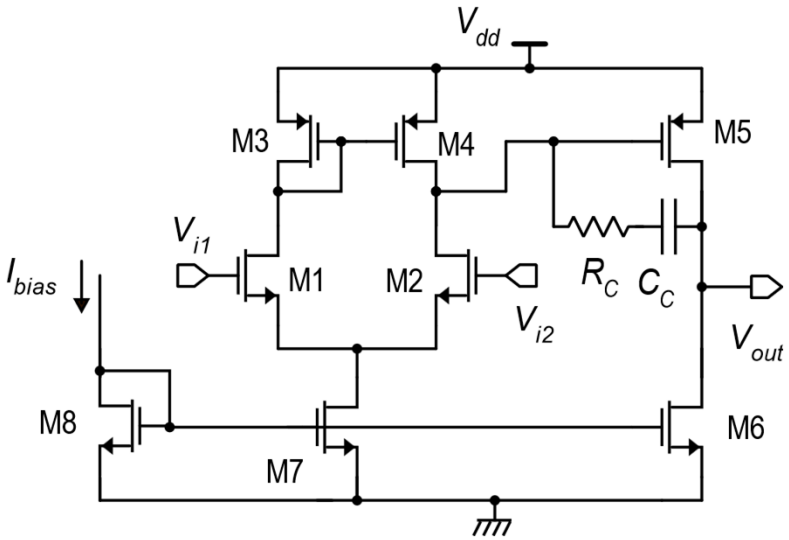
Popular op-amp topologies

Two stage op-amp with simple differential amplifier in the input stage and class-A common-source output stage

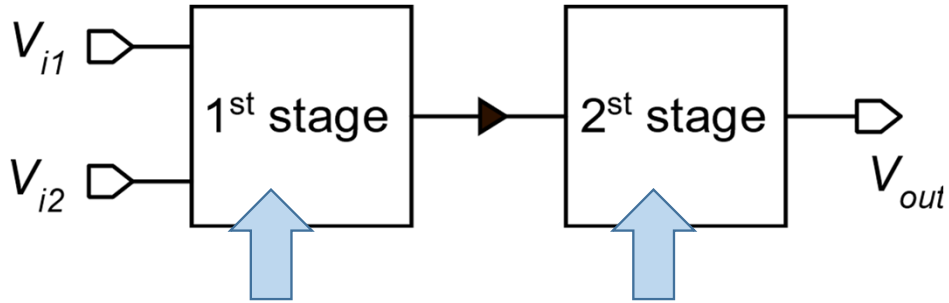


p-input version
Input range may include *gnd*
May **sink** large currents



n-input version
Input range may include V_{dd}
May **source** large currents

Improved topologies
(better performances, but greater complexity)



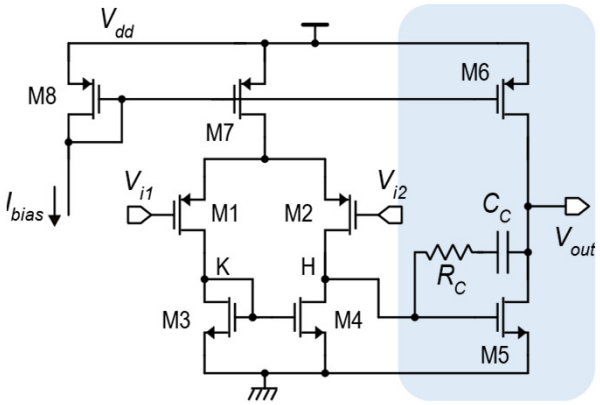
Cascode stages

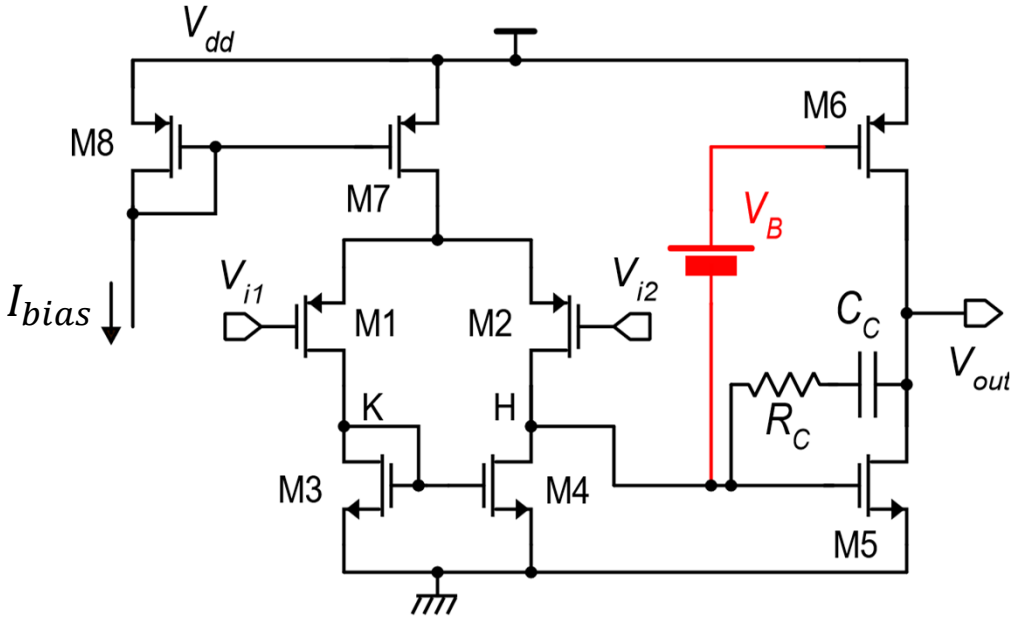
Class AB stages

Larger gain, simpler Rail-to-Rail input stages

Large output current with small quiescent power consumption

Class-AB output stages





$$I_{D5} = \frac{1}{2}\frac{\beta_5}{\beta_3}\frac{\beta_7}{\beta_8} I_{bias}$$

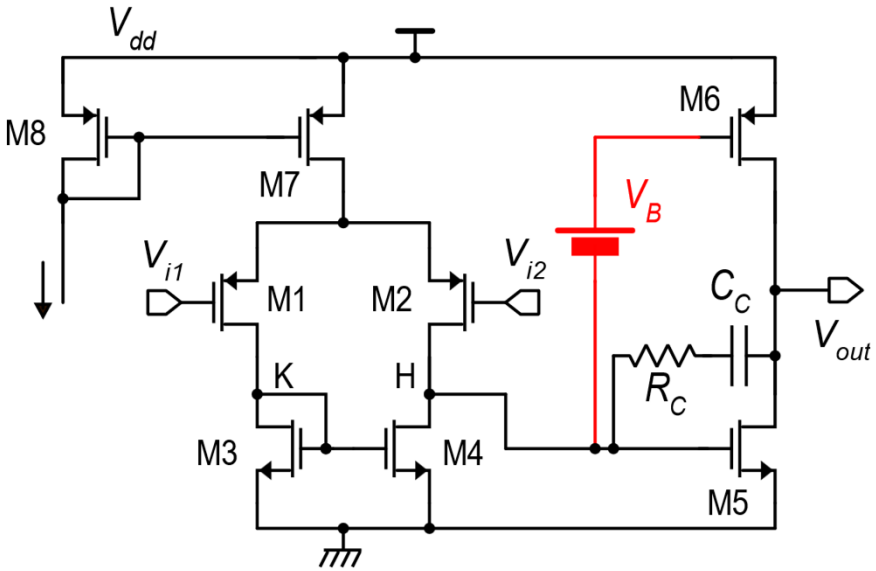
$$I_{D6} = \frac{\beta_6}{2}\left(V_{GS6} - V_{tp}\right)^2$$

I_{D5} does not depend on V_{dd}, while I_{D6} does.
The output short circuit current depends on V_{dd}

$$V_{GS6} = V_{DD} - V_{batt} - V_{GS5}$$

Poor PSSR

Op-amps with class- AB output stages



If we want to save this solution, we need to adapt both V_{GS5} and V_{GS6} when V_{dd} changes, and guarantee that:

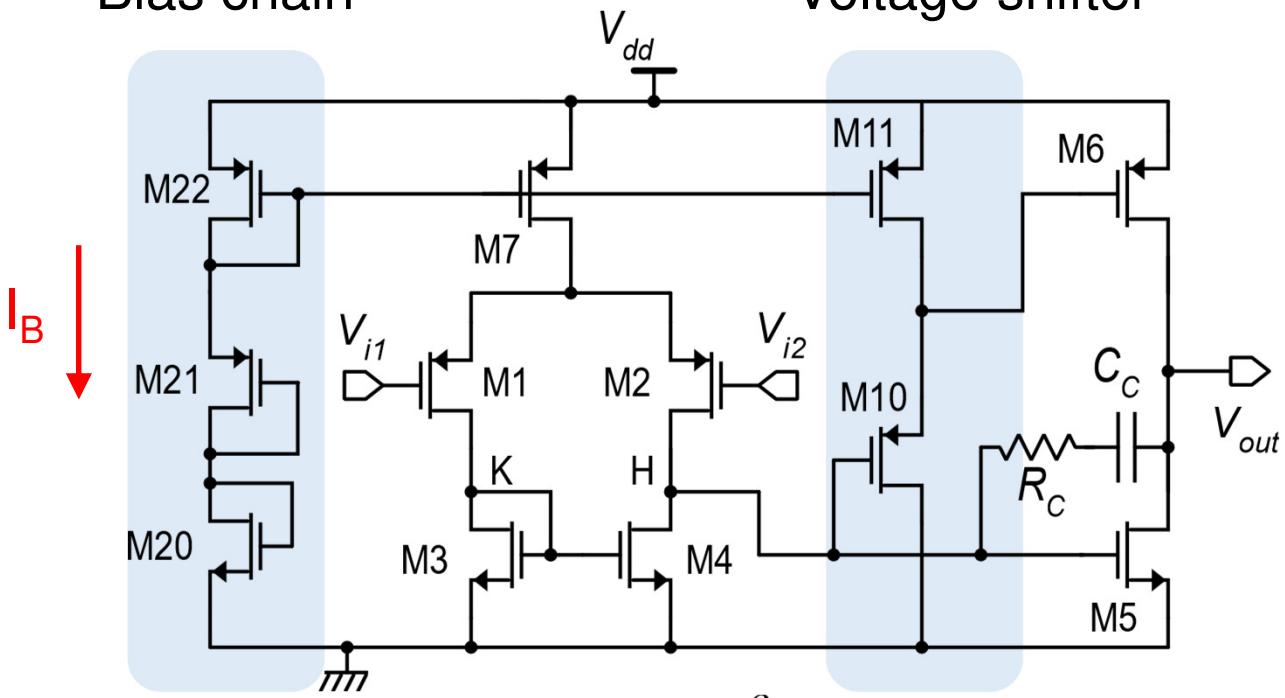
$$I_{D5} = I_{D6}$$

is always valid

Op-amps with class- AB output stages

Bias chain

Voltage shifter



$$I_{D5} = \frac{1}{2}\frac{\beta_5}{\beta_3}\frac{\beta_7}{\beta_{22}} I_B$$

$$I_{D6} = \frac{\beta_6}{2}\left(V_{GS6} - V_{tp}\right)^2$$

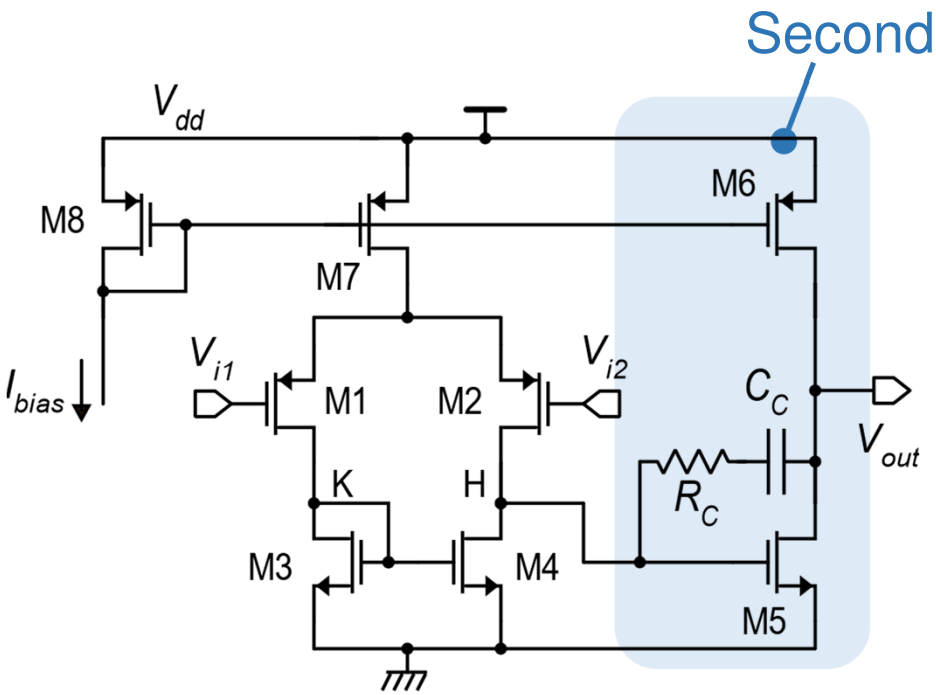
$$|V_{GS6}| = V_{DD} - |V_{GS10}| - V_{GS3}$$

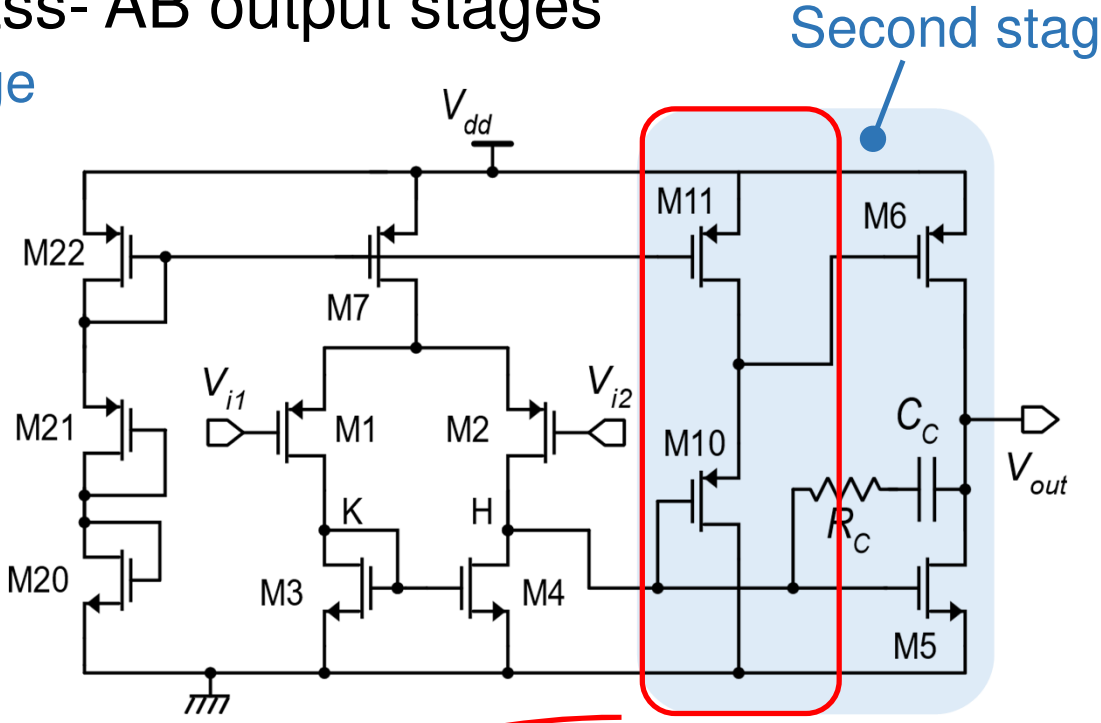
$$|V_{GS22}| = V_{DD} - |V_{GS21}| - V_{GS20}$$

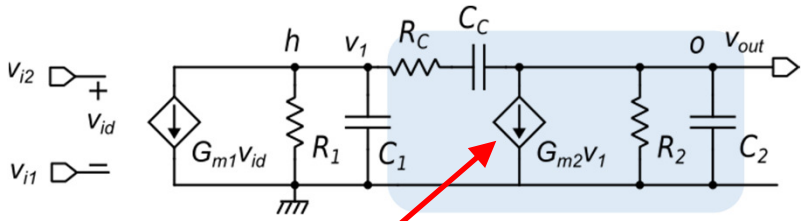
$$\frac{\beta_{21}}{\beta_{10}} = \frac{I_B}{I_{D10}} \qquad \frac{\beta_{20}}{\beta_3} = \frac{I_B}{I_{D3}}$$

$$I_{D6} = \frac{\beta_6}{\beta_{22}} I_B \quad \Leftarrow \quad |V_{GS6}| = |V_{GS22}|$$

Op-amps with class- AB output stages



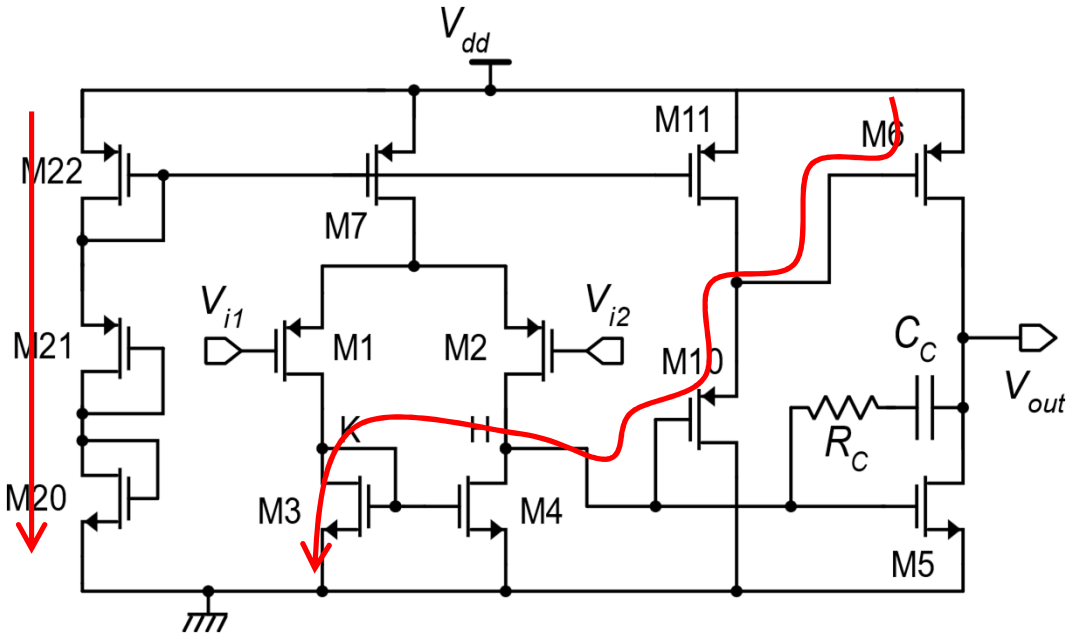




$G_{m2}=g_{m5}+g_{m6}$

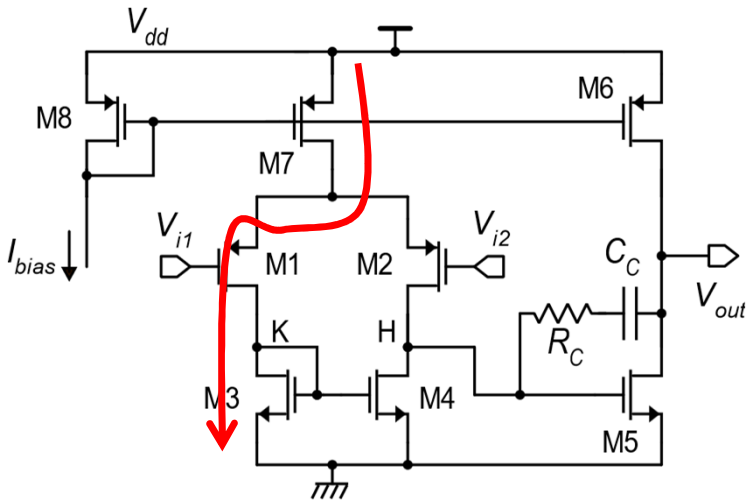
Voltage shifter:
additional singularities
$Y_{m2}(s)$ ⇨ $G_{m2}(s)$

Limitations: minimum V_{dd}

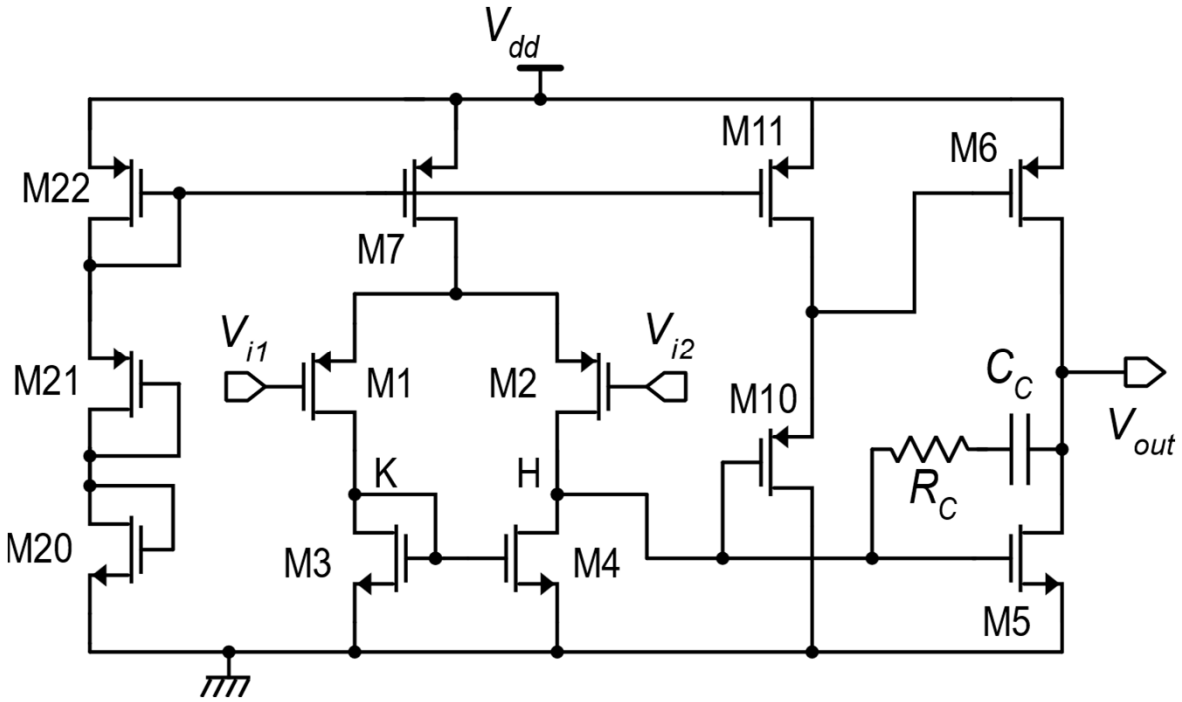


Minimum Vdd: $3V_{GS} \cong 2.1$ V

For the class-A amplifier, the minimum Vdd was only $V_{GS}+2V_{DSAT} \cong 0.9$ V



Reduced V_{GS} excursion for the output devices



$$V_{GS5-MAX} = V_{iC} + V_{GS} - V_{DSAT}$$

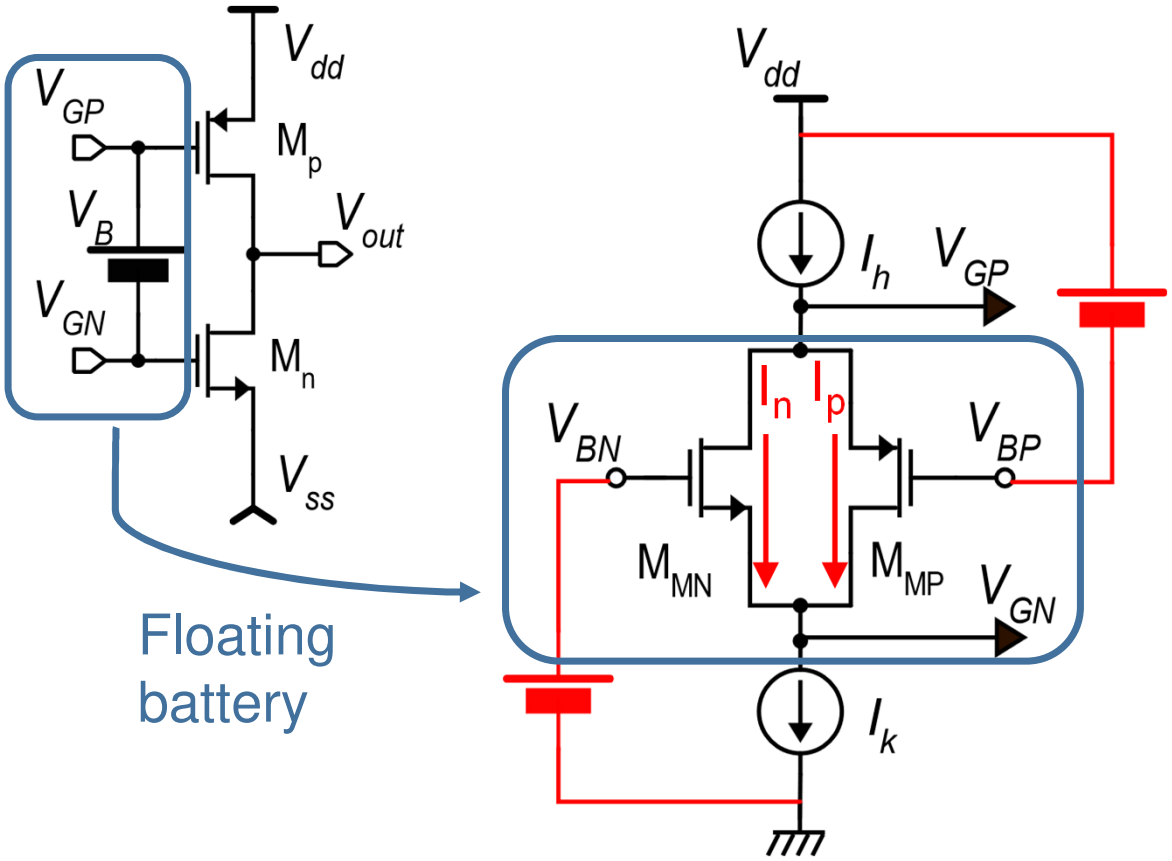
$$V_{GS6-MAX} = V_{dd} - V_{GS10}$$

$$I_{OP-MAX} = \frac{\beta_6}{2}\left(V_{GS6-MAX} - V_{tp}\right)^2$$

$$I_{ON-MAX} = \frac{\beta_5}{2}\left(V_{GS5-MAX} - V_{tn}\right)^2$$

- Both V_{GS5} and V_{GS6} cannot reach V_{dd}. If large output currents are required, this means that M5 and M6 should be designed with very large W
- I_{ON-MAX} strongly depends on the input common mode voltage

The Monticelli's class-AB stage



I_h and I_k includes also the variations due to the input signal and have a high output differential resistance (not shown for simplicity)

$$I_h \cong I_k = const$$

$$I_p + I_n \cong const \qquad i_n + i_p \cong 0$$

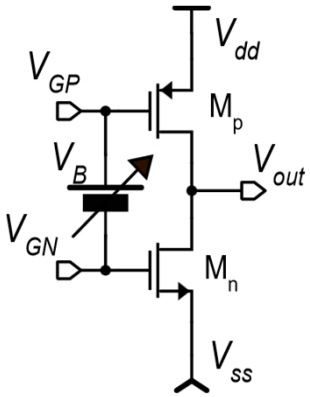
$$i_n = -g_{mMN} v_{gn} \qquad i_p = g_{mMP} v_{gp}$$

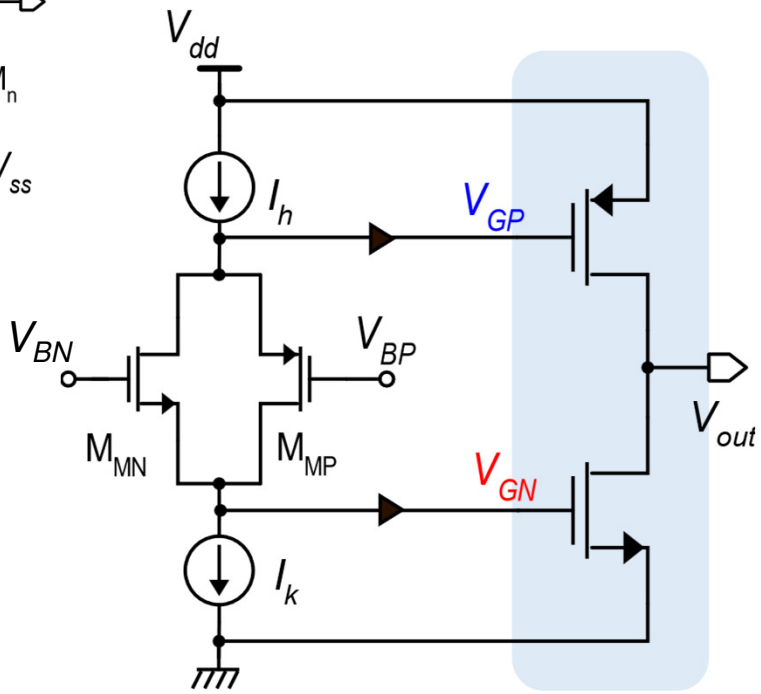
$$g_{mMN} v_{gn} = g_{mMP} v_{gp}$$

$$\frac{v_{gn}}{v_{gp}} = \frac{g_{mMP}}{g_{mMN}}$$

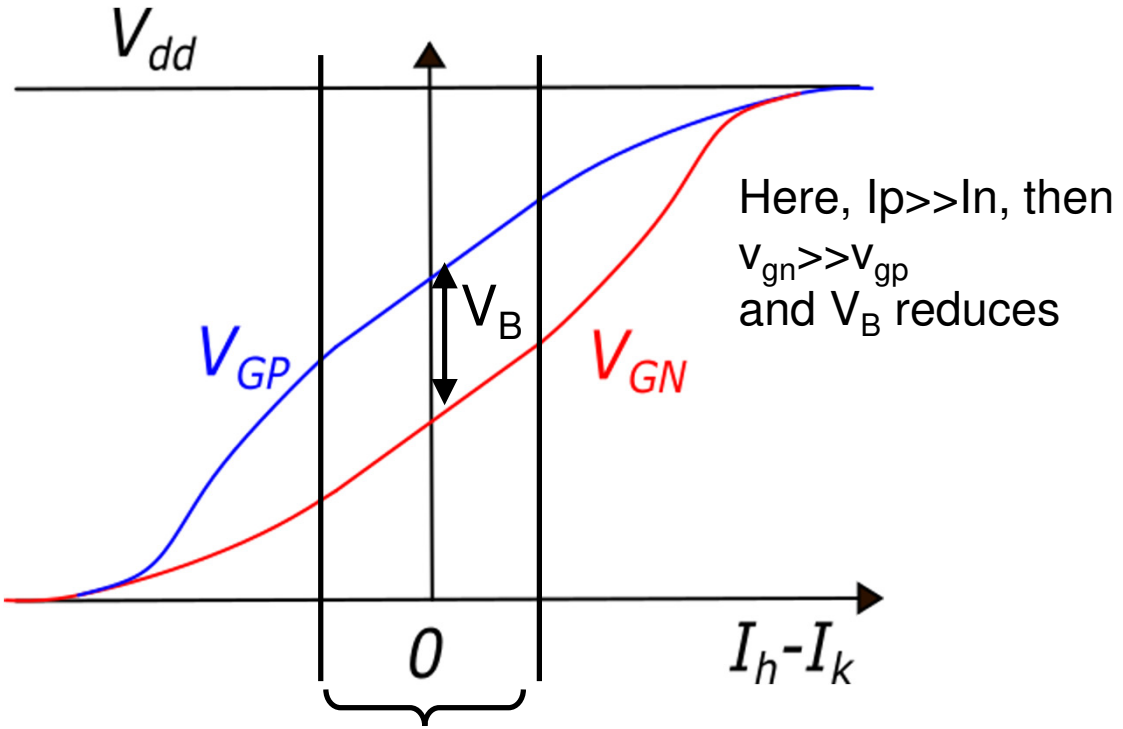
D. M. Monticelli, "A quad CMOS single-supply op amp with rail-to-rail output swing," IEEE J. Solid-State Circuits, vol. SC-21, pp. 1026-1034, Dec. 1986.

The Monticelli's class-AB stage





output devices



Here, Ip>>In, then v_{gn}>>v_{gp} and V_B reduces

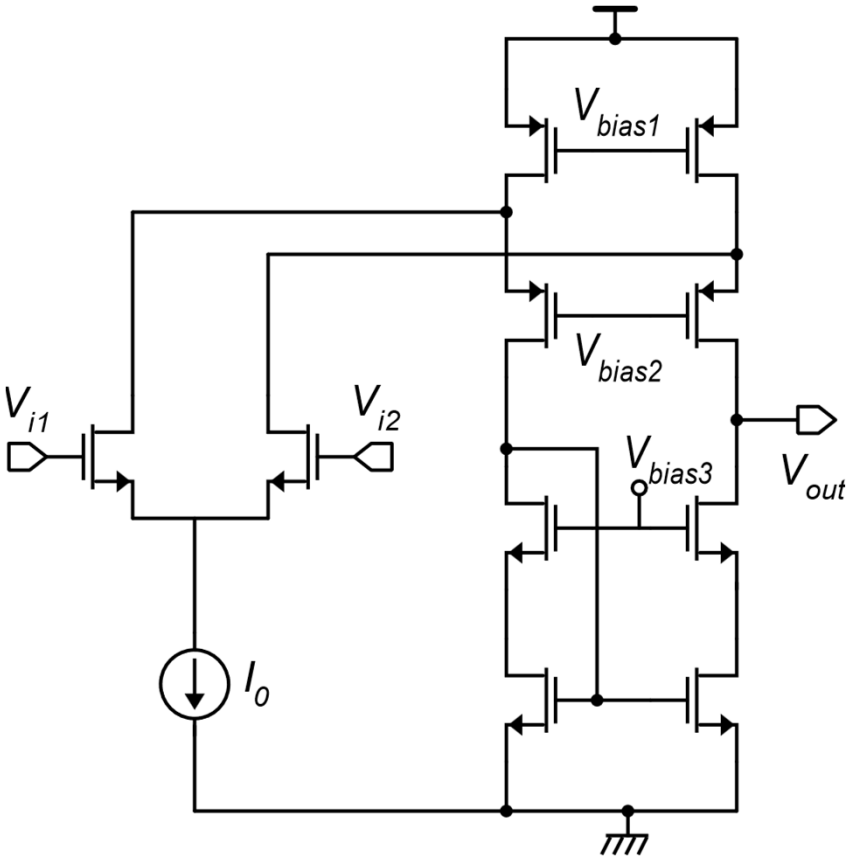
$$\frac{v_{gn}}{v_{gp}} = \frac{g_{mMP}}{g_{mMN}}$$

$$g_m = \sqrt{2 I_D \beta}$$

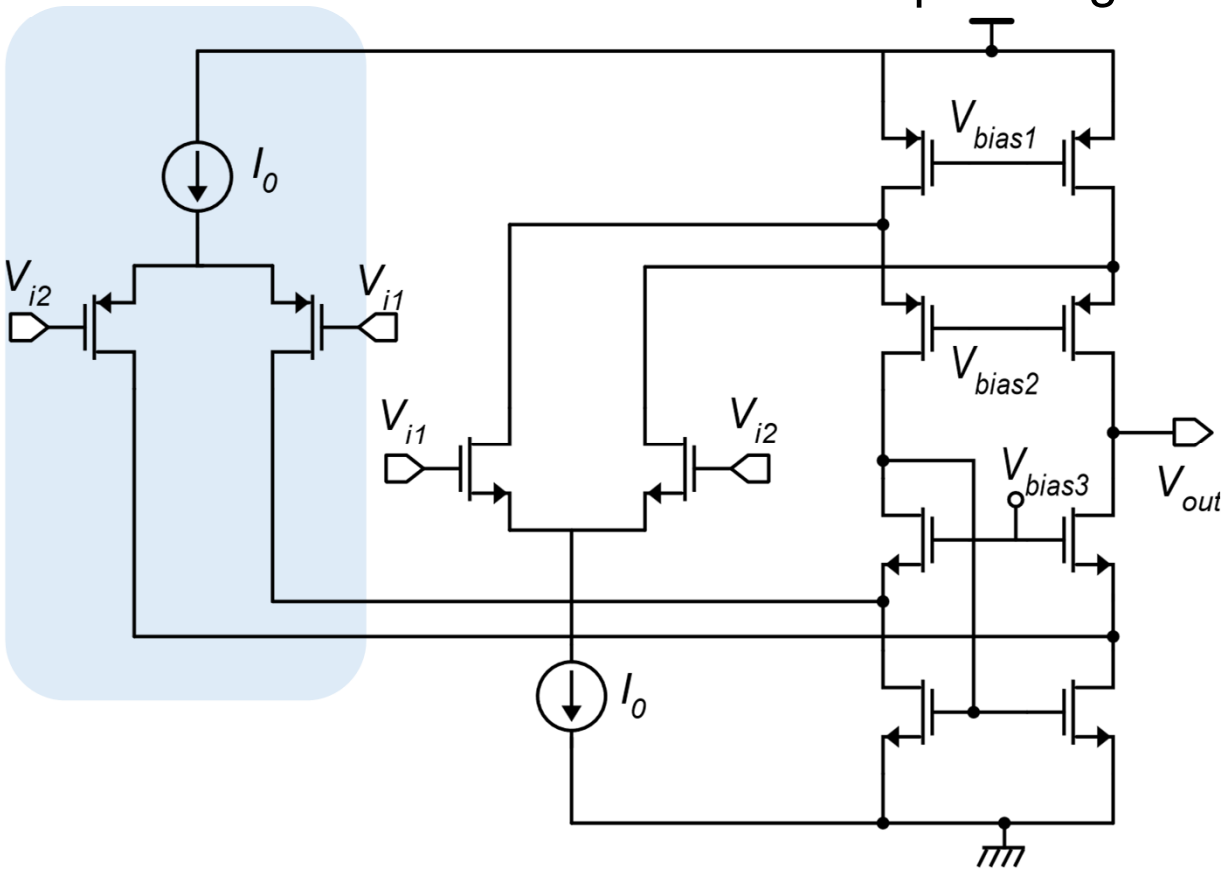
M_{NM} and M_{MP}, are designed to have same g_m in the operating point: v_{gn}=v_{gp} (variations)

First stage: folded cascode for improved gain and larger swing

n-input folded cascode



Folded cascode with rail-to-rail input range



High performance - two-stage CMOS op-amp

- High gain: $\approx (g_m r_d)^3$
- Class-AB output stage
- Rail-to-Rail input range

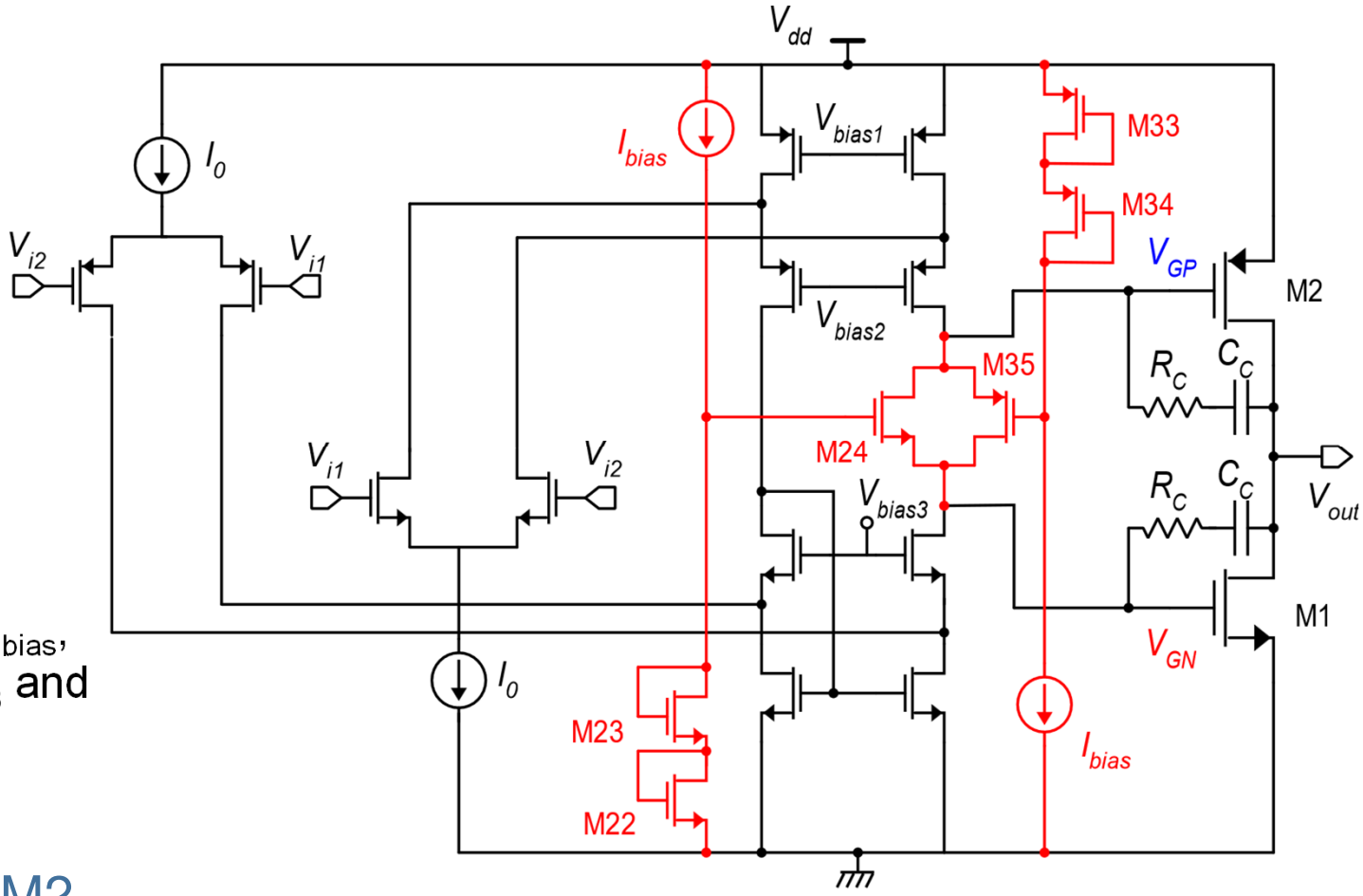
M24 and M35 form the Monticelli's cell

M22-M23 and M33-M34 produce the gate bias for M24 and M35, respectively

In quiescent conditions, we design I_{bias}, M23 and M34 to make: $V_{GS24}=V_{GS23}$ and $V_{GS35}=V_{GS34}$

$$V_{GS1} = V_{GS22}$$
$$V_{GS2} = V_{GS33}$$

This simplify setting of M1,M2 quiescent current



R. Hogervorst et al., "A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries", IEEE JSSC, 1994

Commercial products

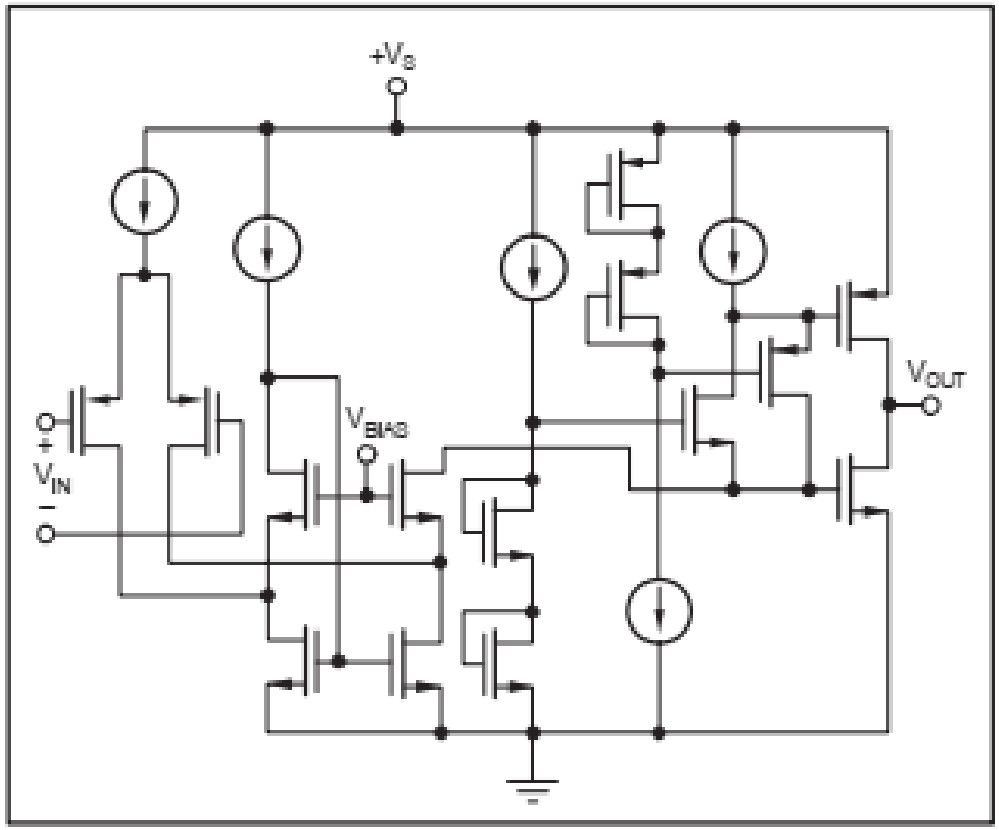


Figure 1. OPA30x Classic Two-Stage Topology