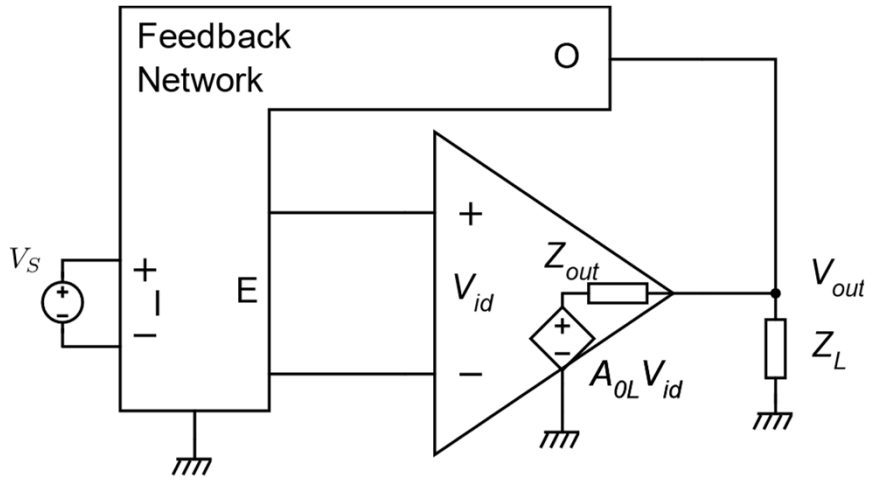
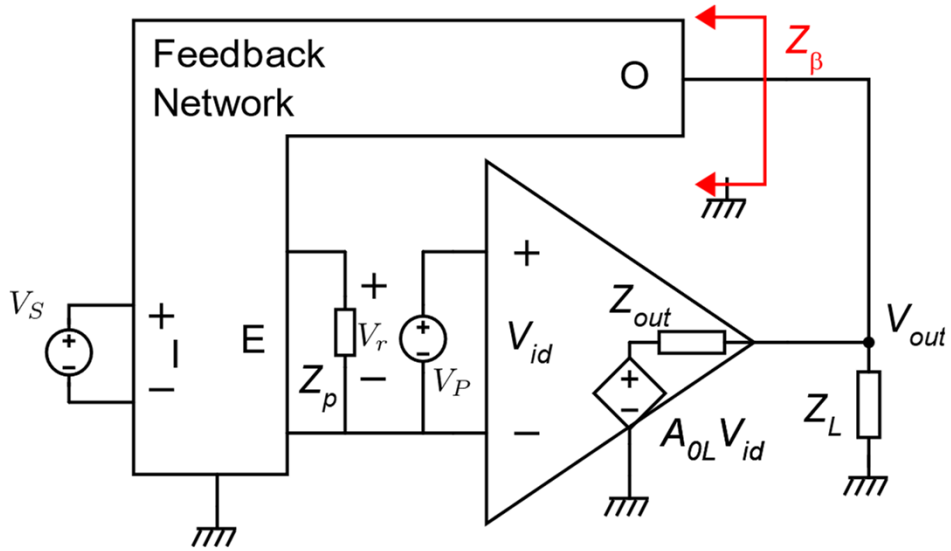
Single-Ended operational amplifiers

Typical requirements

- Voltage amplifiers
- Very large DC gain
- Stability over a wide range of negative feedback conditions.
- High input impedance on both inputs
- Differential input

Typical op-amp-based negative feedback loop





$$\frac{v_{out}}{v_s} = -\frac{\alpha^*}{\beta^*} = -\frac{\alpha_N}{\beta_N} \qquad \varepsilon_R \le \frac{1}{\left|\beta^* A\right|}\left(1+\left|\frac{\gamma}{A_L}\right|\right) \le \varepsilon_{R-MAX}$$

$$A = A_{OL}\frac{Z_\beta \,//\, Z_L}{Z_{out} + Z_\beta \,//\, Z_L}$$

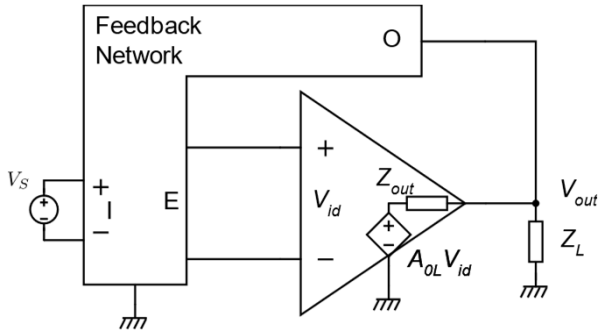
This is a design specification

Requirement on the output impedance

$$\frac{1}{\left|\beta^* A\right|}\left(1+\left|\frac{\gamma}{A_L}\right|\right) \leq \varepsilon_{R-MAX}$$

$$A = A_{OL}\frac{Z_\beta // Z_L}{Z_{out} + Z_\beta // Z_L}$$

Z_{out} should be low enough to guarantee that A is large enough to maintain the relative error below the maximum value allowed in all the expected load conditions



$$\text{load}: Z_\beta // Z_L$$

Example ADA4628 (Analog Devices)

Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 2.4 V	130	140	dB
		−40°C ≤ T_A ≤ +125°C	126		dB
ADA4528-1		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	125	132	dB
		−40°C ≤ T_A ≤ +125°C	121		dB
ADA4528-2		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	122	132	dB
		−40°C ≤ T_A ≤ +125°C	119		dB

R_{L1} A_1 A_2 R_{L2}

Passing from R_L=10kΩ to R_L=2 kΩ the amplifier looses around 8 dB

$$\begin{cases} A_1 = A_{OL}\dfrac{R_{L1}}{R_{L1}+R_{out}} \\ A_2 = A_{OL}\dfrac{R_{L2}}{R_{L2}+R_{out}} \end{cases} \Rightarrow R_{out} \cong 6\ \text{k}\Omega$$

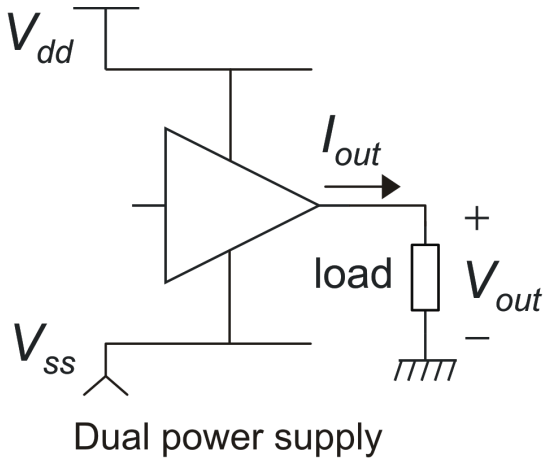
Output stages - specifications

$$-I_{ON-\max} \le I_{out} \le I_{OP-\max}$$

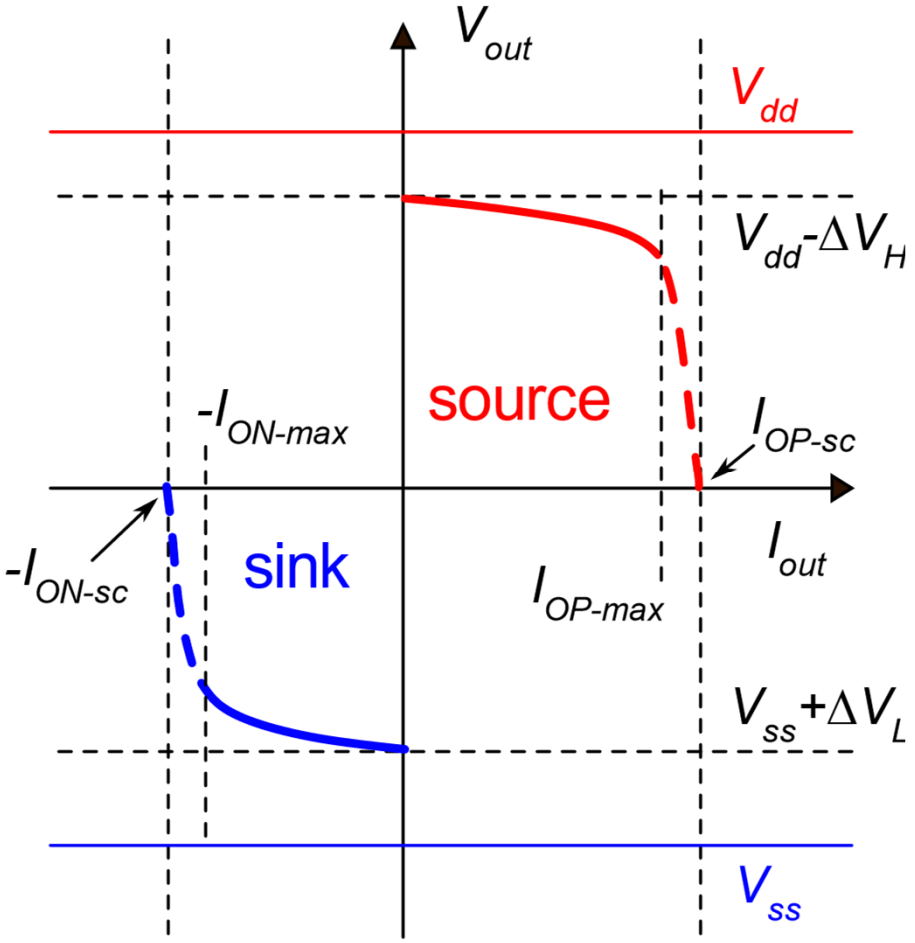
Sink Source

$$V_{out-\max} = V_{dd} - \Delta V_H$$

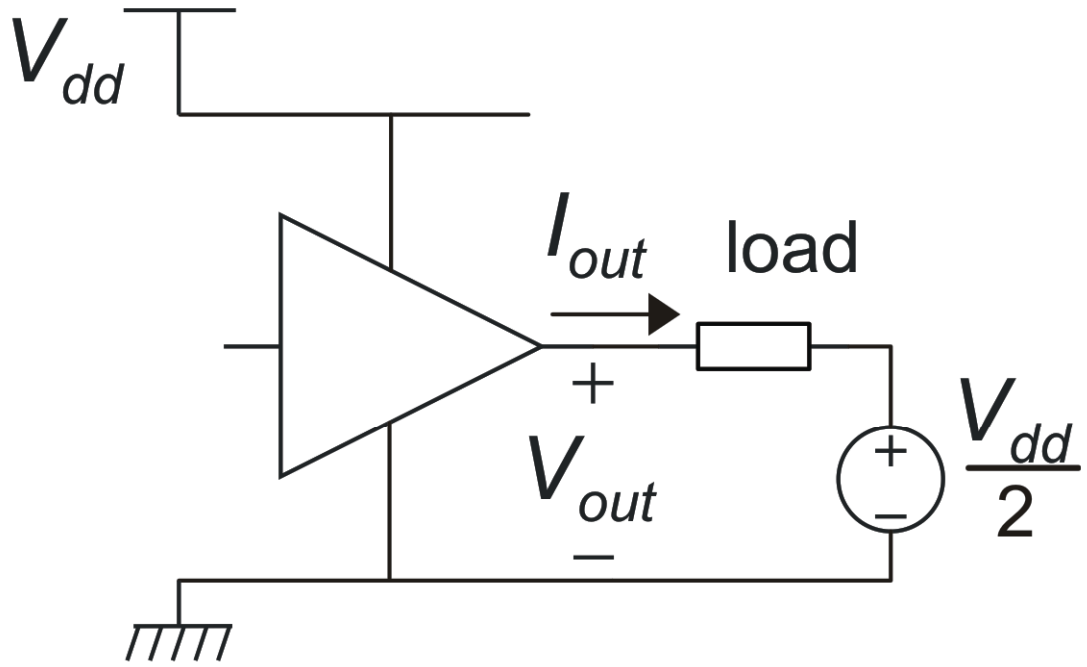
$$V_{out-\min} = V_{ss} + \Delta V_L$$



Dual power supply



Single supply case



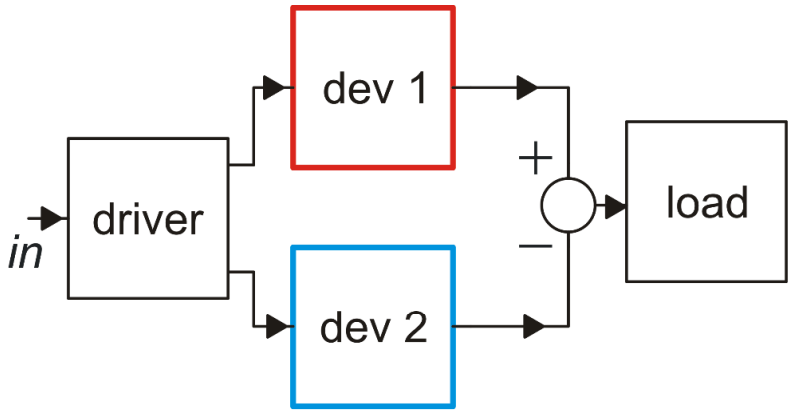
Single power supply

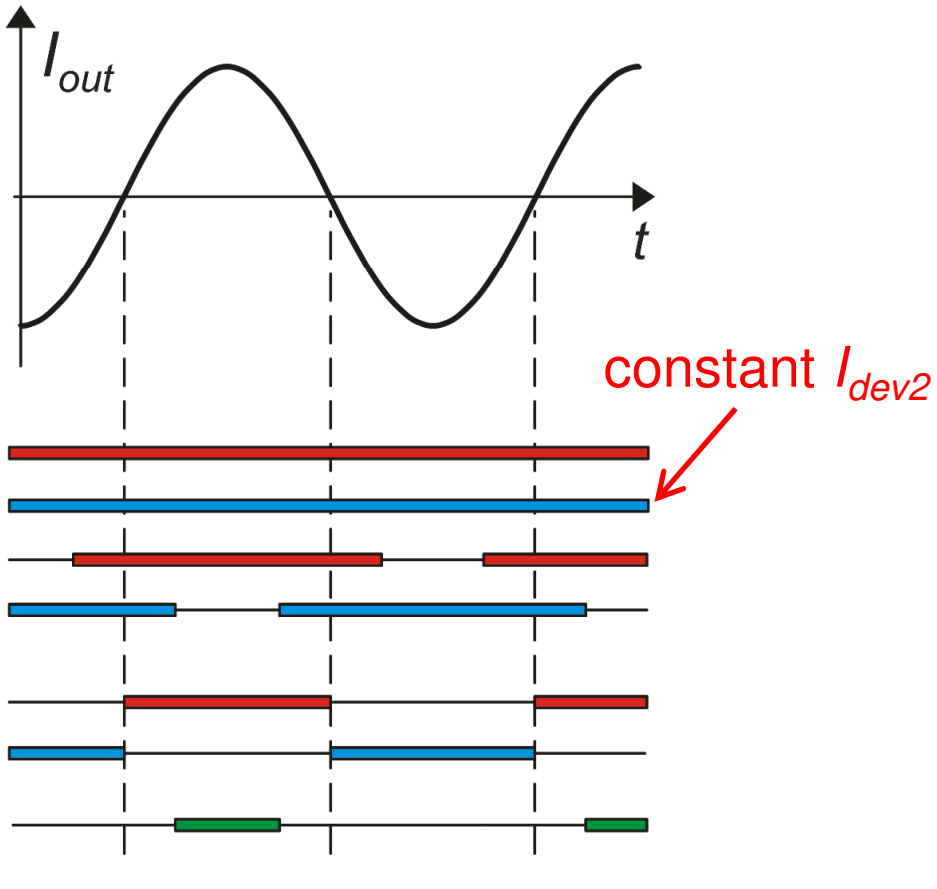
In a single supply voltage circuit, the load cannot be connected to *gnd* (or V_{dd}) if we want a to impose both positive and negative voltages across it.

To achieve this result, the load should be applied across the amplifier output port and a proper constant voltage, typically equal to $V_{dd}/2$.

This voltage must be generated by a proper cell, starting from V_{dd}.

Oputput stage classes

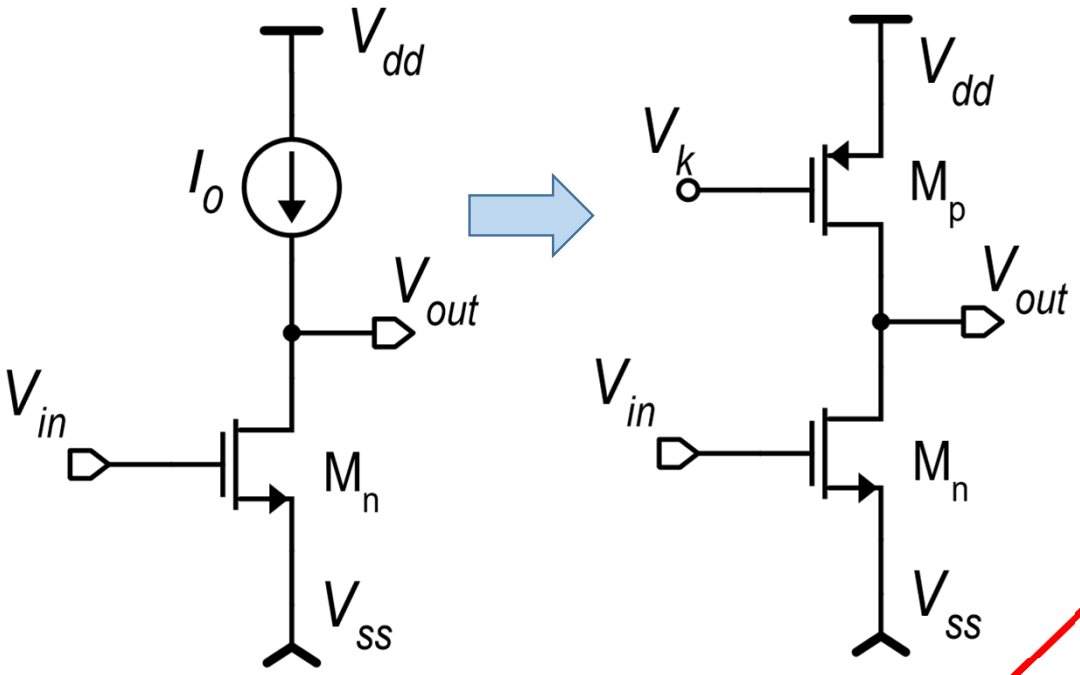




By subtracting two unipolar currents, we obtain a bi-directional output current

$$I_{out} = I_{dev1} - I_{dev2}$$

Common source output stages: class-A case



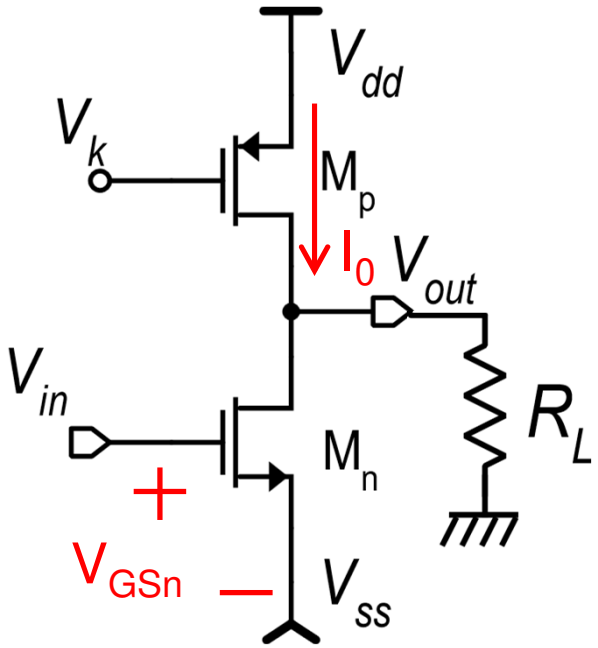
Margins to the rails are now only a V_{DSAT}, which is much smaller than a V_{GS}.

The common source output stage has a practically rail-to-rail output swing

$$V_{ss} + V_{DSATn} < V_{out} < V_{dd} - \left|V_{DSATp}\right|$$

Other info on the class-A common source

n-version



$$V_{in} = V_{in}(0) + v_{in}$$

$$I_{out} = I_{Dp} - I_{Dn}$$

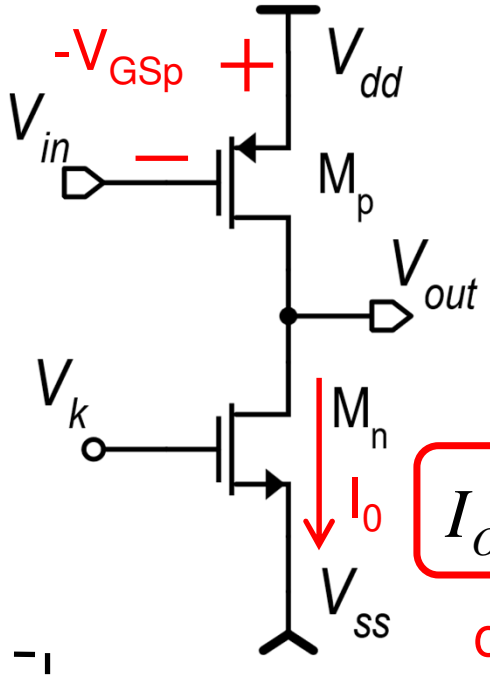
$$V_{in}(0) \Rightarrow I_{Dn} = I_{Dp}$$

$$I_{Dp} = I_0 = constant$$

$$I_{OP-MAX} = I_0$$

class-A

The input voltage is invariant to the supply voltages when it is referred to V_{ss}: the preceding stage should provide an output with the same property

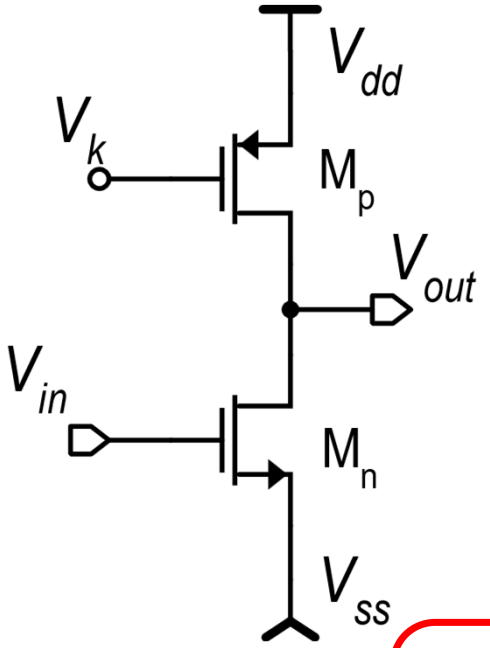


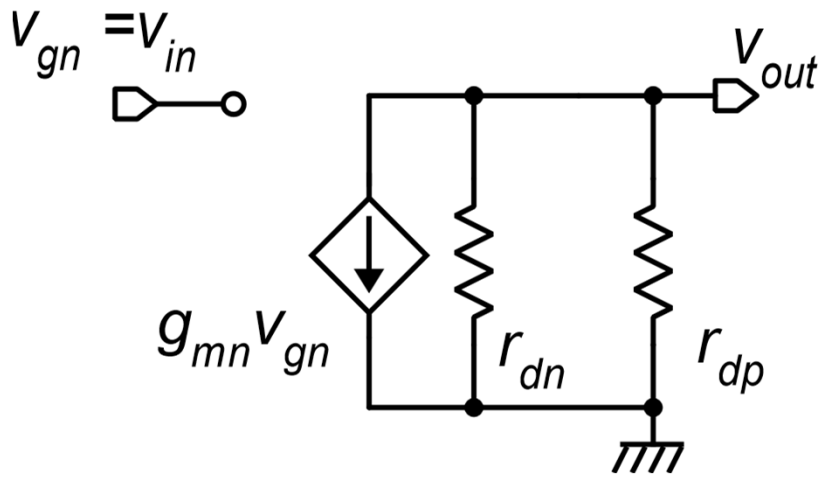
$$I_{ON-MAX} = I_0$$

class-A

p-version:
(the input signal is invariant when referred to V_{dd})

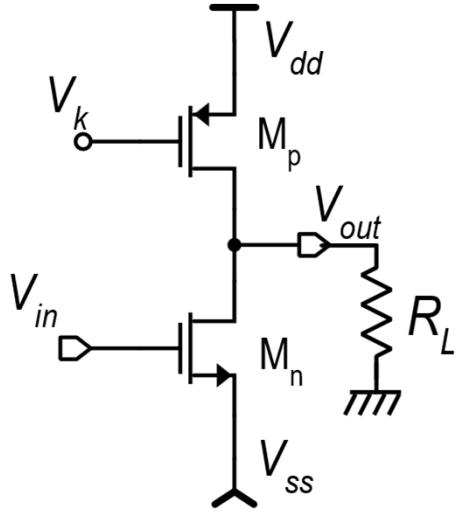
Small signal properties of the class-A common source stage





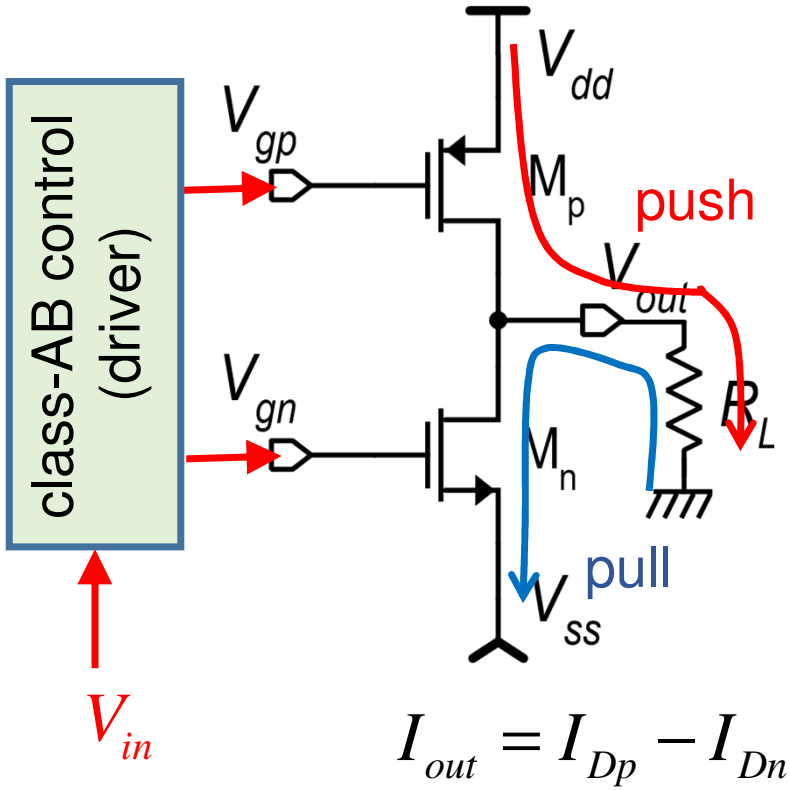
$$A_{VO} = -g_{mn}\left(r_{dn} \,//\, r_{dp}\right)$$

$$R_{out} = \left(r_{dn} \,//\, r_{dp}\right)$$

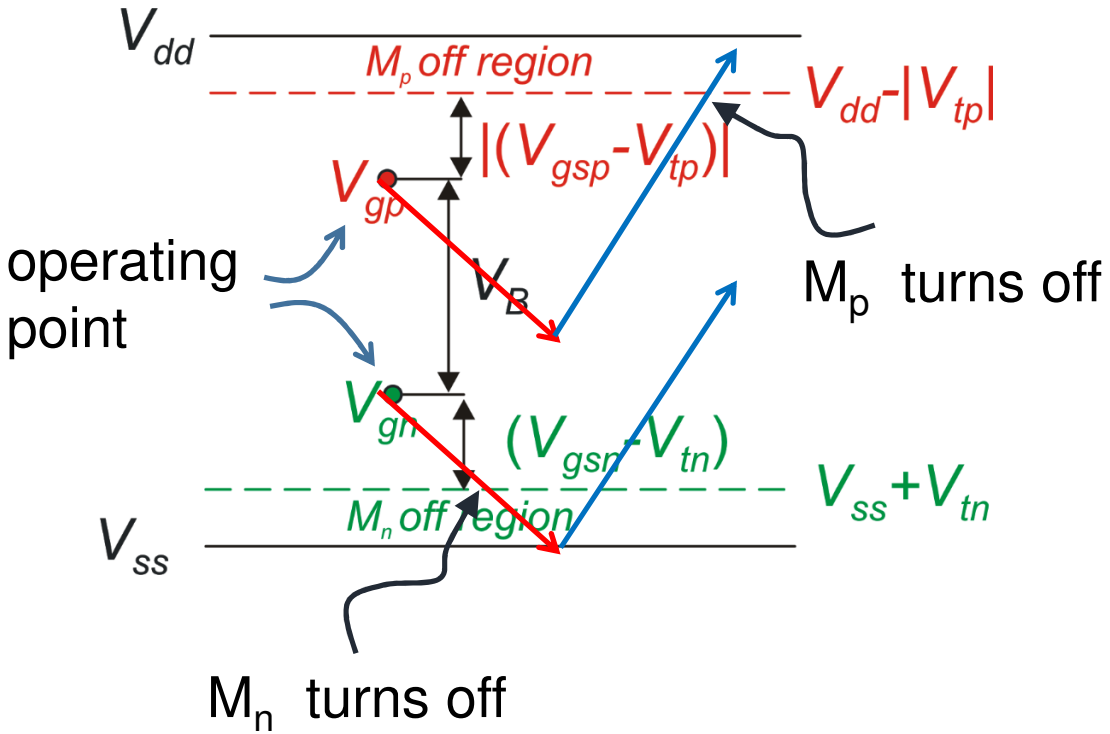


$$A_V = A_{VO}\frac{R_L}{R_{out} + R_L}$$

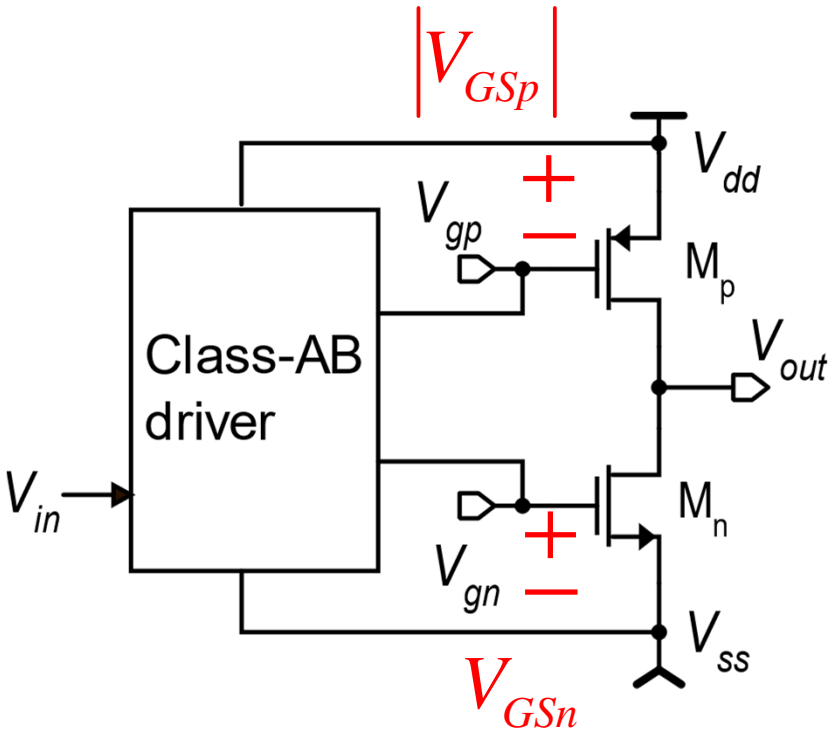
Class-AB common source: principle of operation



$$I_{out} = I_{Dp} - I_{Dn}$$



Class-AB common-source output stages: **maximum output currents**



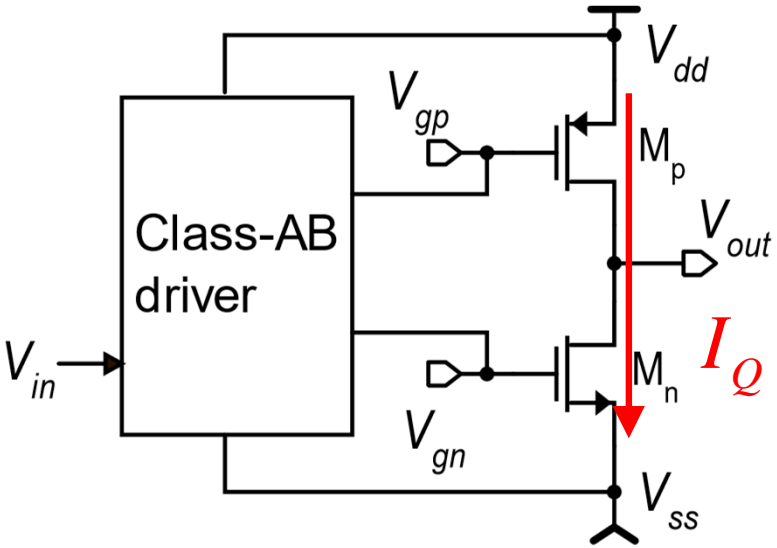
$$I_{OP-MAX} \approx \frac{\beta_p}{2}\left(\left|V_{GSp-MAX}\right| - \left|V_{tp}\right|\right)^2$$

$$I_{ON-MAX} \approx \frac{\beta_n}{2}\left(V_{GSn-MAX} - V_{tn}\right)^2$$

Driver ⇒ $|V_{GSp-MAX}|$, $V_{GSn-\max}$ ⇒ β_p, β_n

Different topologies are available for the class-AB driver. They differ for the maximum V_{GS} that can be delivered to M_p and M_n and for the minimum supply voltage

Class-AB common-source output stages: **quiescent current**



Quiescent condition: $I_{out} = 0$

$$I_{Dn}(0) = I_{Dn}(0) = I_Q$$

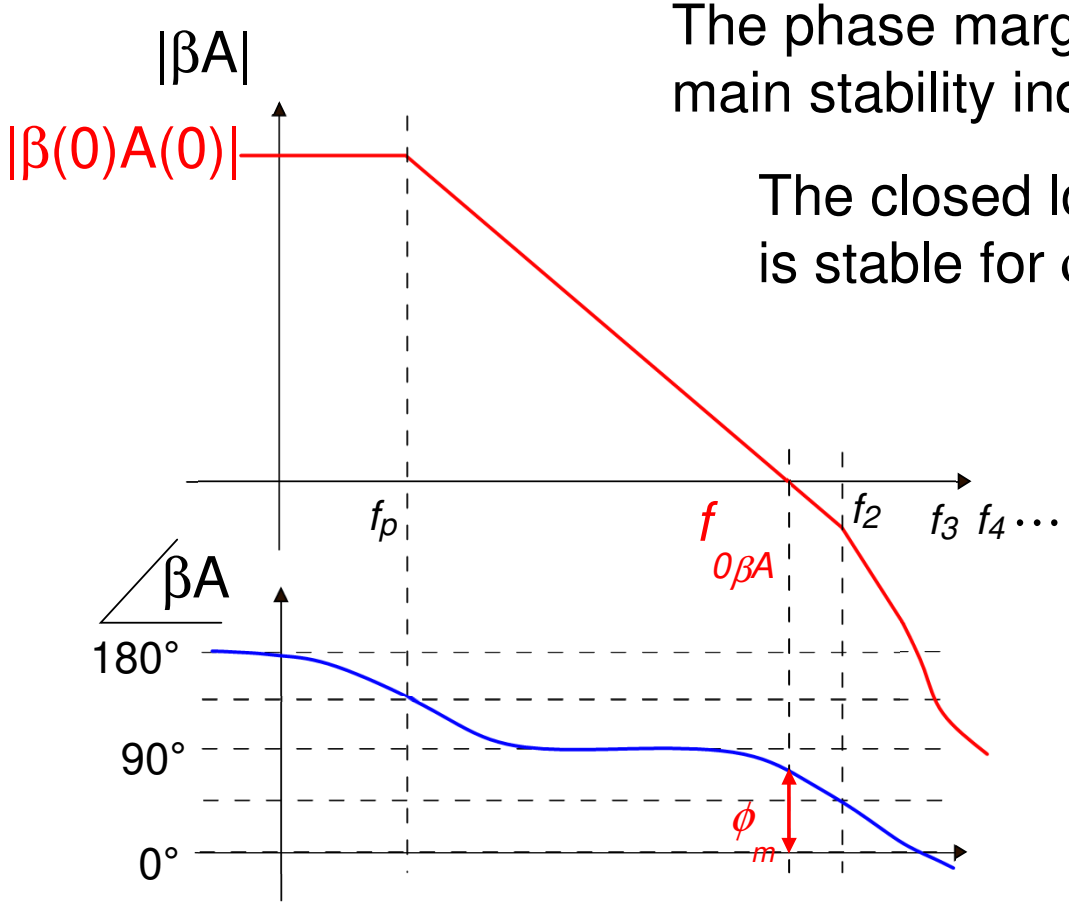
$$I_{Dp}(0) = \frac{\beta_p}{2}\left[\left|V_{GSp}(0)\right| - \left|V_{tp}\right|\right]^2$$

$$I_{Dn}(0) = \frac{\beta_n}{2}\left[V_{GSn}(0) - V_{tn}\right]^2$$

$$\Rightarrow \quad \left|V_{GSp}(0)\right| \qquad V_{GSn}(0)$$

The driver must be able to set the quiescent current with a good accuracy, since I_Q sets the operating point power consumption and the small signal performances of the stage

Frequency response requirements: closed loop gain (βA)



The phase margin (ϕ_m) is the main stability indicator

The closed loop configuration is stable for $\phi_m>0$

However, ϕ_m must be significantly greater than 0 to guarantee:

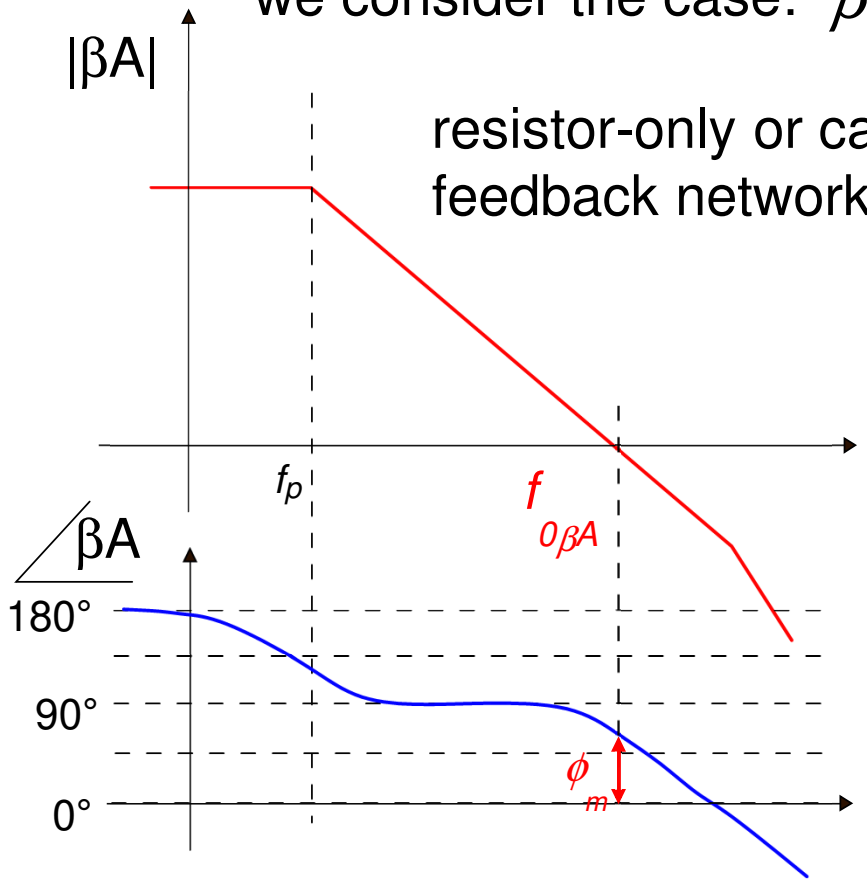
- Stability even against all possible PVT variations
- A step response with reduced ringing and overshoot

Typically, we require: $\phi_m>70°$

Amplifier gain and loop gain: role of the β factor

we consider the case: $\beta = real\ constant < 0$ ⇨ $A(0) > 0$ (for d.c. stability)

resistor-only or capacitor-only feedback networks ⇨ $|\beta| \le 1$

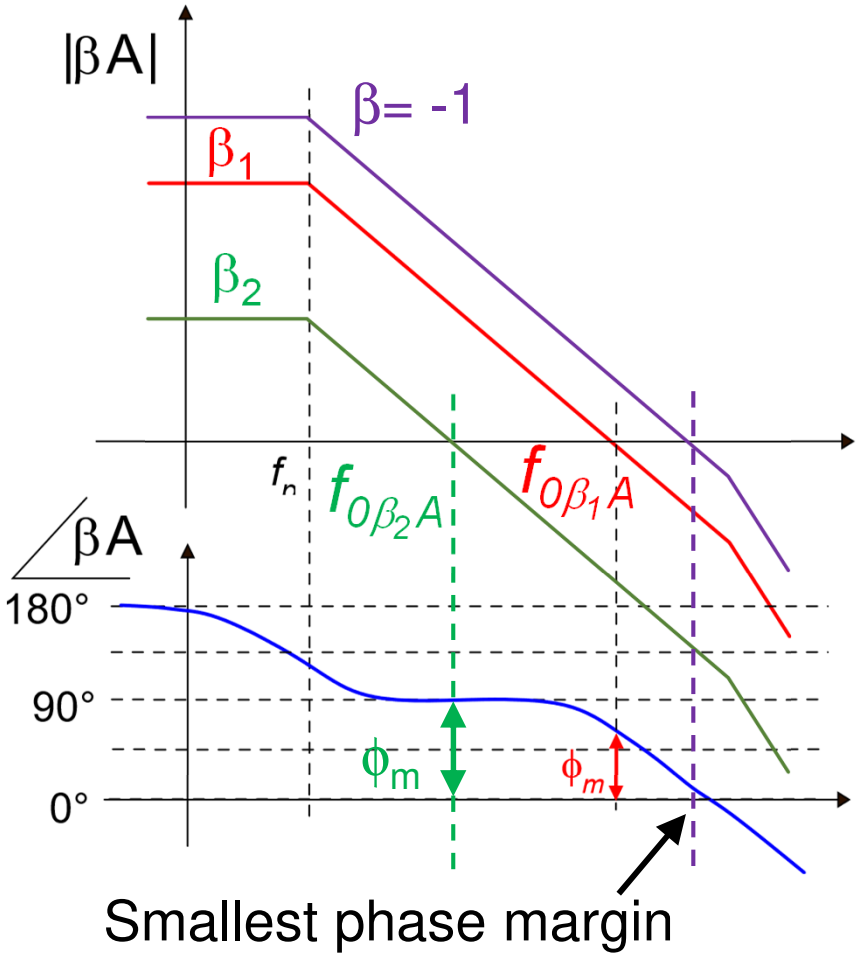


$$f_{0\beta A} = f_0 |\beta|$$

f_0 is the unity gain frequency of the amplifier, equal to GBW (Gain-BandWidth for a dominant pole response

In this case, f_{0bA} represents the -3dB upper band limit of the closed loop transfer function.

Amplifier gain and loop gain: role of the β factor

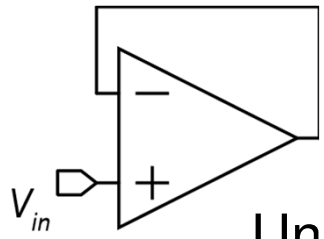


$$|\beta_2| < |\beta_1|$$

$f_{0\beta A}$ gets lower: smaller bandwidth for the closed loop transfer function.

ϕ_m increases: greater stability

Worst case for stability:
maximum |β|: β= -1

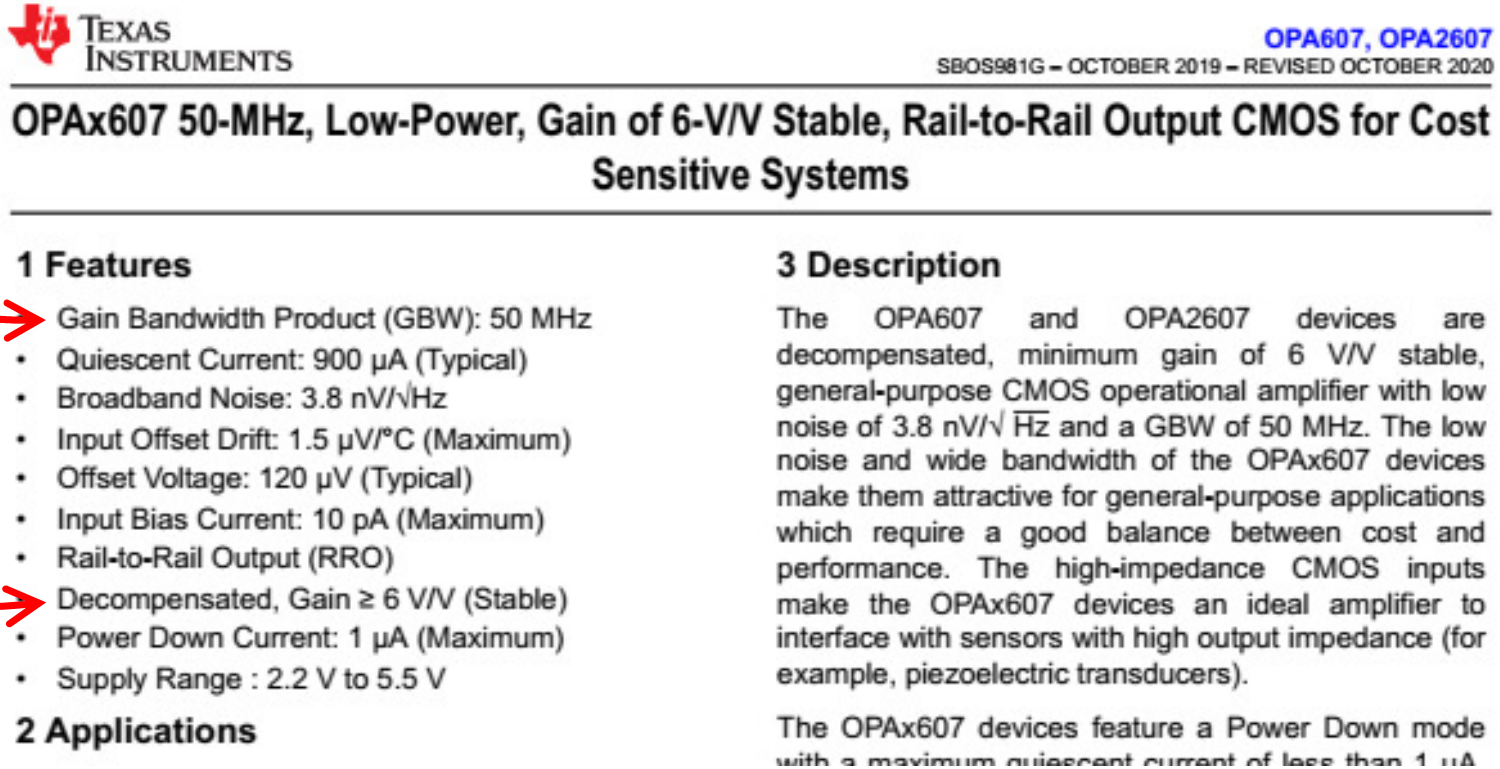


Unity gain configuration

Example of non-unity-gain stable op-amp

Stability for gains $\geq 6 \Longrightarrow \beta \leq \frac{1}{6}$ for non-inverting amplifiers config.

The advantage is a large GBW



TEXAS INSTRUMENTS

OPA607, OPA2607

SBOS981G – OCTOBER 2019 – REVISED OCTOBER 2020

OPAx607 50-MHz, Low-Power, Gain of 6-V/V Stable, Rail-to-Rail Output CMOS for Cost Sensitive Systems

1 Features

- Gain Bandwidth Product (GBW): 50 MHz
- Quiescent Current: 900 µA (Typical)
- Broadband Noise: 3.8 nV/√Hz
- Input Offset Drift: 1.5 µV/°C (Maximum)
- Offset Voltage: 120 µV (Typical)
- Input Bias Current: 10 pA (Maximum)
- Rail-to-Rail Output (RRO)
- Decompensated, Gain ≥ 6 V/V (Stable)
- Power Down Current: 1 µA (Maximum)
- Supply Range : 2.2 V to 5.5 V

2 Applications

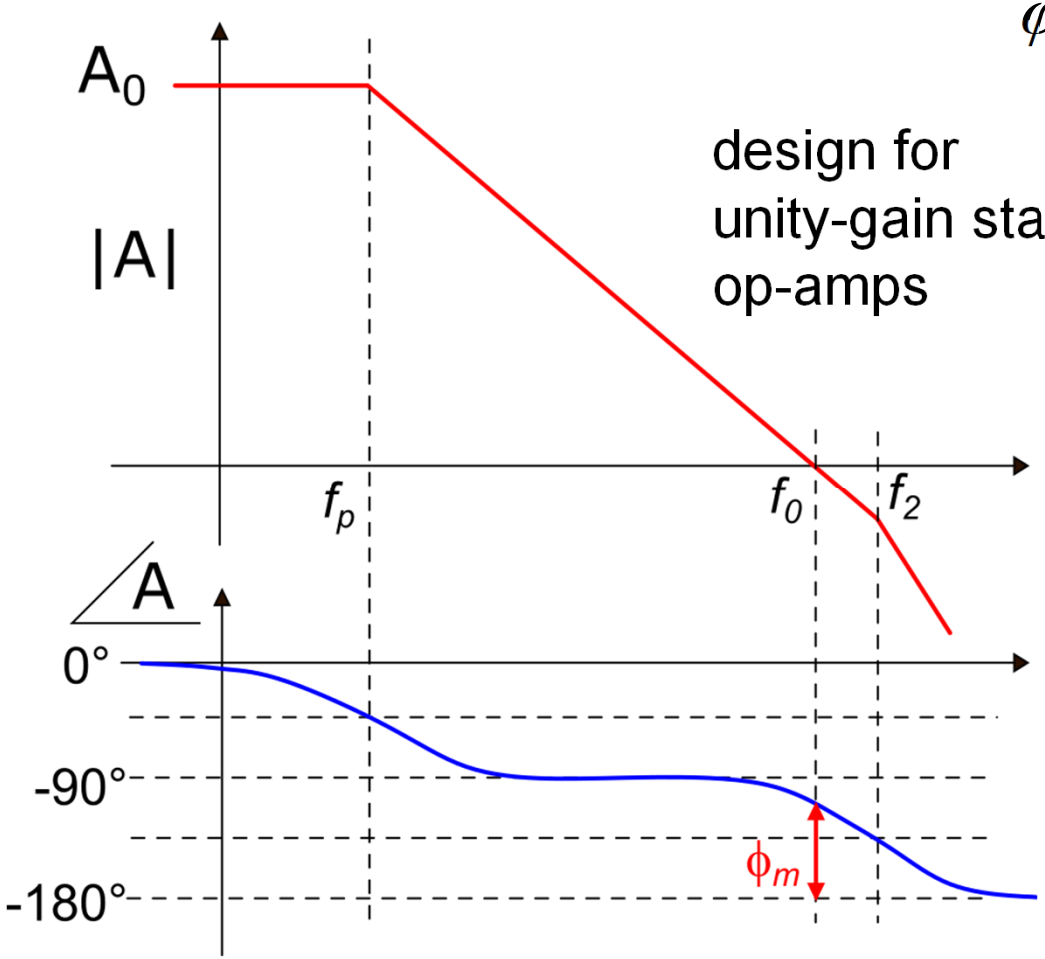
3 Description

The OPA607 and OPA2607 devices are decompensated, minimum gain of 6 V/V stable, general-purpose CMOS operational amplifier with low noise of 3.8 nV/√Hz and a GBW of 50 MHz. The low noise and wide bandwidth of the OPAx607 devices make them attractive for general-purpose applications which require a good balance between cost and performance. The high-impedance CMOS inputs make the OPAx607 devices an ideal amplifier to interface with sensors with high output impedance (for example, piezoelectric transducers).

The OPAx607 devices feature a Power Down mode with a maximum quiescent current of less than 1 µA

Single non-dominant pole case

$$\varphi_m = \pi - \frac{\pi}{2} - \arctan\left(\frac{f_0}{f_2}\right) = \frac{\pi}{2} - \arctan\left(\frac{f_0}{f_2}\right)$$



design for unity-gain stable op-amps

$$\varphi_m = \arctan\left(\frac{f_2}{f_0}\right)$$

$$\frac{f_2}{f_0} = \sigma$$

σ is an important design parameter

σ	0.5	1	2	3	5
ϕ_m	26.6°	45°	63.4°	71.6°	78.7°

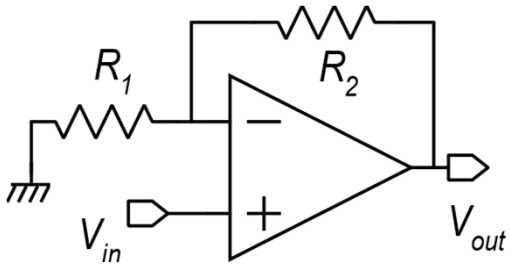
frequent choice

Design specifications for the amplifier response speed

- Gain-BandWidth product (GBW)

  For a single pole frequency response:

  1. $GBW \cong f_0$
  2. In a closed loop configuration, the upper band limit is given by: $f_H = GBW \cdot |\beta|$
  3. For the non-inverting amplifier: $f_H = \dfrac{GBW}{A_L}$



$$A_L = -\frac{1}{\beta}$$

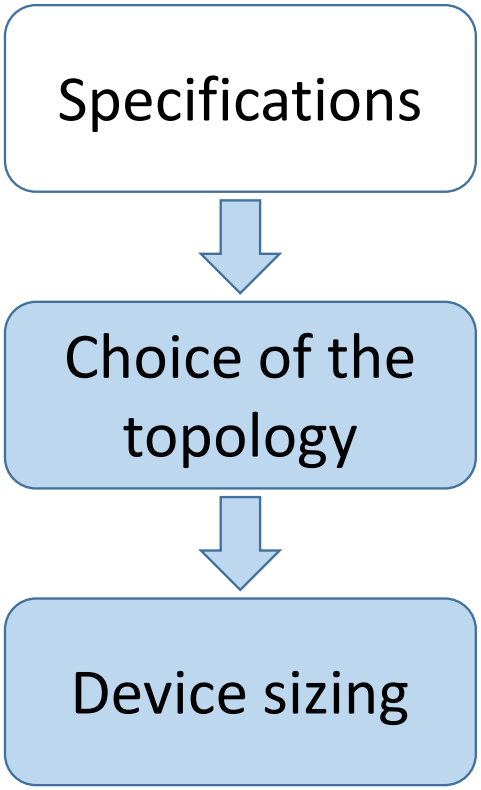
  The same relationships are approximately valid for dominant-pole frequency responses

- Slew rate (s_R): this is the maximum slope that can be obtained from the output voltage. The slew rate affects the behavior for large and fast input transients

A possible set of specification for design of a CMOS op-amp

- dc gain A_0
- Speed: Gain-Band-Width product (*GBW*) and Slew rate (s_R)
- Closed loop stability: e.g. phase margin in unity gain configuration and with a maximum capacitive load (C_L)
- Input referred voltage noise: Thermal : S_{vT}, Flicker: $k_F = f S_{vF}(f)$
- Offset (Input offset voltage: V_{io})
- Static power consumption (I_{supply}, minimum V_{dd})
- Maximum output current $I_{OP\text{-}max}$, $I_{ON\text{-}max}$
- Ranges: Input common mode range (*CMR*), output swing.
- *CMRR*, *PSRR*
- *Area*

Design of an anolog cell: phases



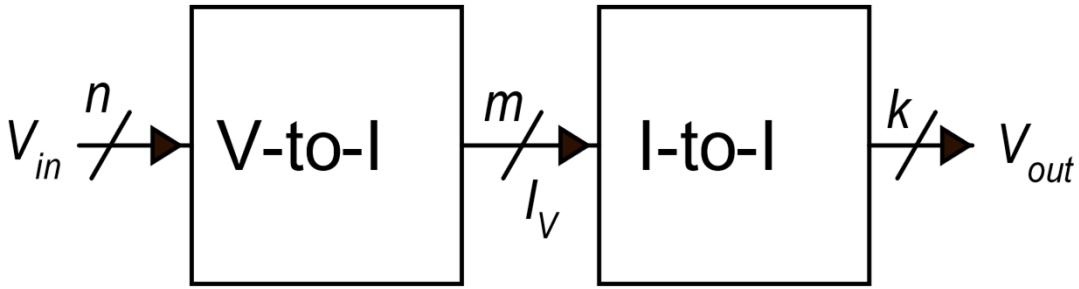
Number of stages, use of cascodes, amplifier class ...

We have to set the values of the Degrees of Freedom (DOFs): W, L, I_{bias}, V_{GS}-V_t ...

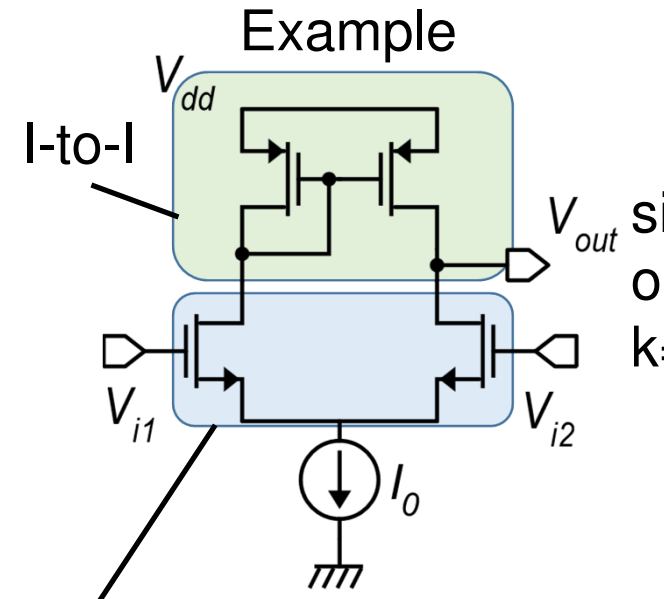
Operational amplifiers: number of stages

In the op-amp design terminology, the number of stages refer only to gain stages.

A gain stage is formed by a V-to-I converter and a network I-to-I that brings the output current(s) of the V-to-I converter to the output port.



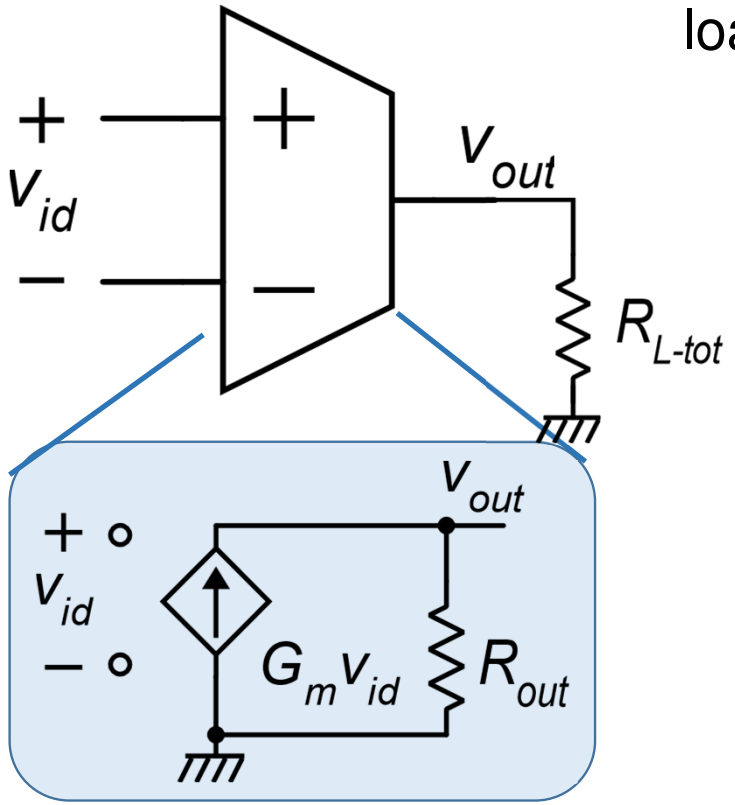
Example



single output: k=1

V-to-I : two inputs n=2
two outputs m=2

Single stage op-amps



In the case of no resistive load (only capacitive load, as in switched-cap. circuits:

$$A_{OL}(0) = G_m R_{out}$$

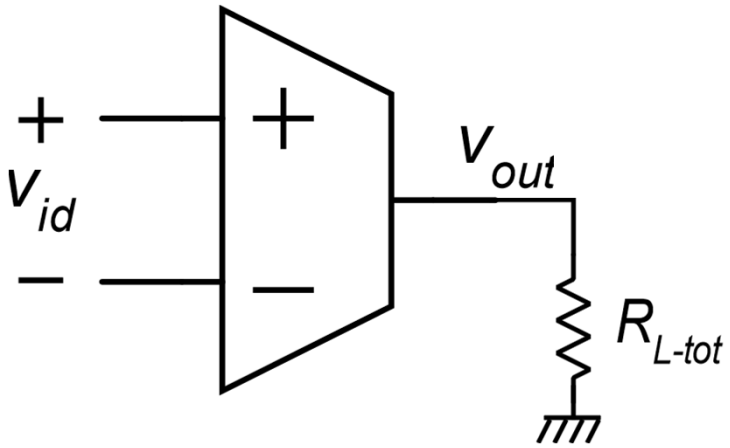
With very large R_{out} values, gains up to 100 dB can be obtained (cascode and regulated cascode architectures)

In the case of resistive loads, the gain falls down to

$$A_{OL}(0) = G_m \left(R_{out} \,//\, R_{L-tot} \right)$$

Includes the load brought by the feedback network

Single stage op-amps with resistive load



$$A_{OL}(0) = G_m \left(R_{out} \,//\, R_{L-tot} \right)$$

$$\text{for } R_{L-tot} << R_{out}$$

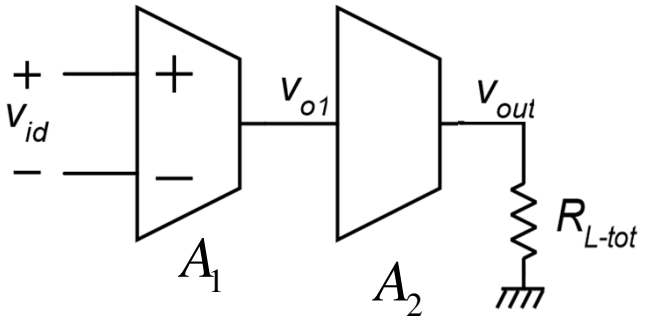
$$A_{OL}(0) \cong G_m R_{L-tot}$$

Can be as low as several tens of kΩ

In single gain stages, G_m coincides with the transconductance (g_m) of a single device or is a linear combination of device transconductances

In most practical cases, loading a single stage op-amp with an even **moderate resistive loads** means reducing the gain **to very small values**, not suitable for op-amp closed loop applications.

Two-stage op-amps



$$A_1 = G_{m1} R_{o1} \quad \text{(40 dB - 100 dB)}$$

$$A_2 = G_{m2} \left(R_{out} \,//\, R_{L-tot} \right)$$

$$A_{OL}(0) = A_1 \cdot A_2$$

- The resistive loads affects only the gain of the second stage.
- Even in the case that the gain of the second stage falls down to a few units, the total dc gain remains as large as to be suitable for most closed-loop configurations.
- The second stage is the output stage and must be designed to provide the required current and voltage ranges to the load.

Considerations on the op-amp number of stages

- **Single stage op-amps:** they can be designed to provide enough gain for a large variety of applications only in the case that the load and the feedback networks are capacitive (switched capacitor circuits). Their advantage is their simple frequency compensation and their power efficiency. Their stability increases with large capacitive loads.
- **Two-stage amplifiers:** they are the most popular options for general purpose op-amps since they are suitable for both capacitive and resistive loads and can be designed to provide very large dc gains. Their stability decreases with large capacitive loads.
- **Three-stage amplifiers:** this option is necessary when two-stage amplifiers cannot provide enough gain. This is the case, for example of very low supply voltages that prevent the use of cascodes. The gain of two-stage amplifiers can be too low also in the case of very fast op-amps, where the gain of each single stage is limited by the necessity to use short-length MOSFETs.
  Three stage amplifiers requires complicated frequency compensation strategies, such as the nested-Miller compensation combined with feed-forward paths (multi-path architectures)