Spice lesson: Fully differential amplifiers

Instructions for running the simulations

Preparation.

- Download the Ese_fully_diff.zip file
- Unzip the files into a new directory
- Descend into sub directory "Exe_total"
  Check that the following files are present in the subdir:
  Elementary building blocks

-) op_amp_core.asc	Fully differential folded cascode op-amp
-) bias_gen.asc, bias_gen.asy	Schematic and symbol of the bias genearator
-) CMFB_static.asc, CMFB_static.asy	Schematic and symbol of the CMFB block

  Complete amplifiers and test benches:

-) op_amp_complete.asc	Test-bench of the complete op-amp
-) op_amp_DDA_inamp.asc	DDA- based in-amp
-) op_amp_DDA_buffer.asc	DDA used to implement a fully-diff buffer
-) opamp_fully_diff.asc, opamp_fully_diff.asy	To be used in the SC amplifier
-) amp_SC.asc	Switched Capacitor (SC) Amplifier
-) op_amp_CM_dyn.asc	Example of dynamic CMFB

Note, some test-benches include different simulation command lines. Command lines beginning with a semicolon (;) are not active. In order to activate a single simulation type (e.g. tran, noise etc) delete and insert semicolon in such a way that only one command line at a time is active.

Execution of the exercises.

Note:

-) In order to facilitate the application of differential signals by specification of the common mode and differential components, use the following block: **se_2_diff** (Ideal library of the DK).

-) In order to decompose a differential signal into a common mode and a differential signal, for a better representation of the results, use the following block: **diff_2_se** (Ideal library of the DK).

Part 1

- Open the op_amp_core schematic.
- Make an instance (F2) of the bias_gen block
- Connect (F3) the terminals VbiasN, Vk1 and Vk2 of the bias_gen to the corresponding nodes of the opamp (suggested method: copy (F6) the labels and place them to wires going out the block)
- Connect terminal Vb of the bias_gen to the Vcmfb node of the opamp
- Place a voltage source (Vdd, 2.5 V) and connect it to the Vdd of both the opamp and bias gen.
- Create a common-mode / differential source and connect it to the input of the amplifier. Set the common mode voltage to 1.25 V and the differential one to 0

- Run an .op simulation and check that everything is correct:
  -) VbiasN=0.63435 V
  -) Vk1=1.058 V
  -) Vk2=1.41538 V
  -) Vb=1.7145
  The total current in the V_{dd} source is 222 µA
- Run a dc sweep (V_d, -2m, 2m, step 10u) And note that the outputs are shifted to V_{dd}.
- Let us try to correct the situation by adding a little more Io current (Increase W_{01} from 40u to 41u) and note that the output common mode is very sensitive since now it is saturated to the lowest end of the output range.
- Try to apply smaller corrections. Note that it is possible to obtain and acceptable response with W_{01}=40.05, but clearly this not feasible, since even a 1 % process error would make the amplifier not usable.

Part 2: Build an output common mode circuit.

- Set W_{01} back to its nominal value 40u.
- Make an instance of the common mode feedback control (CMFB)
- Connect all the input and outputs (suggseted: by labels) and V_{dd}.
- Detach V_{cmfb} from the bias_gen "V_b" output and connect it to the V_{cmfb} output of the CMFB-static block.
- Insert a voltage source (1.25 V) to the V_{ref} input of the CMFB block.
- Run again the sweep and display V_{o1}, V_{o2} showing the correct operation.
- Create the V_{od} and V_{oc} "calculators" to see better what happens to the common mode and differential mode.
- Calculate the DC gain by using the cursors.
- Modify W_{01}, showing the robustness of the control.

Part 3. Stability of the CMFB loop.

- Set the Vref source to produce a step from 1.3 V to 1.25 V with the following schedule: step at 1u, rise time 10n . (use pwl). Simulate for 10u. Note the onset of oscillations at the application of the step. (Note: if the step is not applied, the oscillation starts as well, at around 1.6u
- Place two capacitors of 2 pF from the outputs to ground and simulate again, verifying the achieved stability.

Part 4: Noise.

- Launch a noise simulation with Output=Vod, Input=Vd (The differential voltage source).
- Show that I_noise does not decrease at high frequency (on the contrary, it has a peak). Explain, showing the Onoise and the gain that that we see the result of a mathematical operation, but that noise is not present in any point of the circuit.

- Referring to a SC usage, connect the amplifier in closed loop (reset configuration) by using the labels (in order to modify as little as possible the circuit). Run again and note that the spectrum (Onoise, but equal to the noise present at the amplifier input), now does decrease at high freq. but a peak is still present.
- Increase the capacitances to 5 p and show that the peak has disappeared.

Part 5: Build a DDA.

- Transform the operational amplifier into an operational DDA, by placing a new differential pair and modifying M3-M4 current sources in order to account for the increased bias current produced by the new pair.
- Check the operating point by placing the inputs of the new port to Vc=1.25 V).
- Close the DDA in buffer conditions (remove connection of the new port to Vc and connect it to the output port, taking care to get negative feedback). Note that the output swing is limited by the input differential range of the input pairs. (This is a limit of this DDA architecture when used to build in-amp with small gains)
- Try to build an instrumentation amplifier using a negative feedback.

Part 6: Simulate a switched capacitors fully-differential amplifier.

- Use the complete fully-differential amplifier indicated with "opamp_fully_diff" (provided of a symbol for easy instancing into an upper hierarchy level), the clock generator "ck2ph" and the switch "pass_gate" to build the amplifier. The pass-gate terminals are T1 and T2, while vc is the control terminal and nvc is the (required) negated version of vc.

Part 7: Simulate a dynamic Common Mode control.

- Use file: op_amp_CM_dyn.asc : the common mode control is placed on the top-right corner, together with the required 2-phase clock generator. The input differential signal is a 200 μV sinusoid.
- Launch the transient simulation (4 ms) and plot the output differential mode (vod) and common mode (voc) signals.
- Note that the amplifier starts in a saturation condition (both output voltages are close to Vdd). This is because the CM stabilization is not effective in setting the correct operating point.
- Note that the common mode stabilizes to 1.25 v after a few clock cycles: the Dynamic CM control works correctly.
- The differential mode develops after the correct CM voltage is established.
- Spikes are present on the differential mode: this is a clock-feedthrough artifact. The cause is the charge drawn at each clock cycle by capacitors C3 and C4 when they are connected to the output port (phase 2).