1. General information.

Uncompress the Ese_opamp.zip file into an empty directory. LTSpice must be configured by including the DK (design kit) directories in its model and lib path. Double click on the desired test-bench to execute it by means of LTSpice. Close LTSpice before executing a different test-bench.

2. File list.

opamp_2A.asc:	Schematic view of the opamp
opamp_2A.asy:	Symbol of the opamp
00_test_operating_point.asc	Test bench for operating point
01_test_risp_freq.asc	Test bench for open loop frequency response
01b_AC	Test-bench for common mode gain
02_test_tran_unity_gain.asc	Test bench for transient response in unity gain config.
03_test_noise.asc	Test Bench for noise analysis in gain=10 closed loop config.

3.. Suggested simulations

3.3 Operating point:

Open test bench 00. Edit capacitor C_1 and check that the parallel resistance has been set to $1x10^{15}$ Ω (1000 TΩ). This is higher than the default value (1 TΩ) that would cause a 1 pA current to flow into feedback resistor R_1 and make the input (inverting input) and output voltage slightly different.

Open the LTSpice control-panel (menu: Tools->Control panel) and check that the tab "Save defaults" has the "Save Subcircuit voltages" active.

Run the simulation and see the pop-up window with the node voltages. Check that the output voltage is very close to 1 V (1.0000125 V), confirming that the output replicates the voltage applied to the non-inverting input. The very small difference (12.5 μV) is due to both systematic offset (due to non-ideal behavior of the current mirrors, caused by V_{DS} effects) and finite gain).

The node voltages can be read also by placing the mouse pointer over the node of interest. The value is displayed on the bottom-left corner of the screen. Place the mouse over the op-amp symbol and right-click. Choose to open the op-amp-schematics in the pop up window. The opamp node voltages can be read by placing the mouse pointer on the desired node.

Go back to the test-bench (see the tabs on the upper-left corner) and open the "Spice Error Log" file (menu View->SPICE Error Log) and find the operating point of all mosfets in the op-amp (indentified by u1, u2 etc.). Note that:

- The Vdsat of M1 and M2 are close to 0.1 V, while those of other mosfets are around 0.3 V as designed.
- The g_m's are smaller than designed. In particular, g_{m1} is 0.465 mS, instead of the designed value of 0.63 (25 % difference) . This is due to the fact that we used a strong inversion formula, while, with a $V_{GS}-V_t$ of 0.1 V, M1 and M2 are already in moderate inversion. Note that g_{m5} is more precise (13 % difference).

3.2 Frequency response.

Open test bench 01. A graph with no traces opens. Select the V(out) trace to display, from menu: Plot Settings ->Visible traces, or simply go over the output node with the mouse and left-click. Click the trace label (center top of the graph window) to display the cursor. Use the cursor to find the unity gain frequency (f_0), coinciding with the GBW. Note that the GBW is smaller than designed (6.8 MHz) and the phase margin is around 62°. The smaller GBW is due to the smaller value of g_{m1} (see the operating point discussion). We can correct this discrepancy, if required, by reducing C_C.
-) Change C_C from 10pF to 6pF and run again the simulator. Note that now the GBW is around 10 MHz, but he phase margin is dropped to 48°. The amplifier will be still stable in unity gain configuration, but damped oscillations are going to appear in the step response.
-) Reset C_C to 10 pF and increase the load capacitance (C_L) to 100 pF. Re-run the simulation and note that the phase margin is decreased to 26°. Incidentally, see that ω_0 is also reduced, since ω_2 has reduced so much that now it affects ω_0 (the slope is no more constant up to ω_0).

3.3 Transient response in unity gain configuration.

Open test bench 02. The input source (V2) has been configured to produce a small step (at 1 mS, from 1 to 1.1 V). If you have changed C_C in previous simulations, than set it back to 10 pF. Run the test-bench and display trace V(out). Note that the response has a small overshoot but no damped oscillations. The settling time (to 1 %) is nearly 125 ns. In order to test the effect of compensation resistor R, change it from 532 Ω to 0. Run the simulator again and note that damped oscillations appear (due to a smaller phase margin). An initial decrease of the response is also visible, in agreement with the presence of a positive zero.
Set the resistance back to 532 Ω and perform the following tests:
-) Increase the output capacitance to 100 pF and run the simulation again. See dumped oscillations appear, as a result of the reduced phase margin (ω_2 shifts below ω_0).
-) Reset the output capacitance to 10 pF. Set the compensation capacitance to 6pF, in order to obtain a 10 MHz GBW. See that damped oscillations appear, due to the reduced phase margin (ω_0 increases getting closer to ω_2).
-) Progressively reduce C_C and note that below 1 pF the amplifier become unstable in this configuration and free oscillations start. Note that oscillations are not present before the input voltage step. In a real circuit, oscillations do not need an input signal to start, since the presence of noise is just sufficient to initiate them.

3.4 Noise analysis.

Restore the initial 10 pF value for C_C. Open test-bench 03. The op-amp forms a unity gain configuration. The simulation command is set for (AC) noise analysis. The result is the output noise spectrum and the RTI noise spectrum (referred to V2). Run the simulation and display the V(inoise) and V(onoise) spectra.
Left-Click on the Y-axis to select logarithmic scale. After that, right-click on the axis and chose “auto-Range Y axis”
The V(inoise) and V(onoise) spectra are equal as long as the gain is equal to 1. When the gain gets smaller than 1 (due to the finite bandwidth of the amplifier, nearly equal to the GBW in this configuration) the RTI value increases. Thus, the RTI noise increase is simply a mathematical effect.

The noise on the inverting input, which is often sampled in switched capacitor circuits, follows the output noise spectrum, so that the noise bandwidth is upper-limited by the GBW. The following values can be extracted from the simulation (using the cursors).

-) $\sqrt{S_{BB}}$ (due to thermal noise) = 9.6 nV/$\sqrt{\text{Hz}}$ (analytically calculated value: 6.7 nV/$\sqrt{\text{Hz}}$

-) $\sqrt{S_{vF}(1Hz)}$ =3.28 μV/$\sqrt{\text{Hz}}$ (analytically calculated value: 2.72 μV/$\sqrt{\text{Hz}}$)

The flicker noise prediction can be considered in good agreement with the simulations, while the simulated thermal noise is significantly higher than predicted. There are two reasons for this discrepancy: (1) g_{m1} turned out to be smaller (see paragraph 3.1) than designed and (2) the formula used in the analytical calculations was missing the $(1+g_{mB}/g_m)$ factor, which can be estimated to be around 1.2).

If the "save sub-circuit node voltages" has been selected in the "save defaults" of the control panel, also the contributions of all mosfets to the output noise are present in the available traces.
The thermal noise contribution is indicated with the "id" suffix, while the suffix for the flicker noise is "1overf". It is possible to note that the larger contribution comes from M1 and M2, as designed.