Output Stages and simple operational amplifier topologies

1.1 General considerations and definitions.

In an analog circuit, the output stage should deliver the required power to the load. The typical specifications of an output stages are:

-) Output voltage range
-) Output current range

The voltage range consists of a maximum and minimum value. These values are generally given as distance to the positive and negative power rail, respectively. Therefore, we generally use the following notation:

$$V_{out-\max} = V_{dd} - \Delta V_H \ ; \quad V_{out-\min} = V_{ss} + \Delta V_L \tag{1}$$

Generally, a parameter of merit is obtaining a small margin to both rails, i.e. minimizing ΔV_H and ΔV_L. However, there are applications where only one of the margin is important, since we do not require to get close to one of the two rails.

As far as the currents are concerned, we distinguish the case when the stage is sourcing a current (positive current) from the case when it is sinking a current (negative current). For both cases, the maximum absolute value is specified, so that:

$$-I_{OM-\max} \le I_{out} \le I_{OP-\max} \tag{2}$$

For a general-purpose output stage (such that of operational amplifiers), the amplifier should be able to source and sink currents equally well, in order to apply negative and positive voltages to the load. To understand this, just think of an amplifier that should produce a sinusoidal waveform across a low resistance load. If the amplifier is capable of sourcing high currents but can sink smaller ones, then it will not able to correctly produce the negative half-wave and a distortion will occur in presence of large signals.
Therefore, for general-purpose output stages, the current limit is given by the smaller between I_{OM-max} and I_{OP-max} (worst case). We have to point out that, in particular cases, only one of the current limits is important. A relevant case is that of the voltage regulators, which are devices used to produce a constant and precise power supply form a source (i.e. a battery) that may vary with time, temperature and load condition. In this case, the output stage should only be able to source (positive regulator) or sink (negative regulator) a large enough current. In these cases, the design of the output stage is greatly simplified.

We have to add that current and voltage specifications are not independent. The maximum output voltage that a stage can produce progressively decreases as the output current is increased. For this reason, an output characteristic is often provided. Possible output characteristics are schematically shown in Fig. 1 for the case of dual and single power supply.

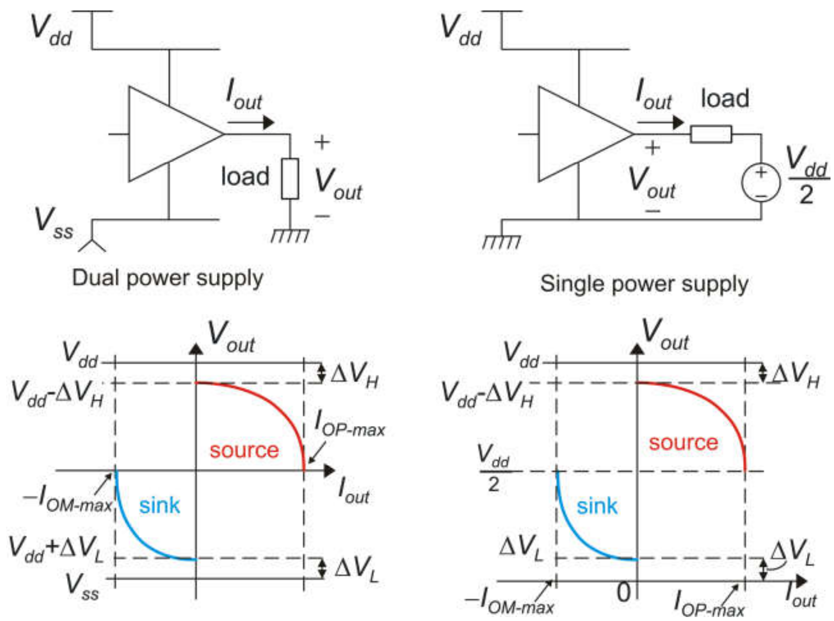

Fig.1 – Example of output characteristics for the case of dual and single power supply. Note that for the single supply case, the test condition requires one load terminal to be connected to a $V_{dd}/2$ source, in order to allow for positive and negative currents.

Another important factor that has to be considered for stages that are designed to deliver power to a load is the "class" of operation. Fig.2 summarizes the main output stage classes. The block diagram provides an abstract representation of an output stage. Two distinct devices (i.e. transistors) can be used to deliver power to the load. The proper input signals to the output devices (dev 1 and dev 2) is provided by a driver stage, which, in turn, is controlled by the input signal (in). A passive summing stage (a simple wire junction or, in older amplifier, a transformer) combines the output signals of dev 1 and 2 in a constructive way to produce the final output signal that drives the load.

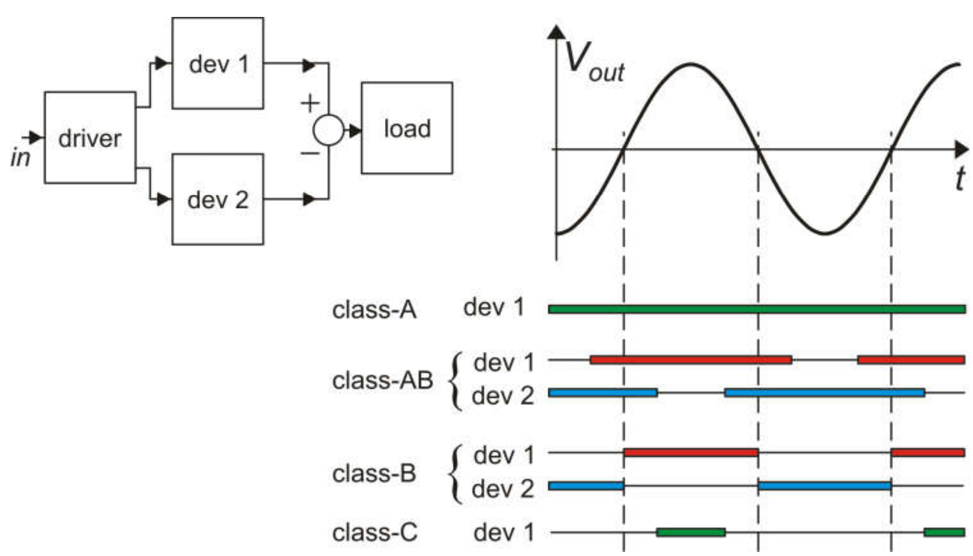

Fig.2 Output stages and class of operation: abstract block diagram of an output stage (left) and intervals of activity for dev2 and dev1 across the signal period (right).

To understand the definition of class, we have to consider the case that the output signal should assume large negative or positive values. To simplify the definition, reference to a pure sinusoidal signal is generally made as in Fig.2. The class of the output stage indicates the fraction of the signal period where a single output device is on. In class-A stages, there is only one device (e.g. dev 1). To ensure linear operation, this device should be always on across the whole period.
In class AB, we have both devices 1 and 2, so that they can be alternated during the signal period. In order to guarantee that there is always a device that is handling the signal, the periods where the devices are on should overlap, so that each device is on for more than one half-period. Class B is a particular case of class-AB, and consist in reducing the overlap to zero, so that each device is on for exactly half period. In class-C output stages, there is again one only device, which is on only for less than one half-period. This class cannot be used in linear stages since it introduces a huge amount of distortion. It is used only in RF amplifiers, in combination with a high-Q RLC resonant circuit to filter out all harmonics that are produced by its intrinsic nonlinear behavior. It has been recalled here only for comparison purposes and, similarly to other classes (such as class-D), will be not considered in the remaining part of this document. Then, we will consider only class-A, AB and B stages.

An important difference between class-A stages and class AB / B is the consequence of having only one device working. Considered that the sign of the current in a transistor cannot be reversed, we have to provide a bias current, which is at least equal to one-half of the maximum current flowing through the device. This situation is illustrated in Fig.3 (left). In order to have a current of both sign, the DC value (I_{bias}) should be removed, obtaining the output current shown in Fig.3 (right). In integrated solutions, cancellation of the DC component occurs by direct subtraction of the I_{bias} component. It is clear that the maximum peak current that can be delivered to the load without distorting the signal is equal to I_{bias}. Then we can draw the following fundamental conclusion:

> In a class-A output stage the worst case between the maximum positive ($I_{OP\text{-}max}$) and negative ($I_{OM\text{-}max}$) current cannot be larger than its bias current. In simpler words, the quiescent current adsorption is higher than the maximum output current that the stage can deliver in a symmetric way).

In class-AB and B stages, the bias current of the output devices (which contribute to the quiescent current adsorption) is independent of the maximum output current. For this reason, class-AB is generally adopted when high output currents with small bias current are required. In class-B stages the bias current is ideally zero. This is not an acceptable condition in linear stages, since important parameters, such as the transistors g_m's would be zero in quiescent conditions, degrading the performances (e.g. bandwidth) for small signals.

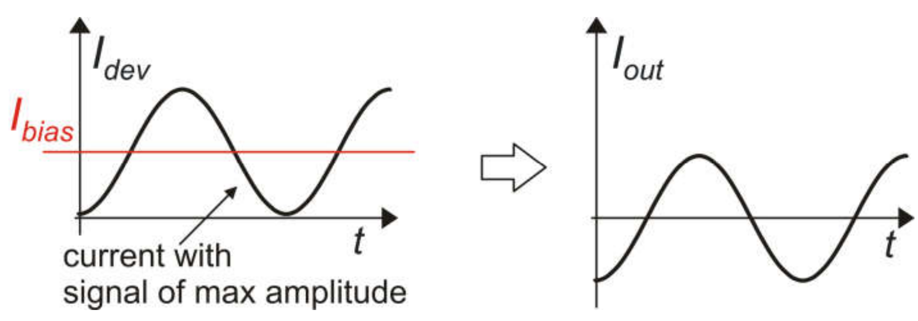

Fig.3 Current in the output device of a class-A stage in the presence of the maximum allowed signal amplitude (left). Output current after subtraction of the DC component (I_{bias}).

1.2 Source-follower output stages

If the output quantity is a voltage, a low output resistance is desirable, in order to reduce attenuation of the output voltage caused by the load. A typical stage featuring a low output resistance is the source follower (emitter follower in BJT circuits), shown in Fig.4 (a) and (b) as an *n*-MOS and *p*-MOS stage, respectively.

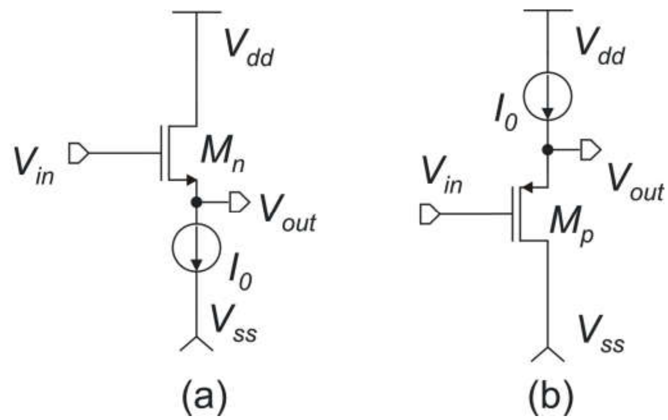

Fig.4 Class-A, source-follower output stages

These stages exhibit an output resistance equal to $1/g_m$, which is the smallest that can be obtained with a single-transistor circuit. They have been very popular when supply voltages of several Volts or even tens of Volts for analog circuits were available for analog circuits. With the continuous reduction of the supply voltage, source follower stages have been progressively ruled out.
To understand this, let us write the in-out characteristic of the stages in Fig.4:

$$\begin{array}{ll} V_{out} = V_{in} - V_{GSn} & (\mathrm{n-stage}) \\ V_{out} = V_{in} + |V_{GSp}| & (\mathrm{p-stage}) \end{array} \tag{3}$$

Since V_{in} must be provided by a preceding stage that shares the same supply voltages as the output stages, then:

$$V_{ss} < V_{in} < V_{dd} \tag{4}$$

Substituting these inequalities into (3), we find the following limitations:

$$\begin{array}{ll} V_{out} < V_{dd} - V_{GSn} \cong V_{dd} - \left(V_{tn} + \sqrt{\dfrac{2I_D}{\beta}} \right) & (\mathrm{n-stage}) \\ V_{out} > V_{ss} + |V_{GSp}| \cong V_{dd} - \left(|V_{tp}| + \sqrt{\dfrac{2I_D}{\beta}} \right) & (\mathrm{p-stage}) \end{array} \tag{5}$$

Therefore:

a) the *n*-stage margin to V_{dd} is V_{GSn};
b) the *p*-stage margin to V_{ss} is $|V_{GSp}|$.

The V_{GS} includes a threshold voltage, which generally is no lower than 0.5 V. In addition, in a standard n-well CMOS process, the source and body of the *n*-MOSFETs cannot be connected together, so that, for the n-stage, V_t is significantly increased by the body effect. As (5) shows, the margin also increases at high output currents, where I_D is large. This occurs at positive output currents for the *n*-stage, negative ones for the *p*-stage.
In conclusion, using a source follower stage, we should expect to lose a margin of roughly 1 V from one of the two rails. With a 3.3 single supply voltage, which is very common in today's analog circuits, this means giving away 30 % of the available output swing. In most cases, this is not acceptable.

In terms of type of operation, both circuits in Fig.3 are class-A stages. We have a single active device (M_n or M_p) that is driven by the input signal. The bias current I_0 sets the maximum negative current for the *n*-stage and the positive one for the *p*-stage.

An example of class-AB source follower stage is shown in Fig.5. In this circuit, the maximum negative and positive output current is determined by the size (aspect ratio) of the output devices (M_n or M_p), while the output bias current, flowing in quiescent condition is given by:

$$I_{bias} = \frac{\beta_n}{\beta_{Bn}} I_0 = \frac{\beta_p}{\beta_{Bp}} I_0 \tag{6}$$

The bias current can be freely set to a value much smaller than the maximum output current, improving power efficiency and quiescent power consumption with respect to class-A stages.

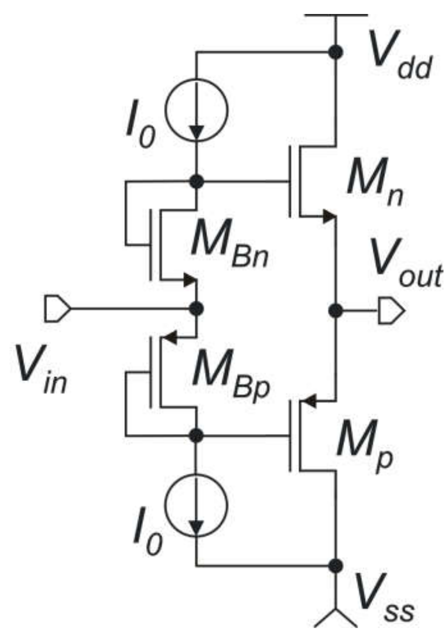

Fig.5 Class-AB source-follower output stage

Unfortunately, in terms output voltage swing, the stage in Fig. 5 loses a V_{GS} from both rails. This characteristic makes this stage completely unsuitable for moderate-to-low supply voltages.

1.3 How to deal with a high output resistance in op-amp output stages.

Source followers (and similarly emitter follower in bipolar circuits) have the advantage of a low output resistance but, as we have seen, are not suitable for low voltage applications. As we will see, the most commonly used stages todays are common source configurations, which are marked by an output resistance of the order of r_d, which, for similar bias conditions, is much higher than $1/g_m$. When the output stage is part of an amplifier to be used in closed loop configuration, this limitation may be not critical. To understand this, see Fig. 6, showing an amplifier with its output resistance, a feedback network and a load resistor. The amplifier gain measured with open output termination (no load and no feedback network) is indicated with A_{OT}.

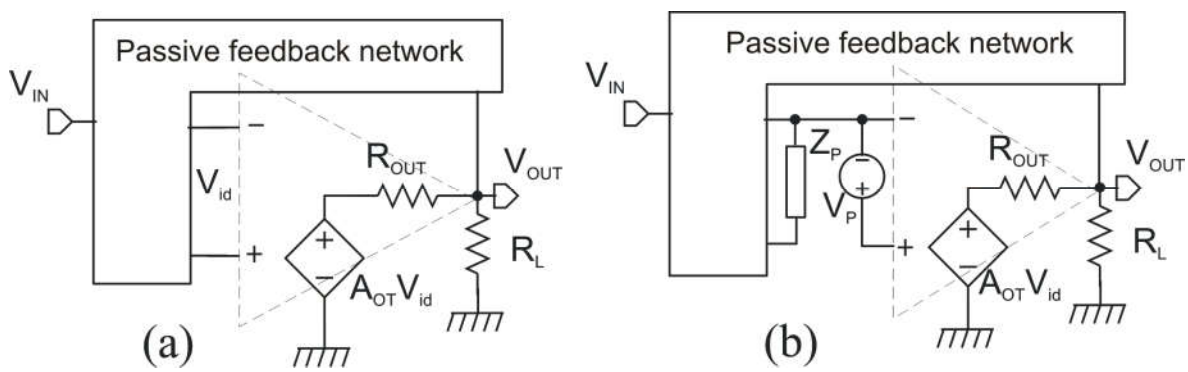

Fig.6 General closed loop configuration (a) and circuit obtained applying the cut-insertion theorem (b).

The target in a closed loop circuit is obtaining a transfer function that does not depend on the amplifier characteristics and is only determined by the transfer functions of the passive feedback network. This is guaranteed by an high enough loop gain β*A*, which can be calculated applying the cut shown in Fig.6(b) and using the cut-insertion theorem. Since generally $|\beta| \leq 1$, in order to have $|\beta A|>>1$ it is required that $|A|>>1$. Parameter *A*, is given by:

$$A = \left.\frac{v_{out}}{v_p}\right|_{v_{in}=0} = A_{OT}\frac{R_L // R_F}{R_L // R_F + R_{out}} = A_{OT}\frac{1}{1+\dfrac{R_{out}}{R_L // R_F}} \tag{7}$$

where R_F is the resistance seen by the amplifier output terminal towards the feedback network (loading effect of the feedback network).

Equation (7) shows that if $R_{out}>>R_L//R_F$, the actual gain A can be much lower than the open terminal gain A_{OT}. However, if $|\beta A|$ is still >> 1, this does not represent a problem and the closed loop amplifier still behaves correctly. Clearly, this condition should be checked anytime a closed loop circuit is designed, but the conclusion is that it is possible to use output stages with relatively high output resistances as far as the loop gain is still much greater than unity. Note that, even if a resistive load (R_L) is absent, a resistive feedback network (such as the one used in inverting and non-inverting op-amp based amplifiers) may constitute a significant load for the output stage. This point should be carefully addressed when designing feedback circuits.

1.3 Common source output stages.

A class-A output stage based on a common-source configuration is shown in Fig.7. For the sake of simplicity, we will analyze only the *n*-type stage. The same considerations apply to the *p*-stage.
On the left, the stage is depicted with an idealized bias current source, while, on the right, the current source is replaced by the typical implementation based on a single *p*-MOS device with constant gate-source voltage ($|V_{GSp}|=V_{dd}-V_k=constant$).

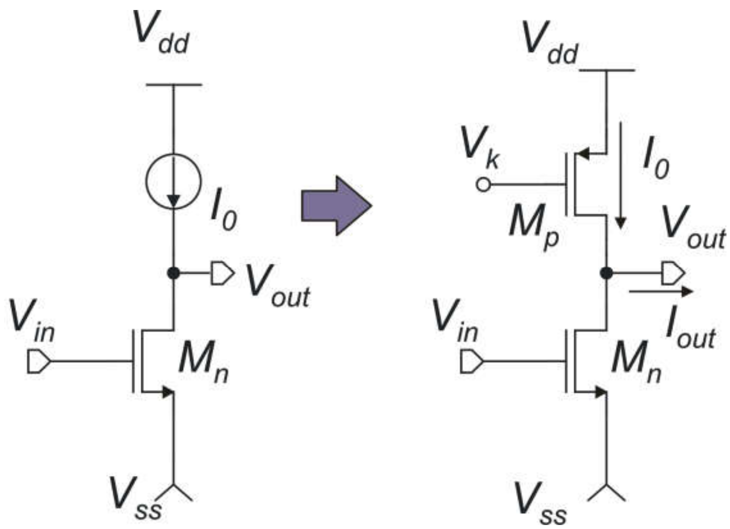

Fig.7. Common source class-A output (gain) stage with idealized bias current source (left) and p-MOS bias current source (right).

The typical inverter-like transfer characteristic of this stage, obtained in condition of zero load, is shown in Fig.8. Note that, in terms of output voltage, the linear region extends from $V_{dd}-|V_{DSATp}|$ to $V_{ss}+V_{DSATn}$. The margin to both rails is then limited to only one saturation voltage.

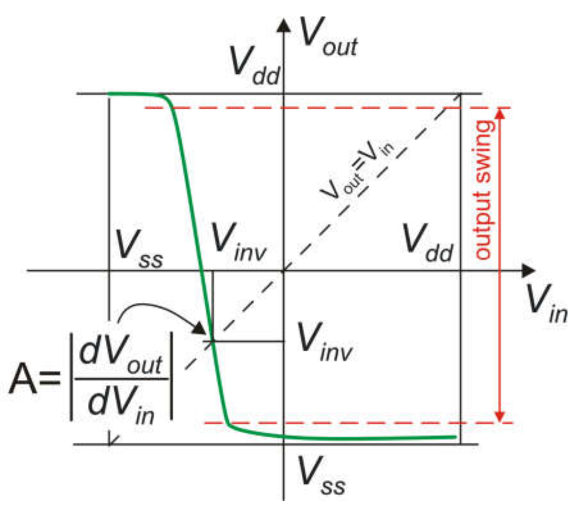

Fig.8. Common source class-A output (gain) stage with idealized bias current source (left) and *p*-MOS bias current source (right)

It is important to observe that, differently from the source-follower stage, the common source is marked by a negative gain (it is an inverting stage), whose absolute value is given by:

$$A = \left| \frac{dV_{out}}{dV_{in}} \right| = g_{mn}(r_{dn} // r_{dp}) \tag{8}$$

The output resistance is given by $r_{dn}//r_{dp}$, and strongly depend on the bias current. This resistance is considerably higher than the one exhibited by a source follower with identical bias current, although, as we have seen, this can be tolerated in amplifiers designed to work in closed loop configuration.

It is possible to find a useful equivalent circuit of the amplifier, by introducing voltage V_{inv} , at which the transfer characteristic crosses the $V_{out}=V_{in}$ straight-line. The equivalent circuit is presented in Fig.9 (a), where "A" is an ideal differential amplifier with gain $=A$.

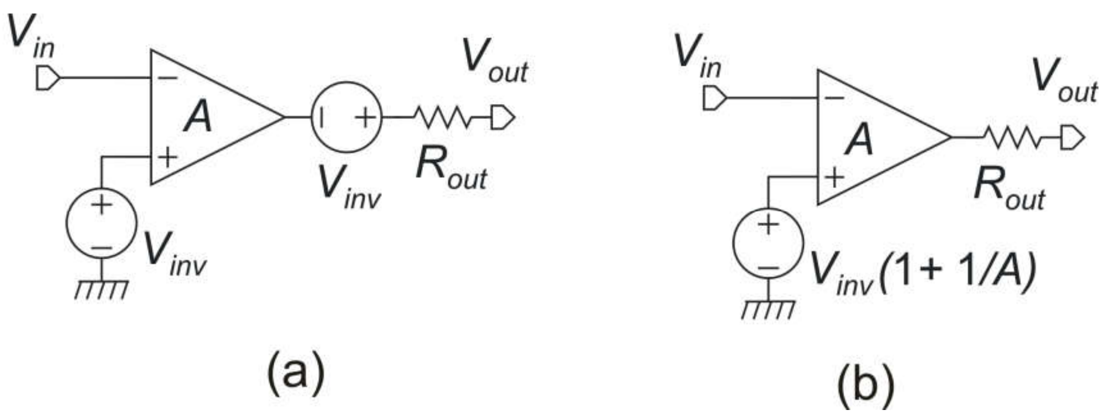

Fig.9. Equivalent circuit of an inverting single/input – single/output stage like that of Fig.7.

Note that the equivalent circuit and the real circuit in fig.7 share the following properties:

1) when $V_{in}=V_{inv}$ the output of the ideal amplifier is zero and V_{out} is then equal to V_{in}
2) for small signals the gain is negative and its absolute value is A.
3) the output resistance is R_{out}.

The V_{in} source placed at the amplifier output in Fig.9(a) can be referred to the input, obtaining the equivalent circuit shown in Fig.9(b). This equivalent circuit can be useful when single inverting stages are used to replace operational amplifiers in switched capacitor circuits, where the non-inverting terminals is generally unused (i.e. tied to a constant potential).

In terms of class, the stage in Fig.7 operate in class-A. The maximum positive output current is produced when M_n completely turns off and the whole bias current I_0 flows is routed to the load. Again, we note that the maximum output current is equal to the current adsorbed in rest condition. This is acceptable if the stage is required to deliver small currents, typically of the order of a few tens of μA. For higher currents, it is convenient to use a class-AB stage.

Common source, class-AB stages are generally based on the simplified circuit of Fig.10. The circuit is similar to that of Fig.7, but here the input signal is also applied to the p-MOS. The result is that M_p does not work as a constant current source, but its current can get much higher than the quiescent value.

In this way, the maximum output current depends only on the maximum V_{GS} that the driver stage signal can apply to M_n (negative currents) and M_p (positive currents), and, obviously on the size of M_p and M_n. The battery V_B splits the gate voltages of M_n and M_p, indicated with V_{Gn} and V_{Gp}, respectively. Its function is controlling the quiescent bias current of the output devices. Obviously, the circuit of Fig.10 is greatly simplified. The battery is generally implemented with a voltage shifter or with other more complicated circuits. In many cases, the driver stage produces the voltages V_{Gp} and V_{Gn} properly separated by a voltage V_B.

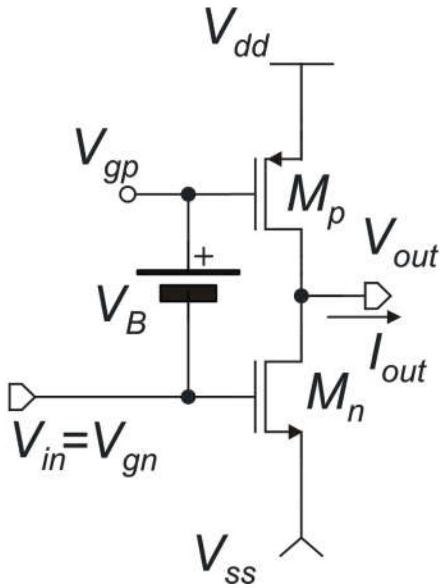

Fig.10.Principle of operation of class-AB, common source output stages.

Design of this stage greatly depends on the type of driver stage. As a general consideration, we can say that the size of M_n and M_p are determined by the desired maximum negative and positive currents, respectively, taking into accounts also the actual excursion of V_{Gn} and V_{Gp}, and then the maximum V_{GSn} and V_{GSp} that the driver can apply. It is beyond the aim of this document to get further into these arguments. We will assume that the aspect ratios of M_n and M_p, and then β_n and β_p are assigned.
At this point, we have to set the quiescent current. To do so, consider the diagram in Fig.11.

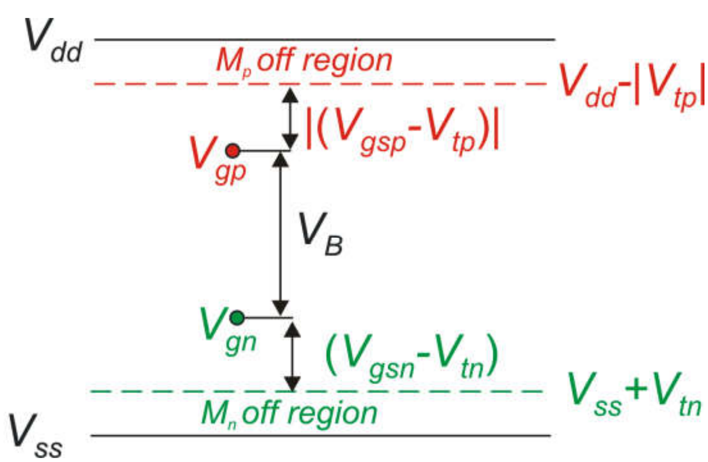

Fig.11.Relevant voltage levels for V_{Gn} and V_{Gp} and role of V_B.

There are two peculiar voltage levels:

-) $V_{ss}+V_{tn}$: when V_{Gn} falls below this level, M_n turns off; the distance of V_{Gn} from this level is M_n overdrive voltage (i.e. its V_{GS}-V_t); therefore, the larger is the distance of V_{Gn} from this level, the higher is M_n drain current.
-) V_{dd}-$|V_{tp}|$: when V_{Gp} rises over this level, M_p turns off; the distance of V_{Gp} from this level is M_p overdrive voltage (i.e. its $|V_{GS}$-$V_t|$); therefore, the larger is the distance of V_{Gp} from this level, the higher is M_p drain current.

We start by setting V_{Gn} quiescent value in such a way that I_{Dn} is equal to the desired quiescent bias current. Since, in quiescent condition, no current should be delivered to the load, that is $I_{Dn}=|I_{Dp}|$, the we have to set V_{Gp} quiescent value is such a way that I_{Dp} is equal to the target bias current. At this point, we have fixed both V_{Gn} and V_{Gp} and their distance is the required voltage shift V_B, ideally produced by the battery.
When a large signal is applied, V_{Gn} and V_{Gp} experience large variations, as shown in Fig.12, but their difference remain equal to V_B. If the input voltages decreases, then M_n overdrive voltage decreases, while M_p one increases. Then I_{Dp} gets higher than I_{Dn} and a positive current is sourced to the load, increasing also the output voltage. When V_{in} increases, the opposite situation occurs and I_{Dn} gets higher than I_{Dp}, so that a negative current is fed to the load. The V_{out} vs. V_{in} characteristic is clearly inverting as in the stages of Fig.7. When the input signal variation is negative and large enough that V_{Gn} drops below the $V_{ss}+V_{tn}$ level, than M_n turns off and M_p alone drives the load (light blue area in Fig.12). Conversely, for large positive V_{in} variations, V_{Gp} rises over the V_{dd}-$|V_{tp}|$ level (light violet area in Fig.12), Mp turns off, and Mn alone drives the load. This alternation of Mn and Mp operation and the fact that for small input voltages both devices are on, proves that the circuit implements class-AB.
When only Mp , in its on phase, "pushes" a current into the load, while Mn "pulls" a current from the load, this kind of stage is indicated as "push-pull".

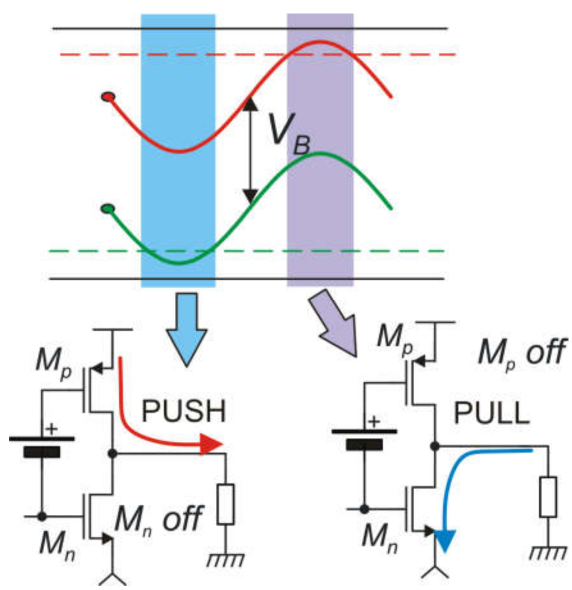

Fig.12. Behavior of the class-AB common source output stage in the presence of large signals. .

The small signal behaviour of the circuit can be modelled with the equivalent circuit of Fig. 13, where gates G_p and G_n coincides, since the battery V_B is a short circuit for variations.

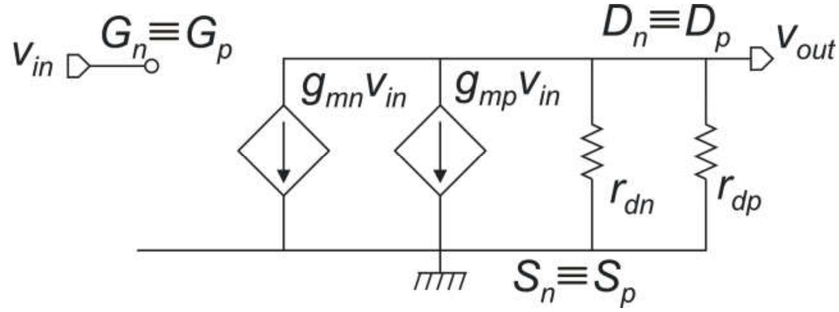

Fig.13. Small signal equivalent circuit of the class-AB common source stage.

The small signal gain is simply given by:

$$\frac{v_{out}}{v_{in}} = -\left(g_{mn} + g_{mp}\right)\left(r_{dn} // r_{dp}\right) \tag{9}$$

The simpler implementation of the circuit in Fig.10 is shown in Fig.14, where a *p*-type source follower (M_S device), biased current I_{BS} is used to operate the voltage shift and obtain correct drive of V_{Gp}. Note that the battery voltage V_B is the absolute voltage of M_S gate-source voltage (V_{GS}.)

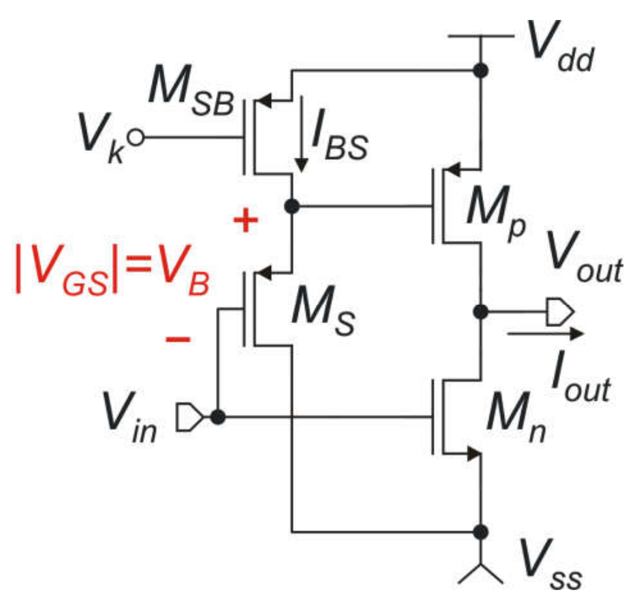

Fig.14. Small signal equivalent circuit of the class-AB common source stage.

The stage in Fig.14 has an inverting characteristic with a small signal gain given by (9), and accepts the same schematization given by the equivalent circuits of Fig. 9, proposed for the class-A stage. Similarly to the class-A version, the common source class-AB stage exhibit an output swing that extend across the two rails, V_{dd} and V_{ss}, with a margin given by one saturation voltage from both sides. The output resistance is again $r_{dn}//r_{dp}$ and, as such, is proportional to the inverse of the quiescent current. The latter determine also the values of Mn and Mp g_m's, which, in turn, affect the speed

1.4 Simple operational amplifier topologies

Figure 15 shows the architecture of a simple two-stage operational amplifier. The first stage is a *p*-input differential amplifier. The second stage is an *n*-input class-A common source output stage. Both stages are biased by M_7 and M_6, that operate as current sources controlled by the input bias current applied to M_8 (I_{bias}).
The overall small signal gain, A_{OT}, is the product of the gain of the two stages. Considering that no load is applied to the output stage (open output port), we simply get:

$$A_{OT} = \frac{v_{out}}{v_d} = g_{m1}(r_{d2} // r_{d4}) g_{m5}(r_{d5} // r_{d6}) \tag{10}$$

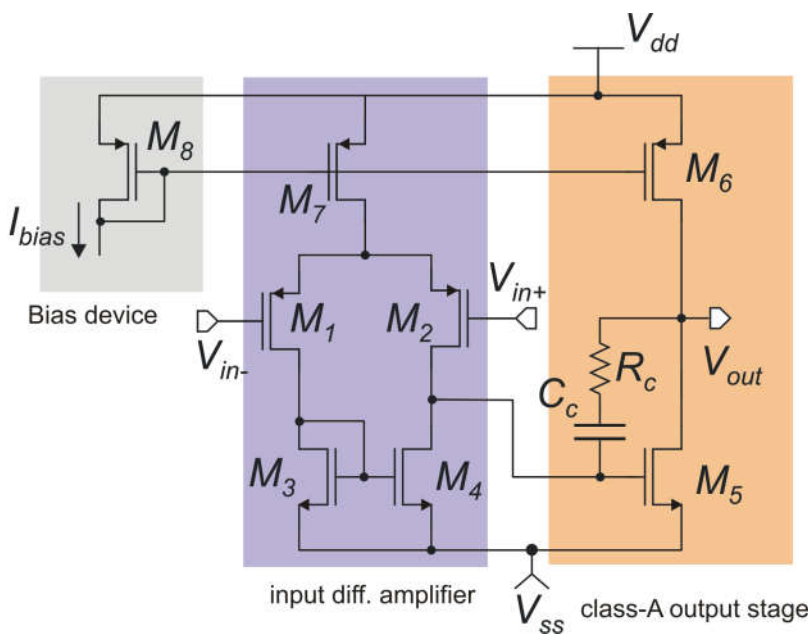

Fig.15. Simple two-stage op-amp with class-A output stage.

Just to have an idea of the gain that can be obtained with this stage, we can consider that all g_m's and r_d's are equal, so we get:

$$A_{OT} \approx \frac{(g_m r_d)^2}{4} \tag{11}$$

Since the $g_m r_d$ product can reach values of a few hundreds, Eq. (11) indicates that it is possible to obtain gains of the order of 10^4 (80 dB).

An important aspect that has to be considered is that the quiescent output voltage of the first stage determine the quiescent point of the second one. The target is obtaining a zero output short circuit current in rest conditions, i.e. with a differential input voltage equal to zero. Then, in rest conditions, the current in M5 should match the constant bias current produced by M6, and this should occur for every supply voltage. Note that the input voltage of the output stage is measured with respect to V_{ss} , since $V_{GS5}=V_{in}-V_{ss}$. In other words, we say that V_{in} "is referred" to V_{ss}. Therefore, the first stage should produce an output voltage that is also referred to Vss. The *p*-input stage used in the amplifier of Fig.15 produces a quiescent output voltage that, for symmetry reasons, is given by: $V_{ss}+V_{GS3}$. Therefore, the effective input of the second stage is V_{GS3}. If we had used an n-type input differential stage, then the output would have been referred to V_{dd}, being equal to $V_{dd}-|V_{GS}|$. In these conditions, the input of the second stage (i.e. V_{GS5}), would have been equal to $V_{dd}-V_{ss}-|V_{gs}|$, so that the current in M_5 would have been strongly dependent on the effective power supply ($V_{dd}-V_{ss}$). This is not acceptable, since the matching between I_{D6} (constant) and I_{D5} (dependent on the supply voltage) could hold true only for a particular value of the supply voltage, making the stage practically unusable. Therefore, only two combinations are possible.

a) *p*-input stage / *n*-output stage (the case of Fig.15).
b) *n*-input stage / *p*-output stage (dual case)

The only important difference between the two options is the input common mode voltage range, which for the *p*-input stage extends down to V_{ss} , while for the *n*-input stage reaches V_{dd}.
The group C_C-R_C performs Miller compensation, which is necessary for two stage amplifiers to achieve closed loop stability.

Finally, a simple two stage operational amplifier using the class-AB output stage of Fig. 14, is shown in Fig. 16. The series of three diode-connected mosfets ($M_{20\text{-}22}$), indicated as bias chain, produces a bias current that depends on the supply voltage. Regardless of the value of I_{bias}, it is possible to properly choose the mosfet aspect ratio in such a way that, in rest conditions:

$$V_{GS20} = V_{GS3} \quad (= V_{GS5}) \;\; ; \;\; \text{and} \;\; V_{GS21} = V_{GS10} \tag{12}$$

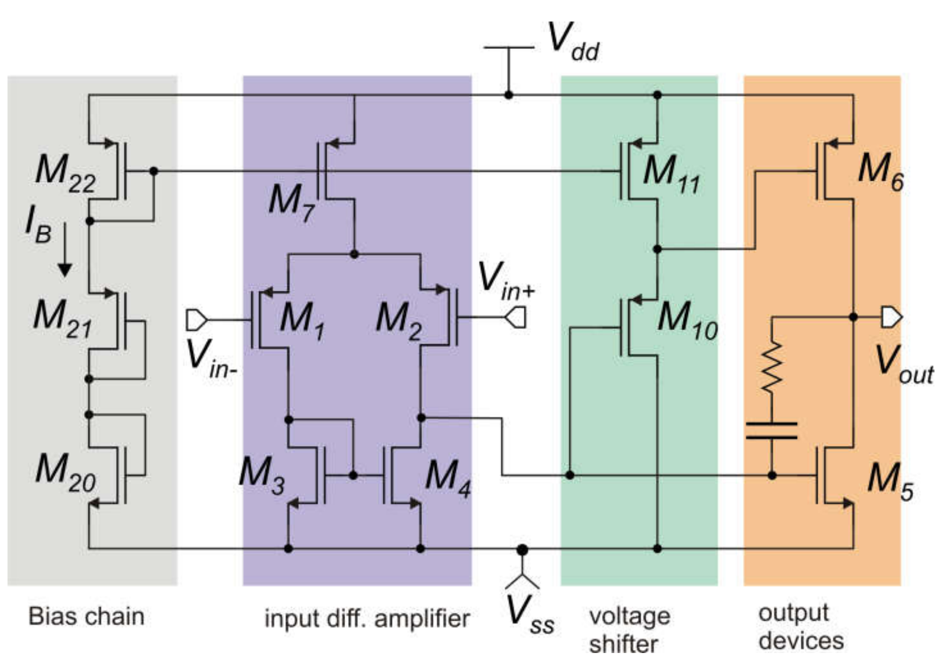

Fig.16. Simple two-stage op-amp with class-AB output stage.

In this way, we get the following result: $V_{GS6}=V_{GS22}$. Currents in the output mosfets are then simply equal to:

$$I_{D5}=\frac{\beta_5}{\beta_{20}}I_{bias};\quad I_{D6}=\frac{\beta_6}{\beta_{22}}I_{bias} \tag{13}$$

Choosing the aspect ratios in order to make $\beta_5/\beta_{20}=\beta_6/\beta_{22}$, drain currents in M_6 and M_5 match, thus the output short circuit current is close to zero in rest conditions at any supply voltages. Note that, to obtain this indispensable property, the battery voltage of the output class-AB stage ($V_B=|V_{GS10}|$) increases at higher supply voltage (adaptive voltage shift), due to variation of $I_{D11}=I_{D10}$, which is proportional to I_{bias}.

The major drawback of this stage is that a minimum $V_{dd}-V_{ss}$ supply voltages equal to three V_{GS} ($V_{GS20}+|V_{GS21}|+|V_{GS22}|$) is required. With typical threshold voltages, the minimum supply voltage is of the order of 2 V. As a comparison, the class-A stage shown in Fig.15 requires only a supply voltage greater than one V_{GS} and two V_{DSAT}, and thus it is suitable for very low voltage operation (down to b supply voltages lower than 1 V).