1 Fully differential amplifiers: transistor level perspective.

1.1 A fully differential operational amplifier based on the folded cascode topology.

Circuit description and analysis

Operational amplifiers based on a single folded cascode amplifier are suitable to be used in most switched capacitors applications, where only capacitive loads are present. On the other hand, they are not appropriate when resistive loads (or resistive feedback networks) have to be used, since their output resistance is very high and a resistive load, even in the hundreds of kΩ range would cause the gain to drop to low values. Nevertheless, since switched capacitor circuits represent a large fraction of the fully differential circuits being currently developed, it is important to study the single-stage, folded cascode fully differential amplifier. The typical topology [1] is shown in Fig.1.1.

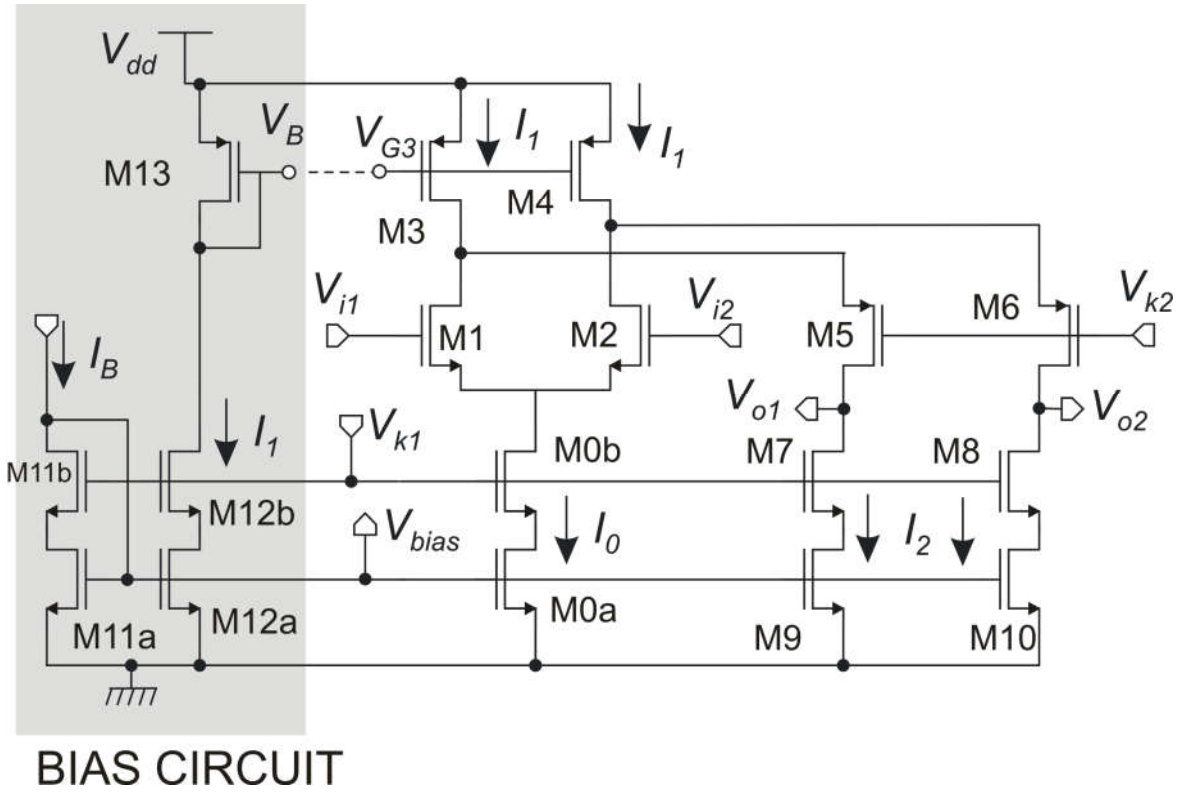

Fig.1.1. Folded-cascode fully differential operational amplifier

The bias circuit is formed by a precise wide swing cascode mirror (see Chap. 3.1), whose input section is made up by M11a and M11b. The bias current I_B is mirrored into the currents I_0, I_1 and I_2. Current I_1 is fed to M13. The gate of M13 (node V_B) can be connected to M3, M4 gates (node V_{G3}) so that current I_1 is mirrored into M3 and M4. We will show later that this is not a correct biasing option, but let now start by assuming that V_B and V_{G3} are connected together (dashed line in Fig.1.1). *Vk1* and *Vk2* are

constant voltages used to bias the wide swing current mirror and the common gate stage (M5, M6), respectively.

In order to study this amplifier, the generalized Norton equivalent circuit (see App. 3.4) of both outputs will be derived as shown in Fig.1.2. We probe the output ports with a voltage source equal to V_{CMO}, where V_{CMO} is the output common mode voltage that the amplifier must assume, by specification. The resulting circuit, shown on the right in Fig.1.2, can be further simplified, assuming that the output resistances R_{out1} and R_{out2} are equal.

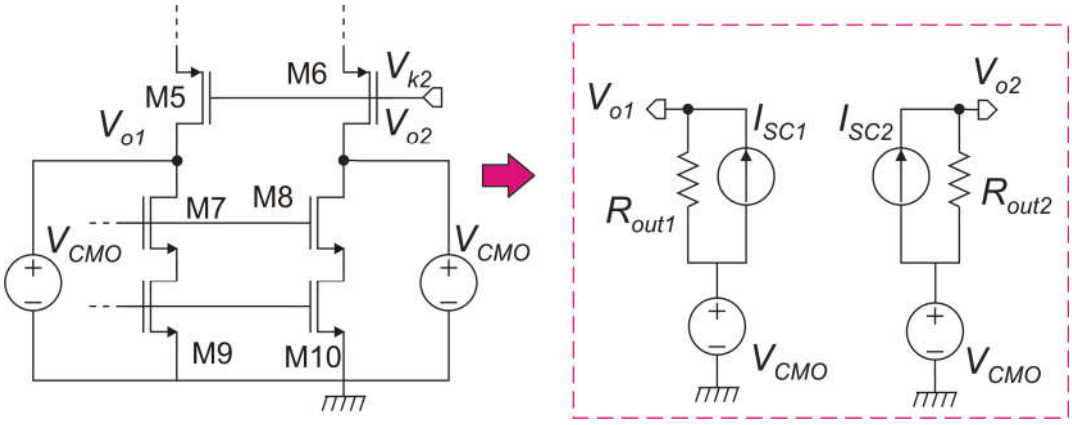

Fig.1.2. Derivation of the generalized Norton equivalent circuit of the amplifier output ports.

The simplified circuit is shown in Fig.1.3. Having set R_{ou1} equal to R_{out2}, corresponding to neglecting output resistance mismatch, greatly simplifies calculations. For an analysis that does not make this assumption, see App.3.6.

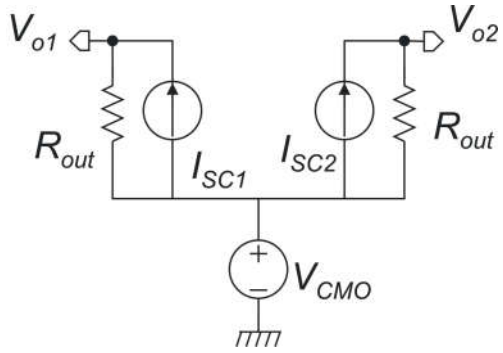

Fig.1.3. Simplified output equivalent circuit

By simple consideration, the output resistance in the nominal case is given by

$$R_{out} = R_{CN} \| R_{CP} \tag{1.1}$$

where R_{CN} is the output resistance of the cascode mirror providing bias current I_2 (M7,M9 and M8,M10 current mirrors), while R_{CP} is the resistance seen from the drain of the common gates (M5 and M6). Performing small signal analysis to M5 (M6 is symmetrical), we note that M5 source is connected to ground by the parallel of the resistances seen towards the drain of M3 and M1, corresponding to r_{d3} and $2r_{d1}$, respectively. Therefore, the resistance seen from M5 source and *gnd* is of the same order as r_d and resistance R_{CP} is of the same order as the output resistance of a cascode mirror.

As a result, due to (1.1), the output resistance R_{out} is also of the same order of magnitude as the output resistance of a cascode mirror, i.e. of $r_d(g_m r_d)$.

By simple considerations, the output short circuit currents I_{SC1} and I_{SC2} are given by:

$$\begin{cases} I_{SC1} = I_1 - I_{D1} - I_2 \quad = \quad I_1 - \left(\dfrac{I_0}{2} + g_{m1} \dfrac{v_{id}}{2} \right) - I_2 \\ I_{SC1} = I_1 - I_{D2} - I_2 \quad = \quad I_1 - \left(\dfrac{I_0}{2} - g_{m1} \dfrac{v_{id}}{2} \right) - I_2 \end{cases} \tag{1.2}$$

Currents I_1, I_2 and I_0 are all derived by the same bias current I_B, thus we can nominally write:

$$\begin{cases} I_0 = k_0 I_B \\ I_1 = k_1 I_B \\ I_2 = k_2 I_B \end{cases} \tag{1.3}$$

where k_0, k_1, k_2 are the nominal current gains of the mirrors. Since all individual mirrors are affected by systematic errors (e.g. due to the effect of the r_d's) and random errors (due to matching errors), we can rewrite equations (1.2) as:

$$\begin{cases} I_{SC1} = k_1 I_B - \dfrac{k_0 I_B}{2} - k_2 I_B - g_{m1} \dfrac{v_{id}}{2} \; + \; I_{\varepsilon 1} \\ I_{SC2} = k_1 I_B - \dfrac{k_0 I_B}{2} - k_2 I_B + g_{m1} \dfrac{v_{id}}{2} \; + \; I_{\varepsilon 2} \end{cases} \tag{1.4}$$

where $I_{\varepsilon 1}$ and $I_{\varepsilon 2}$ are error currents that represent the sum of the errors of each single current mirror. Note that different current sources contribute to I_{SC1} and I_{SC2}. For example, current I_2 is provided by M7,M9 for I_{SC1} and by M8-M10 for I_{SC2}. Matching errors between these sources cause $I_{\varepsilon 1}$ and $I_{\varepsilon 2}$ to be different. Furthermore, due to matching errors between M1 and M2, I_{D1} and I_{D2} are not identical and equal to $I_0/2$ when $V_{id}=0$. This also contributes to make $I_{\varepsilon 1}$ and $I_{\varepsilon 2}$ different.

Now, let us split $I_{\varepsilon 1}$ and $I_{\varepsilon 2}$ into a common mode component (I_ε) and a differential component (ΔI_ε) as:

$$\begin{cases} I_{\varepsilon 1} = I_\varepsilon + \dfrac{\Delta I_\varepsilon}{2} \\ I_{\varepsilon 2} = I_\varepsilon - \dfrac{\Delta I_\varepsilon}{2} \end{cases} \tag{1.5}$$

With a simple transformation, we can refer the differential component to the input offset voltage V_{io}, with:

$$\Delta I_{\varepsilon} = g_{m1} V_{io} \tag{1.6}$$

Using (1.5) and (1.6), Eqns. (1.4) can be re-written as:

$$\begin{cases} I_{SC1} = k_1 I_B - \dfrac{k_0 I_B}{2} - k_2 I_B - \dfrac{g_{m1}}{2}\left(v_{id} - v_{io}\right) + I_{\varepsilon} \\ I_{SC2} = k_1 I_B - \dfrac{k_0 I_B}{2} - k_2 I_B + \dfrac{g_{m1}}{2}\left(v_{id} - v_{io}\right) + I_{\varepsilon} \end{cases} \tag{1.7}$$

Considering the equivalent circuit of Fig.1.3, the output voltages V_{o1} and V_{o2} can be written as:

$$\begin{cases} V_{o1} = V_{CMO} + R_{out} I_{SC1} \\ V_{o2} = V_{CMO} + R_{out} I_{SC2} \end{cases} \tag{1.8}$$

The output differential voltage V_{od} and the output common mode voltage V_{oc} are then given by:

$$V_{od} = V_{o2} - V_{o1} = \; R_{out}\left(I_{SC2} - I_{SC1}\right) \; = \; g_{m1} R_{out}\left(v_{id} - v_{io}\right) \tag{1.9}$$

$$V_{oc} = \frac{V_{o2} + V_{o1}}{2} = V_{CMO} + R_{out}\left(\frac{I_{SC2} + I_{SC1}}{2}\right) = V_{CMO} + R_{out}\left(k_1 I_B - \frac{k_0}{2} I_B - k_2 I_B\right) + R_{out} I_{\varepsilon} \tag{1.10}$$

Equation (1.9) indicates that the differential-to-differential mode gain Add (i.e. the amplifier gain), is given by:

$$A_{dd} = g_{m1} R_{out} \tag{1.11}$$

and that the offset voltage v_{io} defined in (1.6) is actually the total input offset voltage of the amplifier. Since R_{out} is of the order of $r_d(g_m r_d)$., the total gain of this amplifier is of the order of $(g_m r_d)^2$. Then, gains up to 10^4 (80 dB) can be obtained with the topology of Fig.1.1.

Now, let us consider the output common mode voltage, given by (1.10). By design, it is possible to choose the current gains k_0, k_1, k_2 such that:

$$k_1 - \frac{k_0}{2} - k_2 = 0 \tag{1.12}$$

This guarantees that, in the nominal case, where $I_{\varepsilon 1}$ and $I_{\varepsilon 2}$ are zero, the output short circuit currents I_{SC1} and I_{SC2} are also zero. As a result, in the nominal case, $V_{oc}=V_{CMO}$. Unfortunately, due to the presence of systematic and random errors, we have to take into account the presence of the error current I_{ε}. From (1.10) and (1.12) we get:

$$V_{oc} = V_{CMO} + R_{out} I_{\varepsilon} \tag{1.13}$$

The error current I_ε is generally a small fraction (e.g. 1 %) of the amplifier quiescent currents (I_1, I_0, I_2). However, due to the high value of the output resistance R_{out}, even a small error current is sufficient to produce very large differences between V_{oc} and the target value V_{CMO}. In order to give a quantitative estimation of the error, R_{out} can be substituted by its expression derived from (1.11):

$$V_{oc} - V_{CMO} = R_{out} I_{\varepsilon} = \frac{A_{dd}}{g_{m1}} I_{\varepsilon} = V_{TE1} A_{dd} \frac{I_{\varepsilon}}{I_{D1}} = 2 V_{TE1} A_{dd} \frac{I_{\varepsilon}}{I_0} \tag{1.14}$$

Since I_ε is a small fraction of the bias currents (it derives from matching errors), then the ratio I_ε / I_0 is of the order of 10^{-2}. With a gain A_{dd} in the range 10^3-10^4 (typical for this kind of topologies), and choosing V_{TE}=100 mV, we find an error $|V_{oc}$-$V_{CMO}|$ in the range 2-20 V. Such an error is so large that the output common mode voltage may exceed the power supply rails, i.e. it can be greater than V_{dd} or less than zero. This cannot occur, but it is a clear indication that the output voltages V_{o1} and V_{o2} are both saturated to the minimum or maximum limit of the output voltage range, implying that some devices are in triode region. The situation in the case that both output voltages are saturated to the upper limit of the output swing is depicted in Fig.1.4. This occurs when the output common mode voltage V_{oc} is much higher than the target value V_{CMO}, which should be set to the middle of the output range. Applying a differential voltage, eventually puts one of the output voltages out of saturation, but pushes the other one even further into saturation. For this reason, it not possible to find an interval of input voltages where both outputs are in the linear region.

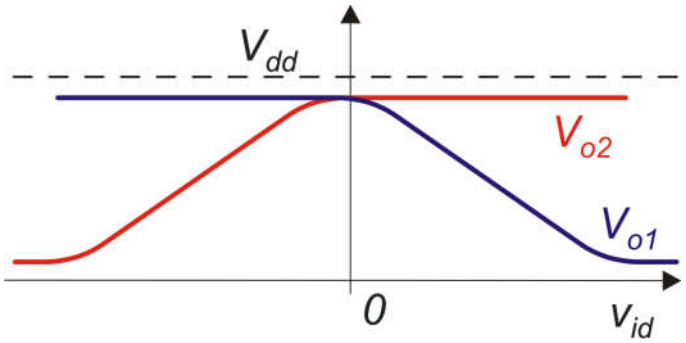

Fig.1.4. Dependence of the output voltages on the input differential voltage in the case that both outputs are saturated high, i.e. the output common mode voltage is close to the upper limit of the output swing.

The ideal situation is depicted in Fig.1.5 (left), where the both the output voltages coincides with the middle of the output range for v_{id}=0 and then show symmetrical linear dependences on v_{id} when the latter is within the input differential range. The behavior shown in Fig.1.5 (left) represents the particular case of null input offset voltage. The more realistic case of non-zero offset voltage is shown in Fig.1.5 (right). This is a perfectly acceptable case, since an input voltage interval in which the output voltages behaves in a symmetrical linear way is still present.

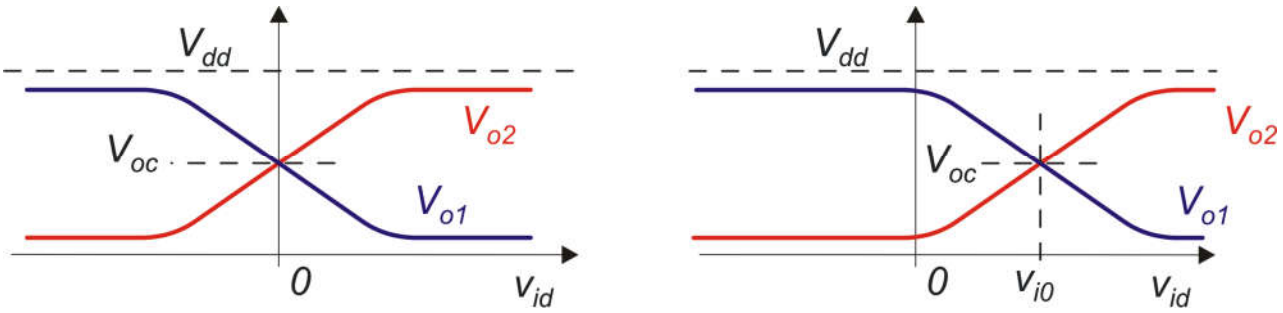

Fig.1.5. Dependence of the output voltages on the input differential voltage in the case of correct output common mode voltage: zero offset voltage (left) , non-zero offset voltage (right).

Output common mode stabilization: the Common Mode Feedback (CMFB) method.

In order to obtain the correct operating conditions shown in Fig.1.5, it is necessary to control the output common mode voltage (V_{oc}) and set it the correct value (V_{CMO}). The most effective approaches uses negative feedback to form a so-called Common Mode FeedBack circuit (CMFB). This consists in modifying one the main bias currents I_0, I_1, I_2 in such a way to introduce a term proportional to the error (V_{oc}–V_{CMO}). We will choose to modify I_1, but the other cases (i.e. when I_0 or I_2 are involved) are quite similar. Generally, it is not desirable to act on I_0, since this current directly biases the input differential pairs and then affects the input transconductance (g_{m1}).

According to this approach, current I_1 is no more constant but is given by:

$$I_1 = k_1 I_B - g_m^* (V_{oc} - V_{CMO}) \tag{1.15}$$

where g_m* is a transconductance factor. To do this, it is not possible to connect V_B to V_{G3} in the circuit of Fig.1.1, i.e. the connection represented by the dashed line should not be done. Two different methods to make I_1 follow Eqn. (1.15) will be explained later. Now, let us see how Eqn. (1.15) results in a precise control of the output common mode voltage.

Following the same steps from (1.3) to (1.7), with the sole difference that I_1 is given by (1.15), equations (1.7) becomes:

$$\begin{cases} I_{SC1} = k_1 I_B - g_m^* (V_{oc} - V_{CMO}) - \dfrac{k_0 I_B}{2} - k_2 I_B - \dfrac{g_{m1}}{2}(v_{id} - v_{io}) + I_\varepsilon \\ I_{SC2} = k_1 I_B - g_m^* (V_{oc} - V_{CMO}) - \dfrac{k_0 I_B}{2} - k_2 I_B + \dfrac{g_{m1}}{2}(v_{id} - v_{io}) + I_\varepsilon \end{cases} \tag{1.16}$$

Using these expressions in (1.9) and (1.10) we obtain that the differential mode is not changed, while the expression of the common mode voltage becomes:

$$V_{oc} = V_{CMO} + R_{out}\left(k_1 I_B - \frac{k_0}{2} I_B - k_2 I_B\right) + R_{out} I_\varepsilon - g_m^* R_{out}(V_{oc} - V_{CMO}) \tag{1.17}$$

Again, choosing all the current gains in such a way that (1.12) is respected, we obtain:

$$V_{oc} = V_{CMO} + R_{out} I_{\varepsilon} - g_m^* R_{out} \left(V_{oc} - V_{CMO} \right) \tag{1.18}$$

Solving for V_{oc}, we get:

$$V_{oc} = V_{CMO} + \frac{R_{out} I_{\varepsilon}}{1 + g_m^* R_{out}} \tag{1.19}$$

Comparing this expression with Eqn. (1.13), that was obtained without the CMFB approach, shows that the error present in (1.13) is now divided by ($1+g_m*R_{out}$). Considering that g_m* is generally made equal to the transconductance of a MOSFET, the term g_m*R_{out} is of the order of $(g_m r_d)^2$, that it is >> 1. Therefore, the CMFB strongly reduces the discrepancy between V_{oc} and V_{CMO} caused by I_{ε}. Considering that g_m*R_{out} >> 1, equation (1.19) can be approximated by:

$$V_{oc} = V_{CMO} + I_{\varepsilon} \frac{1}{g_m^*} \tag{1.20}$$

The residual error is now given by the product of I_{ε} by a relatively small resistance, namely $1/g_m*$. As a result, the output common mode voltage V_{oc} differs from V_{CMO} only by a small voltage, which is typically only a few mV large. In practical implementations, g_m* is actually the transconductance of a certain MOSFET. Indicating with I_D* and $V_{TE}*$ the drain current and equivalent thermal voltage, respectively, of that MOSFET, the error can be rewritten as:

$$V_{oc} - V_{CMO} = I_{\varepsilon} \frac{1}{g_m^*} = \frac{I_{\varepsilon}}{I_D^*} V_{TE}^* \tag{1.21}$$

Considering that I_{ε}/I_D* is again of the order of a relative matching error (~10^{-2}), and that $V_{TE}*$ is, at most, of the order of a few hundred mV, the residual error will be only of a few mV. Comparing (1.21) with (1.14) we note that the error is now much smaller and the common mode voltage is effectively stabilized.

Common Mode Feedback control based on a static circuit.

The first example of CMFB circuit [1] is shown in Fig.1.6. This circuit does not involve dynamic operations, such as periodical charging and discharging of capacitors and does not require a clock signal. For this reason, it will be indicated as “static” CMFB.

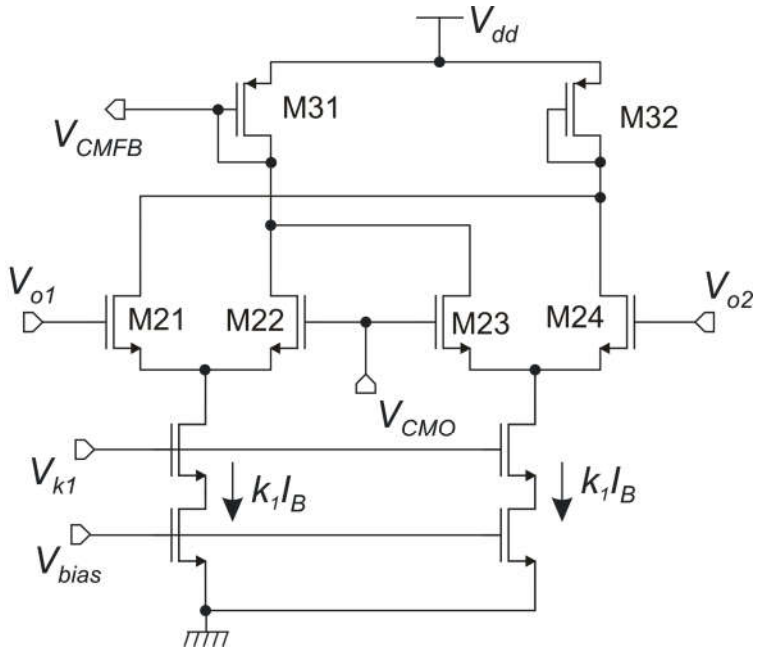

Fig.1.6. Static CMFB circuit

This circuit has to be applied to the amplifier of Fig.1.1, where it substitutes the branch formed by M11a, M11b and M13. The output indicated with V_{CMFB} has to be connected to the gate of M3 and M4 (voltage V_{G3}) in the circuit of Fig.1.1. For simplicity, we will consider that M31 is identical to M3 and M4 and therefore $I_1=I_{D31}$.

$$I_1 = I_{D31} = I_{D22} + I_{D23} \tag{1.22}$$

The circuit is formed by two differential pairs: M21-M22 and M23-M24. These pairs receive the input differential voltages given by $V_{o1}-V_{CMO}$ and $V_{o2}-V_{CMO}$, respectively. If these differential voltages are much smaller than the maximum input value of the pairs, V_{DMAX}, than a linear behavior can be considered and currents I_{D22} and I_{D23} are given by:

$$\begin{cases} I_{D22} = \dfrac{k_1 I_B}{2} - \dfrac{g_{m21}}{2}\left(V_{o1} - V_{CMO}\right) \\ I_{D23} = \dfrac{k_1 I_B}{2} - \dfrac{g_{m23}}{2}\left(V_{o2} - V_{CMO}\right) \end{cases} \tag{1.23}$$

Substituting (1.23) into (1.22) and considering that M21-24 are identical, so that $g_{m21}=g_{m22}=g_{m23}=g_{m24}$, we get:

$$I_1 = k_1 I_B - \frac{g_{m21}}{2}\left(V_{o1} + V_{o2} - 2V_{CMO}\right) = k_1 I_B - g_{m21}\left(\frac{V_{o1} + V_{o2}}{2} - V_{CMO}\right) \tag{1.24}$$

Since $(V_{o1}+V_{o2})/2=V_{oc}$, we finally obtain:

$$I_1 = k_1 I_B - g_{m21}(V_{oc} - V_{CMO}) \tag{1.25}$$

Let us recall that, in order to implement the CMFB control, we needed to produce a current I_1 that follows (1.15) Inspection of Eqn. (1.25) demonstrates that the circuit in Fig.1.6 really perform the required operation with g_m*=g_{m21}.

A major drawback of this circuit is the fact that the two differential pairs M21-22 and M23-24 must operate within the input linearity interval. Note that each pair receive an input voltage equal to the difference between the respective output voltage (V_{o1} or V_{o2}) and the target common mode voltage V_{CMO}. This problem is illustrated in Fig.1.7 where an example of time evolution of the two output signals is represented.

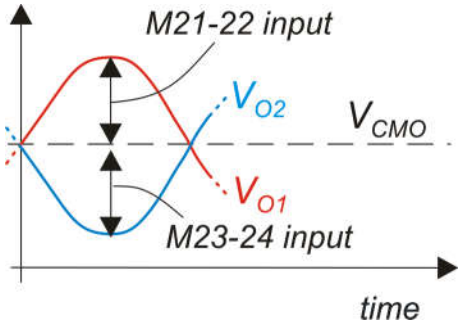

Fig.1.7. Sketch of the signal present at the input of the differential pairs in the static CMFB circuit.

In order for the differential pair to remain in the linearity interval, the maximum difference between each output signals and the common mode voltage V_{CMO} is nearly equal to the gate-overdrive voltage of M21-24. The maximum differential voltage is two times this value, so that:

$$\max(V_{od}) = 2\max(V_{o1,2} - V_{CMO}) \cong 2(V_{GS} - V_t)_{21} \tag{1.26}$$

The overdrive voltages cannot be made arbitrarily large, since the following constraint should also be satisfied:

$$V_{CMO} - V_{GS21} > V_{\min} \tag{1.27}$$

where V_{min} is the minimum output voltage of the mirrors providing the tail currents $k_1 I_B$. It can be easily shown that the maximum feasible V_{GS}–V_t voltages are generally around a few hundred mV, resulting in a maximum swing for V_{od} voltage that rarely exceeds 1 V. Another limitation of the circuit of Fig.1.6 is its static power consumption.

Dynamic Common Mode Feedback control.

An alternative circuit is based on a switched capacitor implementation. Consider voltage V_{G3} in Fig.1.1. If V_{G3}=V_B, then I_1=$k_1 I_B$. If we produce a variation ΔV_{G3} we obtain a current variation given by $\Delta I_1 = -g_{m3}\Delta V_{G3}$. Then, the current I_1 corresponding to a voltage V_B+ΔV_{G3} will be given by:

$$I_1\ (for\ \ V_{G3} = V_B + \Delta V_{G3}) = k_1 I_B - g_{m3}\Delta V_{G3} \tag{1.28}$$

Therefore, in order to implement a CMFB that satisfies (1.15), it is sufficient to produce a voltage V_{CMFB} (i.e. V_{G3}) given by:

$$V_{CMFB} = V_B + (V_{oc} - V_{CMO}) \tag{1.29}$$

If V_{oc} were available, we could obtain it with a two-phase switched capacitor circuit as that of Fig. 1.8 (a).

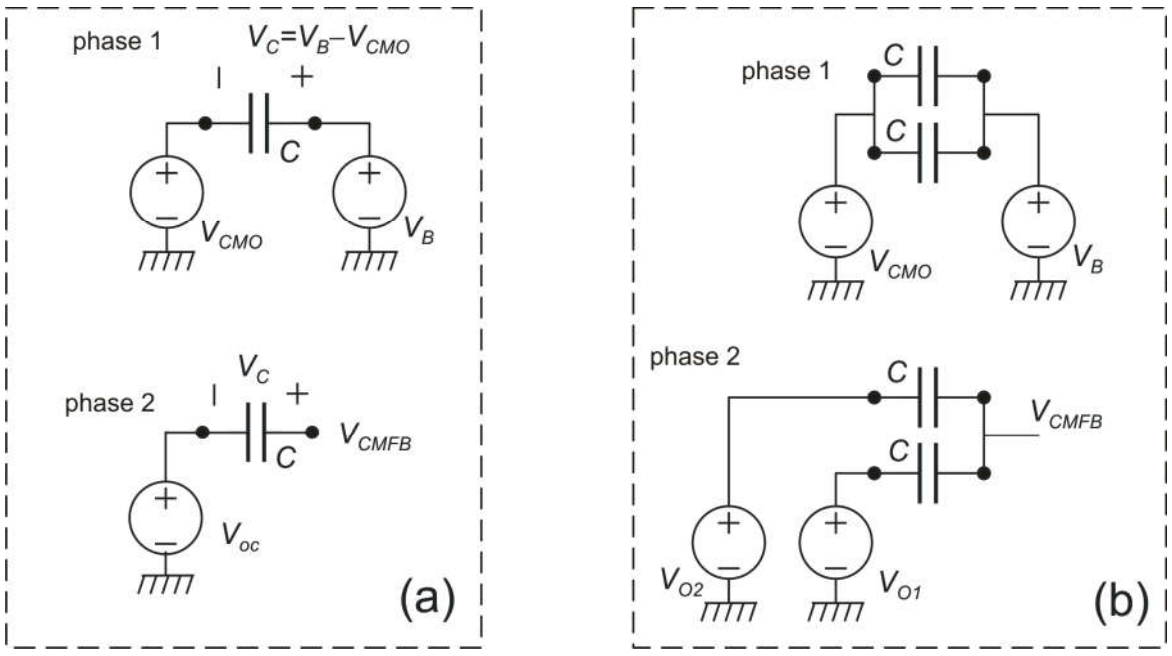

Fig.1.8. Switched capacitor CMFB control when V_{oc} is directly available (a) and not available (b).

In phase 1, the capacitor is pre-charged to $V_B - V_{CMO}$, while in phase 2 the terminal that was connected to V_{CMO} is now connected to V_{oc} and the other terminal is left open so that it produces the voltage:

$$V_{CMFB} = V_{oc} + V_C = V_{oc} + (V_B - V_{CMO}) = V_B + (V_{oc} - V_{CMO}) \tag{1.30}$$

This is just what we need. Unfortunately, V_{oc} is generally not available, so that we have to produce it from the output voltages V_{o1} and V_{o2}. The circuit in Fig.1.8 (b) does this job using two identical capacitors. Phase 1 is identical to the case of Fig.1.8(a) and both capacitors are pre-charged to $V_B - V_{CMO}$ Then, one capacitor is connected to V_{o1} and the other one to V_{o2}. We can intuitively understand that the effect is identical to connecting both capacitors to the average value of V_{o1} and V_{o2}, that is to V_{oc}. The circuit of Fig.1.8 (b) is implemented with the topology shown in Fig.**Error! Use the Home tab to apply Titolo 1 to the text that you want to appear here.**.9.

To study this circuit in a rigorous way, it is useful to first analyze the behavior of a generic capacitive divider as that shown in Fig.1.10. In phase 1, we pre-charge capacitors C_1 and C_2 to voltages $V_1^{(1)}$ and $V_2^{(1)}$, respectively. In phase 2, we connect the capacitor series to a voltage V_{AB}, as shown in the figure. The target is calculating voltages V_1 and V_2 in phase 2. Since capacitors are connected in series, the same charge flows through them in the transition from phase 1 to phase 2. Therefore, we can write the following equation:

$$V_2^{(2)} = V_2^{(1)} + \frac{\Delta Q_{C2}}{C_2} = V_2^{(1)} + \frac{\Delta Q_{C1}}{C_2} \;=\; V_2^{(1)} + \frac{C_1\left(V_1^{(2)} - V_1^{(1)}\right)}{C_2} \tag{1.31}$$

Obviously, voltages in phase 2 should also satisfy:

$$V_1^{(2)} + V_2^{(2)} = V_{AB} \tag{1.32}$$

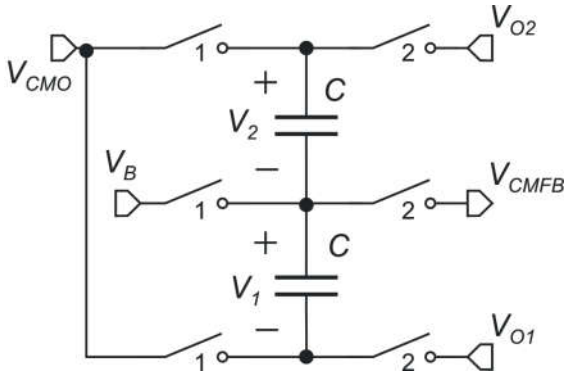

Fig.**Error! Use the Home tab to apply Titolo 1 to the text that you want to appear here.**.9. Actual implementation of the circuit of Fig.1.8 (b): dynamic CMFB circuit.

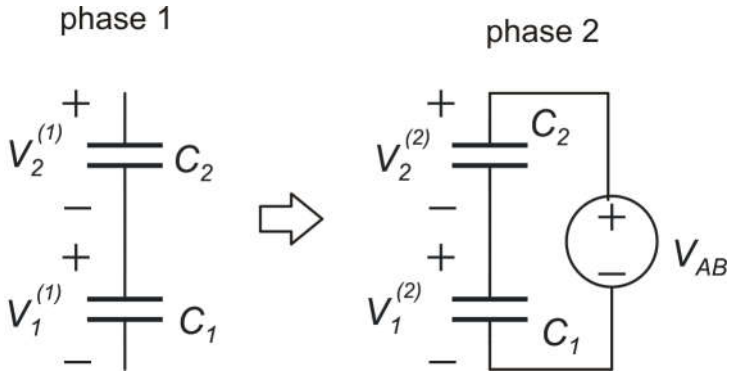

Fig.1.10. Capacitive voltage divider connected to V_{AB} (phase 2) after pre-charging of the individual capacitors (phase 1).

Substituting (1.31) into (1.32) we obtain an equation where the only unknown is $V_1^{(2)}$. Solving this equation, we get:

$$V_1^{(2)} = \frac{C_2 V_{AB} - C_2 V_2^{(1)} + C_1 V_1^{(1)}}{C_1 + C_2} \tag{1.33}$$

Note that if capacitors are not pre-charged, i.e. their voltage is zero in phase 1, (1.33) reduces to the well known ac expression of the capacitive divider: $V_1^{(2)} = V_{AB} C_2/(C_1+C_2)$. Now, let us go back to the CMFB circuit in Fig.**Error! Use the Home tab to apply Titolo 1 to the text that you want to appear here.**.9. In that case, $C_1=C_2=C$. Furthermore, in phase 1 we have:

$$\begin{cases} V_1^{(2)} = V_B - V_{CMO} \\ V_1^{(2)} = -\left(V_B - V_{CMO}\right) \end{cases} \tag{1.34}$$

In phase 2, the common terminal of the two capacitor is not connected to a voltage source and it will assume the voltage V_{CMFB} as a result of charge transfer through the capacitors. Since $V_{AB}=V_{o2}-V_{o1}$, equation (1.33) becomes:

$$V_1^{(2)} = \frac{C\left(V_{o2} - V_{o1}\right) - C\left[-\left(V_B - V_{CMO}\right)\right] + C\left(V_B - V_{CMO}\right)}{2C} = \frac{\left(V_{o2} - V_{o1}\right)}{2} + \left(V_B - V_{CMO}\right) \tag{1.35}$$

Considering that, from the circuit of Fig.**Error! Use the Home tab to apply Titolo 1 to the text that you want to appear here.**.9:

$$V_{CMFB} = V_{o1} + V_1^{(2)} \tag{1.36}$$

We finally get:

$$V_{CMFB} = \frac{\left(V_{o2} + V_{o1}\right)}{2} + \left(V_B - V_{CMO}\right) \tag{1.37}$$

Since $(V_{o2}+V_{o1})/2=V_{oc}$, equation (1.37) is equivalent to (1.30) as initially requested.

The circuit in Fig.**Error! Use the Home tab to apply Titolo 1 to the text that you want to appear here.**.9 should be coupled to the amplifier of Fig.1.1, by connecting V_B, V_{o1} and V_{o2} to the corresponding nodes in Fig.1.1 and V_{CMFB} to V_{G3}. A problem may arise from the fact that during phase 1 the CMFB circuit is disconnected from the amplifier. In this interval, since a feedback path is missing, the output common mode voltage is prone to disturbances and drift. This drawback can be easily overcome with the simple modification shown in Fig.1.11.

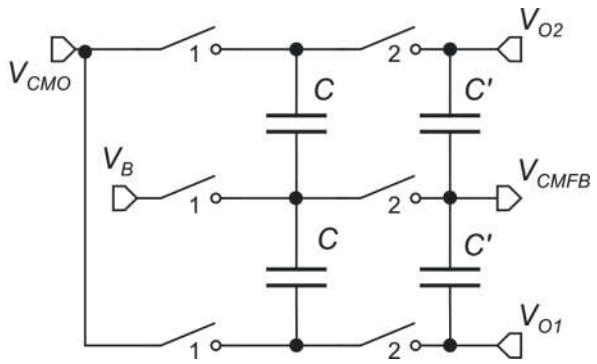

Fig.1.11. Dynamic CMFB with AC feedback path.

In practice capacitors C' have been added between each output terminal and the V_{CMFB} node. These capacitors provide a direct path that is active even during phase 1. If both output voltages increase, then V_{oc} increases, then also V_{CMFB} is pulled up, reducing I_1 through (1.15), and this, in turn, counteracts the initial increase of V_{oc}. On the other hand, the output differential voltage does not affect V_{CMFB}, due to obvious symmetry reasons. Capacitors C' alone could not provide a complete CMFB control, since they are sensitive only to AC variations of V_{oc}. DC feedback is provided by the switched capacitor section composed by capacitors C and the switches.

The dynamic CMFB circuit described in this section does not suffer from output swing limitations, since switches (complementary pass-gates) and capacitors operates correctly over the whole rail-to-rail range. The main drawback of this circuit is the fact that capacitors C are discharged (in phase one) and connected back across the output terminals (v_{o1} and v_{o2}) in phase 2. The current to charge the capacitors in phase 2 must be provided by the output ports. This implies that an impulsive current is drawn from the amplifier, producing unwanted spikes on the output differential voltage and an effect similar to a load resistor that reduces the gain (switched capacitor equivalent resistance).

Noise performance of the folded-cascode fully differential amplifier

The input referred noise of the fully-differential operational amplifier can be studied using the circuit of Fig.1.12.

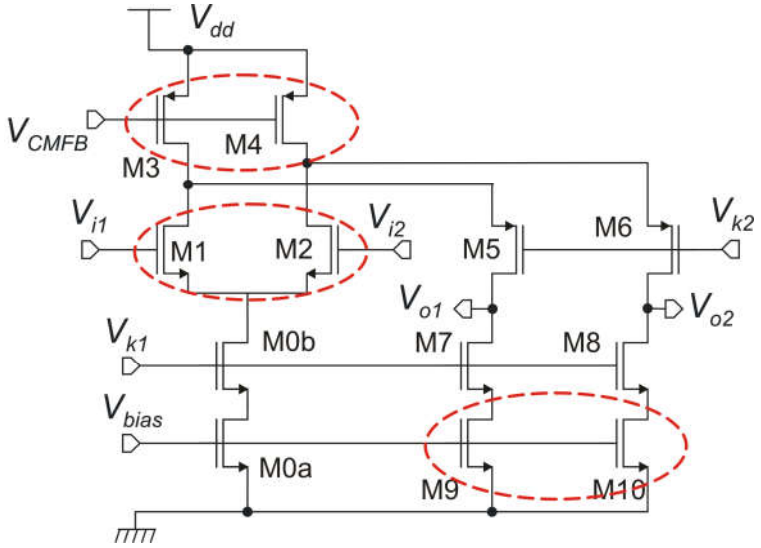

Fig.1.12. Fully-differential operational amplifier with indication of the MOSFETs that give the dominant noise contributions.

In order to evaluate the effect on the output noise, it is necessary to add the noise current sources to all devices shown in Fig.1.12. Then, we can find the contribution of each noise source to the output short-circuit currents I_{SC1} and I_{SC2} and finally calculate the output noise using the equivalent circuit in Fig.1.3.

The analysis is performed on the nominal circuit (no matching errors) with zero input differential voltage.

MOSFETs indicated by the red ellipses in Fig.1.12 produce the dominant noise contributions. All the remaining devices produce negligible effects. In fact:

- M0a and M0b introduce only common mode effects (their noise currents cause identical effects on V_{o1} and V_{o2}) and therefore their contribution in the nominal case (perfectly symmetrical circuit) is zero.
- M7 and M8 are the common gate section of a cascode mirror and we have already shown (see Chap. 3.1) that their contribution is negligible.
- M5 and M6 are the common gate stage of the amplifier. Their contribution to the output short circuit currents is negligible for the same reason of M7 and M8. This is explained in Fig.1.13, where the small signal equivalent circuit of the common gate formed by M5 is represented. Resistor r_{s5} is the small signal resistance connecting M5 source to ground. This resistance, as we have already stated at the beginning of this chapter, is the parallel of r_{d3} and $2r_{d1}$ and is then of the same order of magnitude as r_d. M3 noise source has been split into two current sources, each one with a terminal connected to ground. Repeating the study performed for the cascode mirror in Chap 3.1, we can demonstrate that the two sources give practically opposite contributions to I_{SC1} and then their effect cancels out almost completely.

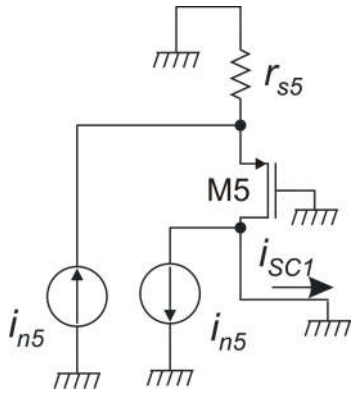

Fig.1.13. Equivalent circuit used to demonstrate that the common gate stage gives a negligible noise contribution

Let us study the effect of the MOSFETs that really give a significant noise contribution.

- The noise currents of M9 and M10 reach the output ports practically unaltered, as demonstrated in Chap. 3.1 about cascode mirrors.
- The same happens to M3 and M4 noise sources. Indeed, they are connected to the input of the common gate stage formed by M5 and M6. Since the input resistance of the common gate ($1/g_{m5}$) is much smaller than all the other resistances connected to M5 and M6 sources (of the order of r_d's), practically the totality of M3 and M4 noise currents get into the common gate stages and, through them, reach the output port, contributing to the output short-circuit currents.
- The noise sources of M1 and M2 are floating; they can be split into two sources, each one with a terminal to *gnd*, exactly as in the case of the two stage, single ended op-amp studied in Chap.3.2. The currents entering M1 and M2 sources produce only a common mode effect, thus they can be ignored. The current sources connected to M1 and M2 drains enter the common gate stage (M5, M6) and ends up into the output short circuit currents.

As a result, with very simple circuit analysis we can write:

$$v_{n-out} = R_{out}\left(i_{nsc2} - i_{nsc1}\right) = \left[\left(i_{n1} - i_{n2}\right) + \left(i_{n3} - i_{n4}\right) + \left(i_{n9} - i_{n10}\right)\right] R_{out} \tag{1.38}$$

The input referred noise can be obtained by dividing $v_{n\text{-}out}$ by $-A_{dd} = -g_{m1}R_{out}$:

$$v_{n-rti} = \frac{\left[\left(i_{n2} - i_{n1}\right) + \left(i_{n3} - i_{n4}\right) + \left(i_{n10} - i_{n9}\right)\right]}{g_{m1}} \tag{1.39}$$

The input noise power spectral density (PSD) can be obtained by substituting the PSDs to each current, taking into account that M2 is identical to M1, M4 to M3 and M10 to M9 and that all noise currents are independent:

$$S_{vni} = 2\frac{S_{I1} + S_{I3} + S_{I9}}{g_{m1}^2} \tag{1.40}$$

Substituting the current PSDs with the corresponding voltage PSDs, we get:

$$S_{vni} = 2\frac{g_{m1}^2 S_{V1} + g_{m3}^2 S_{V3} + g_{m9}^2 S_{V9}}{g_{m1}^2} = 2\left(S_{V1} + F_3^2 S_{V3} + F_9^2 S_{V9}\right) \quad (1.41)$$

where:

$$F_3 \equiv \frac{g_{m3}}{g_{m1}} = \frac{I_{D3}}{I_{D1}}\frac{V_{TE1}}{V_{TE3}}; \quad F_9 \equiv \frac{g_{m9}}{g_{m1}} = \frac{I_{D9}}{I_{D1}}\frac{V_{TE1}}{V_{TE9}} \quad (1.42)$$

Equation (1.42) shows that this stage is not particularly efficient in terms of noise. With respect to the single ended op-amp discussed in Chap. 3.2 there are two more transistors that contribute to the total noise (six instead of four). Furthermore, M3 and M4 give a larger contribution since F_3 includes the ratio I_{D3}/I_{D1}. Typically, in rest conditions, I_{D3} is set to $2I_{D1}$, i.e. $I_{D1}=I_0/2$, $I_{D3}=I_0$. The reason is shown in Fig.1.14, representing the currents in the case of a fully unbalanced input pair caused by a large input differential signal.

Note that, if $I_1<I_0$, the current in M5, calculated as I_1-I_{D1}=I_1-I_0, would be negative. This is not possible, but would simply mean that I_{D5} gets to zero before that the input pair becomes saturated. In that case, the input differential range would not be fully exploited, and the output short circuit current at port V_{o1} would not reach the maximum (negative) value of $I_0/2$. With I_1 set to I_0, M5 drain current gets to zero just when the input differential voltage reaches V_{DMAX}, so that the full input swing is maintained. Increasing I_1 beyond I_0 does not give benefits and only increases power consumption. For this reason, generally I_1 is set to a value close to I_0.

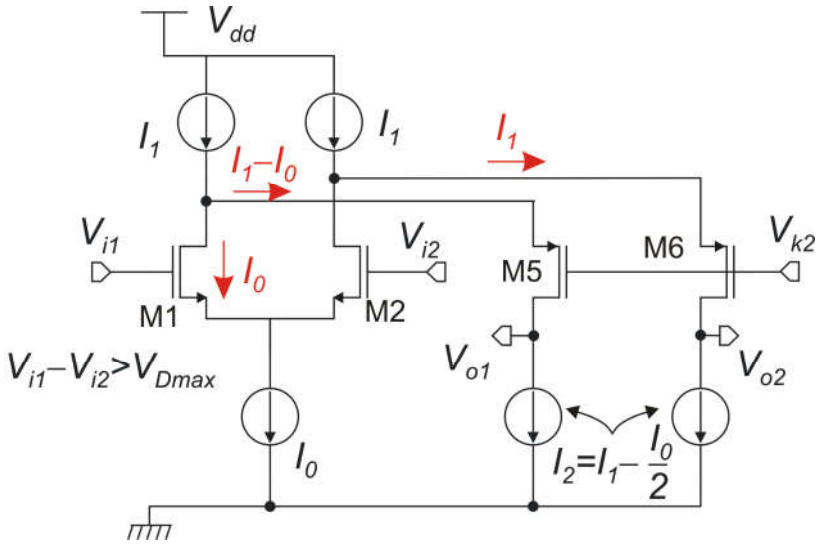

Fig.1.14. Currents in the amplifier for an input differential voltage as large as to fully unbalance the input pair.

With this design choice, the ratio I_{D3}/I_{D1} is equal to 2, so that it is difficult to obtain an F_3 coefficient much smaller than 1 in order to cancel the noise of M3, M4.

Furthermore, this stage is also not efficient in term of power consumption, since we have two sections, namely the common source (M1, M2) and the common gate (M5, M6) each one requiring its own bias current.

1.2 Brief introduction to the telescopic amplifier.

A more efficient stage is the telescopic amplifier [1], consisting in a non-folded cascode amplifier. The schematic view of the telescopic amplifier is shown in Fig. 1.15 (a). The denomination "telescopic" derive by the large number of series devices present between *gnd* and V_{dd}, recalling the structure of an extensible telescope.

In this amplifier, the common source (M1, M2) and common gate (M3, M4) are formed by devices of the same type. In the example of Fig.1.15 (a), they are n-MOS, but the version with all p-MOS is also possible. The advantage of the telescopic amplifier is that the devices of the common gate are placed in series to those of the common source, so that the same current that bias one stage is re-used for the other one. On the contrary, in the folded cascode we need two different currents to bias the common source and the common gate. Then, in equal conditions of bias current for the common source and common gate, the telescopic amplifier used half the current of the folded cascode. Furthermore, with the same arguments that have been used for the noise analysis of the folded cascode, it is possible to show that in the telescopic amplifier only four MOSFETs (instead of six) give a significant contribution to the total noise. These transistors are M1, M2, M7 and M8.

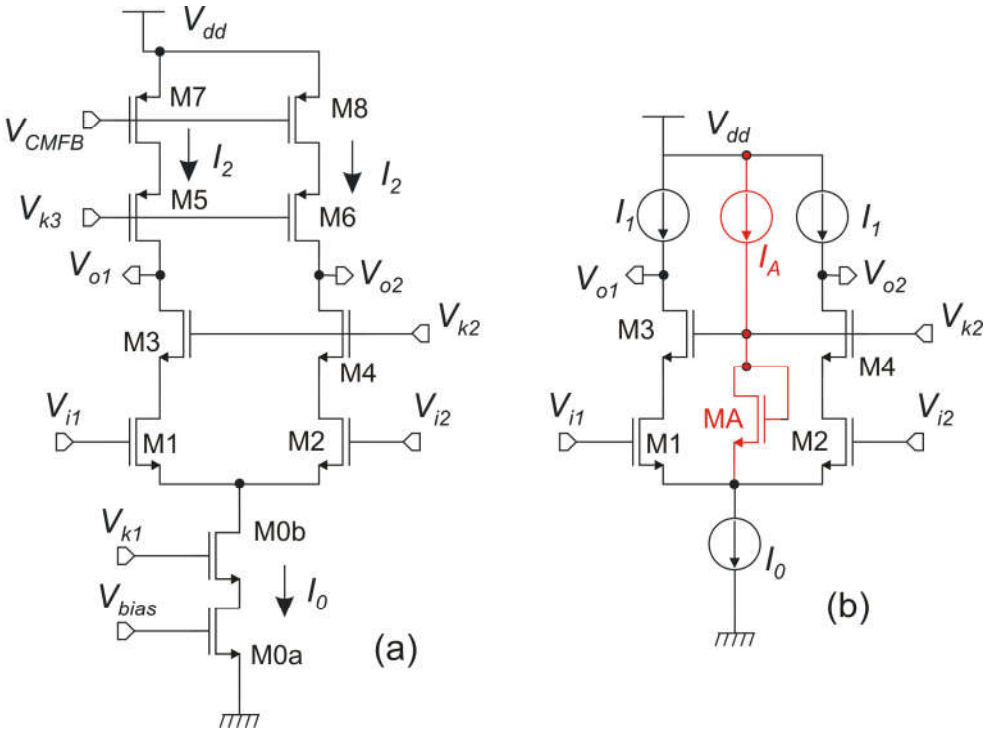

Fig.1.15. Telescopic amplifier (a); a method to adapt the V_{k2} bias voltage to the input common mode voltage (b).

The input referred noise is given by:

$$S_{vni} = 2\left(S_{V1} + F_7^2 S_{V7}\right) \quad \text{with} \quad F_7 = \frac{g_{m7}}{g_{m1}} = \frac{I_{D7}}{I_{D1}} \frac{V_{TE1}}{V_{TE7}} = \frac{V_{TE1}}{V_{TE7}} \tag{1.43}$$

Note that M7 and M8 are biased with the same current as M1 and M2, so that F_7 includes only equivalent thermal voltage ratios that can be easily made smaller than one, attenuating the contribution of M7 and M8. When thermal noise specifications are particularly strict, this contribute to reduce the request for high current consumption, so that the telescopic amplifier can require less than one third of the current of a folded cascode designed for the same input thermal noise density.

Unfortunately, the telescopic amplifier suffers from the well know output swing limitation of pure cascode stages. The output voltage should stay over V_{k2}-V_{tn}, in order to keep M3 and M4 in saturation region. This would suggest to make V_{k2} as low as possible, but V_{k2} sets the upper limit of the input common mode range. Then a trade-off should be made between these two requirements (output swing and input common mode range). As a result, the available output swing is generally much smaller than that of a folded cascode stage.

Thus in a signal processing chain made up of several cascaded stages, the first stage is often a telescopic amplifier, since first stages generally handles small signals, then large output swings are not required. Since the first stage is the one that contribute to most of the noise, the use of a telescopic amplifier allow reaching small input noise densities with relatively low current consumptions. In the following stages, where the signals are larger, folded cascode amplifiers are used, due to their large output range (almost rail-to-rail). The worst noise performance of the folded cascode is not a problem since, being placed after the telescopic amplifier; their contribution to the total noise is less significant.

Let us recall the fact that V_{k2} sets the upper boundary of the input common mode range. This can be a problem if V_{k2} is fixed. Fig.1.15 (a) shows an example of V_{k2} generation which adapts to the input common mode voltage. If V_{ic} increases, also the source voltage of M1 and M2 increases. Device MA, being diode connected and biased by the constant current I_A, acts as a voltage shifter. Indeed: Vk2 is given by:

$$V_{k2} = V_{ic} - V_{GS1} + V_{GSA} \tag{1.44}$$

Eqn. (1.44) proves that, if V_{ic} increases also V_{k2} is increased of nearly the same amount, extending the input common mode range. Obviously, the increase of V_{k2} reduced the available output swing, thus the circuit of Fig.1.15 (b) does not eliminate the typical limitation of telescopic amplifier, but makes it more flexible, since the trade-off between the input range and the output swing is changed as a function of the characteristics of the input signal.

1.3 Frequency response and compensation of the folded cascode fully differential operational amplifier

Before analyzing the complete amplifier, it is necessary to find an approximate and very simplified description of the frequency behavior of a common gate stage. The small signal equivalent circuit that we will consider is shown in Fig.1.16, where we have depicted the common gate stage formed by M5

in the circuit of Fig.1.1. In most cases of interest for integrated circuits, it is convenient to consider that the input signal of the common gate is a current, represented by current source i_s in Fig.1.16. The output signal consists in the short circuit current i_{sc}. Resistor r_{s5} is the parallel of all resistances that connect the source of M5 to *gnd*. This resistance, as we have already found previously, is of the order of the r_d.

Parasitic capacitance C_p is the sum of the C_{GS5} (dominant contribution), C_{SB5} and the C_{DB} of all the MOSFETS whose drains are connected to the common gate input (M1 and M3 for the amplifier of Fig.1.1).

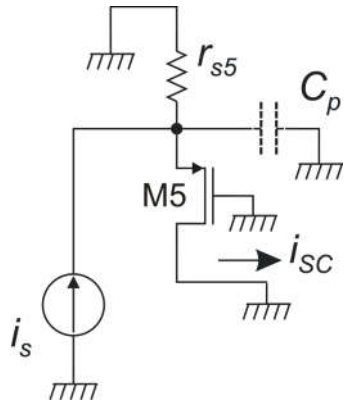

Fig.1.16. Small signal equivalent circuit of the common gate stage formed by M5 in the folded cascode amplifier.

The resistance seen toward the source of M5 is practically equal to $1/g_{m5}$. At low frequencies, where C_p can be neglected, i_{sc} is practically equal to i_s, since the input resistance ($1/g_{m5}$) and r_{s5} form a current divider where $1/g_{m5}$, being much smaller than r_{s5} gets almost the totality of the current. At higher frequencies, the impedance of C_p gets so low that it cannot be neglected with respect to $1/g_{m5}$. The capacitors start stealing current and i_{sc} is progressively reduced. As the frequency tends to infinity, i_{sc} tends to zero. With these considerations, it is easy to understand that the simplified transfer function of the stage is:

$$f_{CG}(s) = \frac{1}{1+\frac{s}{\omega_{CG}}} \qquad \text{where:} \quad \omega_{CG} = \frac{1}{\frac{1}{g_{m5}}C_p} = \frac{g_{m5}}{C_p} \tag{1.45}$$

Now, let us go back to the folded cascode amplifier. Consider the circuit in Fig.1.12 from the point of view of small circuit analysis. The input pair, (M1, M2), injects differential mode currents into the common gate stage (M5, M6), so that M5 receives $-g_{m1}v_{id}/2$ and M6 $g_{m1}v_{id}/2$. In addition, M3 and M4, driven by V_{CMFB}, injects the common mode currents given by (1.15), where the small signal component is $-g_m * v_{oc}$. These currents reach the output nodes through the common gate stage and form the output short circuit currents i_{sc1} and i_{sc2}. Then:

$$\begin{cases} i_{sc1} = \left(-g_{m1}\frac{v_{id}}{2} - g_m^* v_{oc}\right) f_{CG}(s) \\ i_{sc2} = \left(g_{m1}\frac{v_{id}}{2} - g_m^* v_{oc}\right) f_{CG}(s) \end{cases} \tag{1.46}$$

The small signal equivalent circuit of the amplifier output ports is shown in Fig.1.17 where the common mode capacitors (C_o) and the differential mode capacitor (C_D) are shown. The capacitors are the sum of load capacitors and parasitic capacitors.

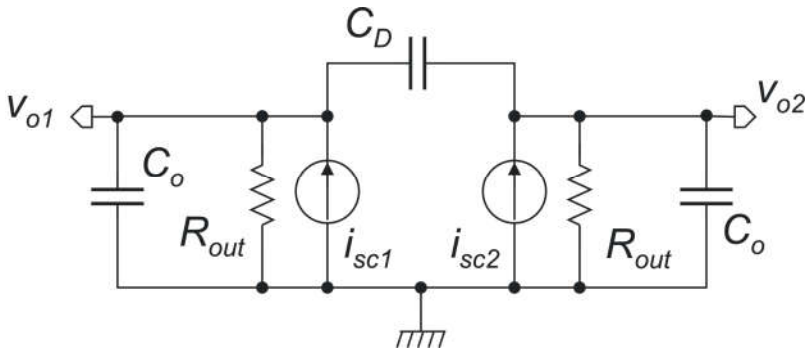

Fig.1.17. Small signal equivalent output circuit.

If we consider only the differential components of i_{sc1} and i_{sc2}, the reduced equivalent circuit shown in Fig.1.18 can be used. Capacitor C_{oD} is given by:

$$C_{oD} = C_o + 2C_D \tag{1.47}$$

The differential mode gain is given by:

$$A_{dd}(s) \equiv \frac{v_{od}}{v_{id}} = \frac{-2v_{o1}}{v_{id}} = g_{m1}R_{out}\frac{1}{1+s/\omega_{pd}}f_{CG}(s) \tag{1.48}$$

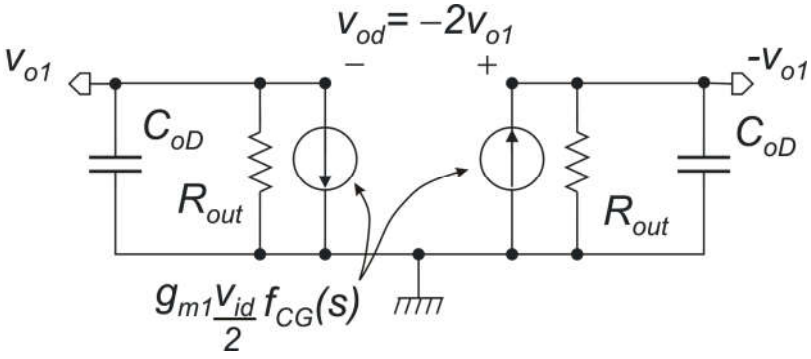

Fig.1.18. Small signal equivalent output circuit for the differential mode

where we note that the differential mode output capacitance COD create a pole of angular frequency ω_{pd} , given by:

$$\omega_{pd} = \frac{1}{R_{out} C_{oD}} \tag{1.49}$$

Due to the very high output resistance, the angular frequency of the pole, ω_{pd}, is much smaller than ω_{CG}, therefore ω_p is the dominant pole. In these conditions, the unity gain frequency for the differential mode amplification is given by:

$$\omega_{0D} = \frac{g_{m1}}{C_{oD}} \tag{1.50}$$

If we intend to use the amplifier in closed loop configuration and we want it to be stable, with a reliable phase margin, even in the case of β=1 (output V_{o1} connected to input V_{i2} and V_{o2} to V_{i1}), then the first non-dominant pole (ω_{CG}) should be at frequencies higher than ω_{0D}. Considering the analysis made in Chap. 3.2 for the single-ended op-amp, ω_{0D} and ω_{CG} play the role of ω_0 and ω_2, respectively. If ω_{0D} is too high, it can be reduced by simply increasing the capacitive load of the amplifier, as clearly suggested by (1.50). Clearly, this has the side effect of reducing the GBW, which is equal to $\omega_{0D}/2\pi$. If the specifications do not allow this, it is necessary to increase ω_{CG}, and this is generally done by increasing the bias current and then the power consumption.

In addition to differential mode stability, also common mode stability should be guaranteed. The output common mode voltage is set to the desired value by a feedback loop (CMFB) that should be stable. The output equivalent circuit for only the common mode voltage is shown in Fig.1.19. The differential mode capacitance C_D does not affect the common mode behavior since it connects two points, V_{o1} and V_{o2}, which are symmetrical in the common mode analysis, and then are at the same potential.

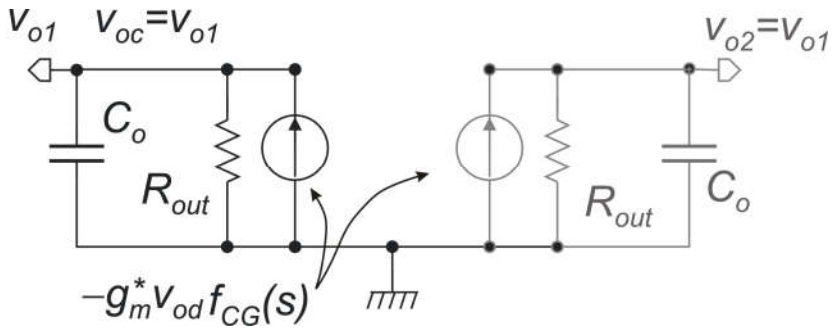

Fig.1.19. Small signal equivalent output circuit for the common mode. The section corresponding to v_{o2} is identical to that of v_{o1}, so that only one section can be considered.

Note that v_{oc} depends on the current sources, which, in turn, depend on v_{oc}. This can be schematically represented by the block diagram of Fig.**Error! Use the Home tab to apply Titolo 1 to the text that you want to appear here.**.20, which is equivalent to the circuit in Fig.**Error! Use the Home tab to apply Titolo 1 to the text that you want to appear here.**.20.

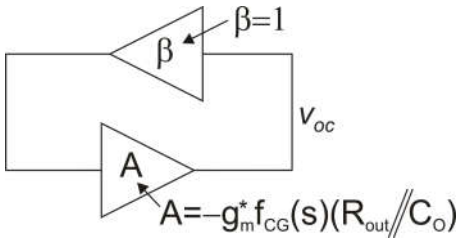

Fig.**Error! Use the Home tab to apply Titolo 1 to the text that you want to appear here.**.20. Block diagram representation of the small signal, common mode feedback loop

The circuit represent a classical feedback where the loop gain is given by:

$$A_{CMFB}(s) = -g_m^* \frac{R_{out}}{1 + s/\omega_{pc}} f_{CG}(s) \tag{1.51}$$

The angular frequency of the CMFB dominant pole, ω_{pc} is given by:

$$\omega_{pc} = \frac{1}{R_{out} C_o} \tag{1.52}$$

while, as for the differential mode gain, the first non-dominant pole is due to the common gate stage (ω_{CG},). The CMFB unity gain angular frequency, ω_{0C}, is given by:

$$\omega_{0C} = \frac{g_m^*}{C_o} \tag{1.53}$$

Again, in order to achieve a large phase margin for of the CMFB loop, ω_{CG} should be higher than ω_{0C}, possibly $\omega_{CG} \geq 3\omega_{0C}$. This can be obtained by reducing ω_{0C}, increasing the common mode capacitors C_o. Note that increasing C_o, we reduce both ω_{0C}, and ω_{0D}, improving at the same time the differential and common mode stability.

1.4 Transformation of the folded cascode operational amplifier into an instrumentation amplifier.

The topology illustrated in Fig.1.1 can be simply modified to obtain an instrumentation amplifier (in-amp) that, differently from other architectures, does not uses negative feedback from the output to the input to set a precise gain. A simplified schematic view of this amplifier is shown in Fig.1.21.

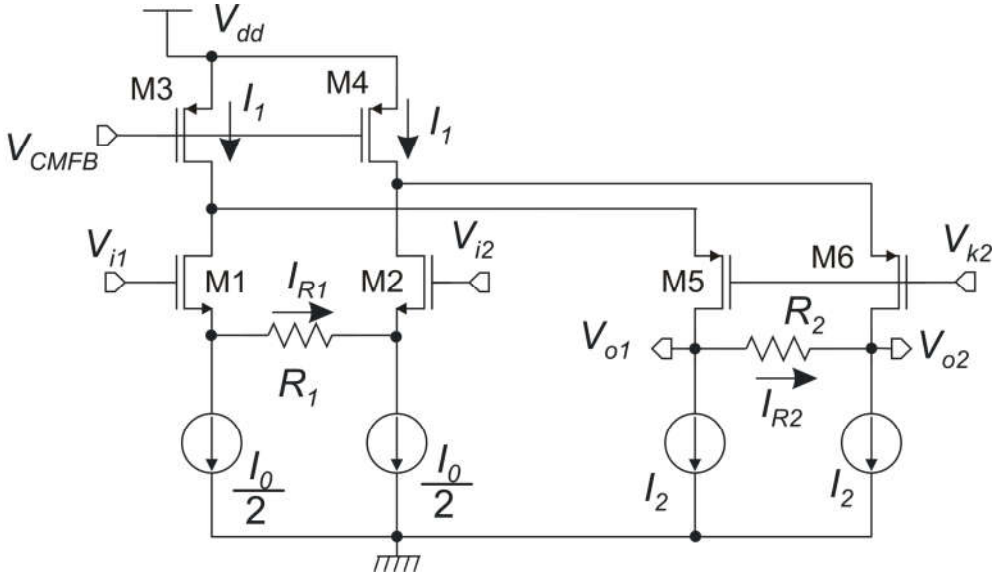

Fig.1.21. Fully differential instrumentation amplifier.

The operating principle is based on source degeneration, i.e. the insertion of the resistance R_1 in series with M1 and M2 sources. The bias source I_0 (tail current) has been split into two sources $I_0/2$. In this way, in rest conditions (v_{id}=0, symmetric configuration), no current flows into R_1. Let us write currents I_{D1} and I_{D2}:

$$\begin{cases} I_{D1} = \dfrac{I_0}{2} + I_{R1} \\ I_{D2} = \dfrac{I_0}{2} - I_{R1} \end{cases} \tag{1.54}$$

Subtracting I_{D2} from I_{D1} we find:

$$I_{D1} - I_{D2} = 2I_{R1} \tag{1.55}$$

The voltage across resistor R1 is the difference between the source voltages of M1 and M2:

$$V_{R1} = V_{S1} - V_{S2} = V_{i1} - V_{GS1} - \left(V_{i2} - V_{GS2}\right) \quad = \quad V_{id} - \left(V_{GS1} - V_{GS2}\right) \tag{1.56}$$

If V_{GS1} were equal to V_{GS2}, then the voltage across R_1 would be equal to the input differential voltage. We will discuss later how precisely this could happen. For now, we will suppose that:

$$V_{R1} \cong V_{id} \tag{1.57}$$

At the amplifier output, we can write:

$$\begin{cases} I_{D5} = I_2 + I_{R2} \\ I_{D6} = I_2 - I_{R2} \end{cases} \tag{1.58}$$

But: $I_{D5}=I_1-I_{D1}$ and $I_{D6}=I_1-I_{D2}$. Substituting these expressions into (1.58) we get:

$$\begin{cases} I_1 - I_{D1} = I_2 + I_{R2} \\ I_1 - I_{D2} = I_2 - I_{R2} \end{cases} \tag{1.59}$$

Subtracting these two equations, we find:

$$I_{R2} = \frac{-(I_{D1} - I_{D2})}{2} \tag{1.60}$$

Using (1.55), we finally get:

$$I_{R2} = -I_{R1} \tag{1.61}$$

We can write I_{R2} as a function of the output differential voltage, $V_{od}=V_{o2}-V_{o1}$:

$$I_{R2} = \frac{V_{o1} - V_{o2}}{R_2} = \frac{-V_{0d}}{R_2} \tag{1.62}$$

Using (1.62) for I_{R2} and the approximate relationship (1.57) for V_{R1}, equality (59) finally gives:

$$A_{dd} \equiv \frac{V_{od}}{V_{id}} = \frac{-I_{R2}R_2}{V_{id}} = \frac{I_{R1}R_2}{V_{id}} = \frac{\frac{V_{id}}{R_1}R_2}{V_{id}} = \frac{R_2}{R_1} \tag{1.63}$$

Summarizing: the degenerated input pairs produce a current difference, I_{D1}-I_{D2} that is nearly proportional to the input signal, and in particular equal to V_{id}/R_1. This current is transported to the output ports and made to flow into R_2. The output voltage is then $V_{id}R_2/R_1$. The amplifier gain is then given by a resistor ratio and can be made precise.

Now, let us come back to the assumption of linearity between V_{R1} and $V_{id,}$ expressed by (1.57). This is based on the fact that the term ($V_{GS1}-V_{GS2}$) in (1.56) can be neglected, i.e. V_{GS1} and V_{GS2} are practically equal. Since, as suggested by (1.54), I_{D1} grows and I_{D2} diminishes for positive I_{R1} (and vice versa for negative I_{R1}), V_{GS1} and V_{GS2} variations, occurring when a signal is applied, are opposite. For this reason, ($V_{GS1}-V_{GS2}$) is negligible only when I_{D1} and I_{D2} variations are negligible with respect to the quiescent current $I_0/2$. Since (1.54) states that the I_D variations are equal to $\pm I_{R1}$, it is necessary to guarantee that I_{R1} is much smaller than $I_0/2$ over the whole range of input signals. This is generally not efficient in terms of power consumption, since it would require bias currents much larger than the maximum current variations induced by the signal. This is also not efficient in terms of noise, since the current noise produced by current sources (I_0, I_1 and I_2 in Fig.1.21) is proportional to the bias current (see Chap 3.1 on current mirrors), so that the signal to noise ratio is degraded.

In order to solve this problem, several solutions can be adopted. The simplest is shown in Fig.1.22, that represents only the input pair and resistor R1, since the rest of the circuit is unchanged.

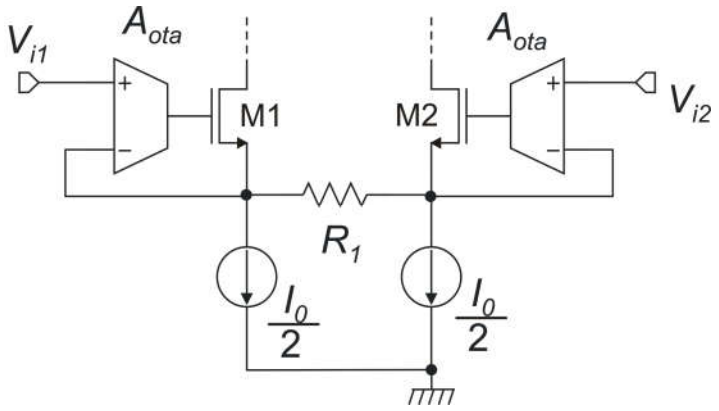

Fig.1.22. Modification of the input stage by the introduction of servo-amplifiers.

In practice, M1 and M2 acts as source follower stages cascaded to the differential amplifier indicated with A_{ota}. The source voltage of M1 and M2 are the output of the composed amplifiers formed by the mentioned cascade. Note that these outputs are connected to the corresponding inverting inputs, forming unity gain amplifiers that precisely replicates the inputs V_{i1} and V_{i2} to nodes S1 and S2, respectively. In this way, the differential input voltages is precisely transferred across resistor R1 and (1.57) can be assumed to be true over a wide range of input signals.

Finally, we will mention the fact that having placed a resistor across the output ports of the amplifier greatly simplifies the implementation of the CMFB loop. Indeed, we can split resistor R_2 into two resistors of value $R_2/2$ as in Fig.1.23 (a). The central point of the resistance now is equal to the output common mode voltage. In this way, the CMFB circuit is simply a differential pair as shown in Fig.1.23 (b). Note that the input of this pair is only the difference between the actual common mode voltage V_{oc} and the target value V_{CMO}, so that it does not impose the limitations to the output swing described for the circuit of Fig.1.6. Clearly, this solution was not possible for the operational amplifier of Fig.1.1, where placing a resistor across the output would mean an unacceptable gain reduction.

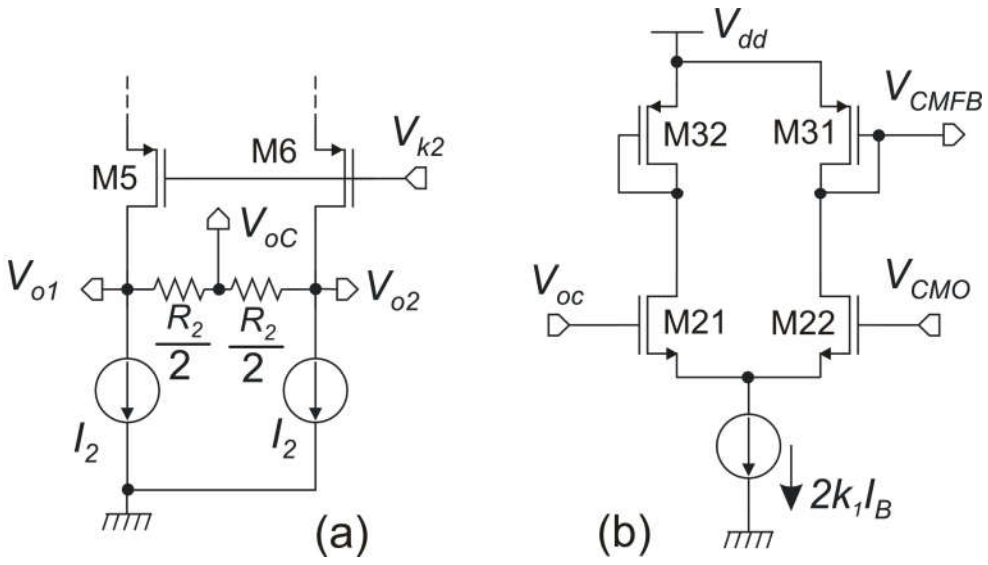

Fig.1.23. Common mode feedback (CMFB) control, optimized for the in-amp if Fig.1.21.

1.5 Transformation of the folded cascode operational amplifier into a DDA

The symbol of the DDA is recalled in Fig.1.24. The difference with respect of the simple fully-differential amplifier is the presence two differential input ports: Port B and Port A.

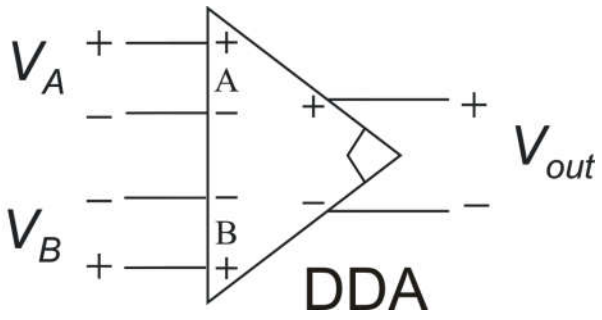

Fig.1.24. Symbol of a DDA.

The two ports should have identical characteristics, so that the DDA is characterized by the following input/output relationship:

$$V_{od} = A(V_A + V_B) \text{ with } \quad A >> 1 \tag{1.64}$$

where V_A and V_B are the differential voltage applied to port A and B, respectively. To obtain DDA, it is possible to expand the amplifier of Fig.1.1 by simply adding a differential pair. The result is shown in Fig.1.25, where the additional differential pair is enclosed in the gray box.

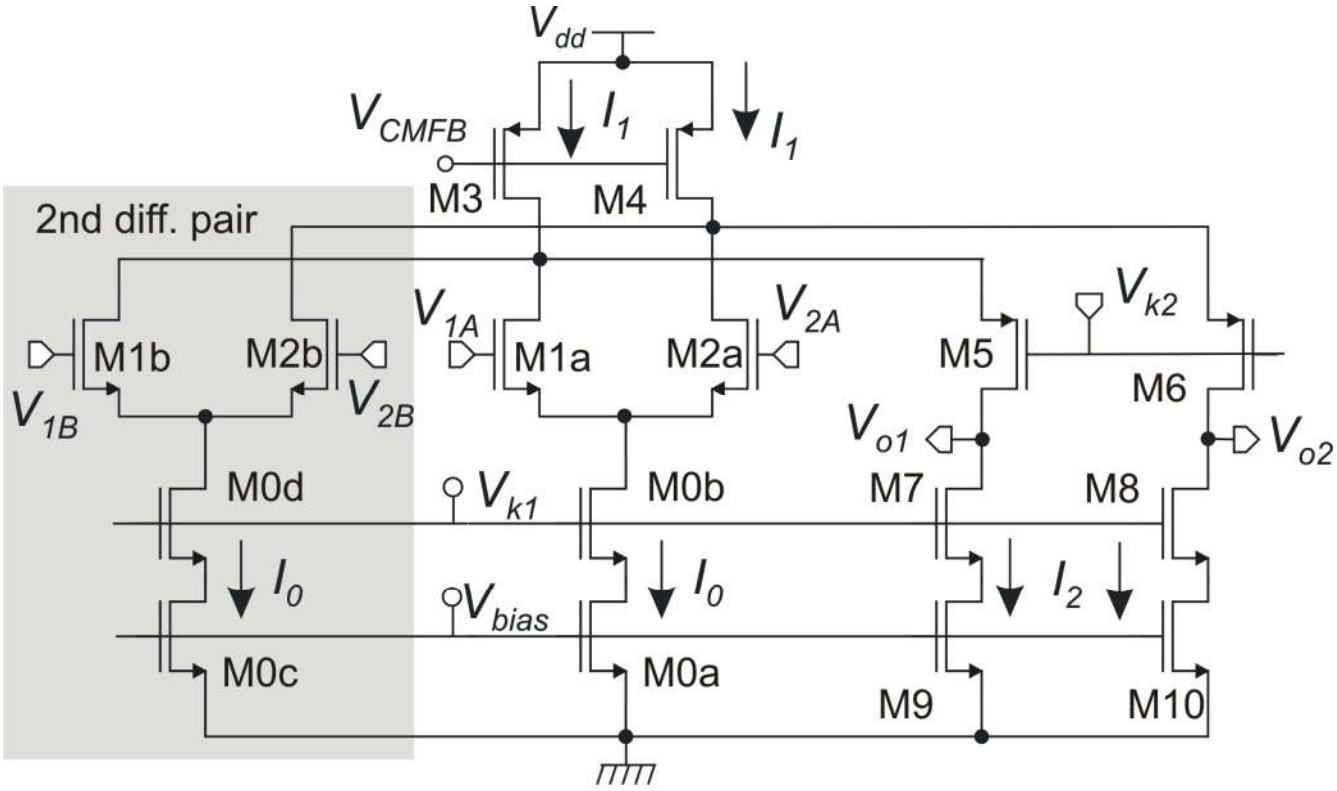

Fig.1.25. A DDA obtained by adding a differential pair (gray box) to a folded cascode fully-differential op-amp.

Obviously, current I_1 should now feed two differential ports and output common gate. Therefore its nominal value should be $(3/2)I_0$ (it was I_0 in the single-input port op-amp of Fig.1.1). A CMFB circuit is needed also for this amplifier to adjust I_1 around the nominal value in a closed loop fashion and set the output common mode voltage to the desired level. The costs of adding the second port are:

- Increased supply current
- Increased input referred noise.

1.6 Two-stage fully-differential operational amplifier.

As in most single-stage architectures, the folded cascode operational amplifier or DDA is not suitable to drive low resistive loads. This is due to the fact that the high gain of the stage is due to the very high output resistance, which can be of the order of several megaohms or even tens of megaohms. Resistive loads of several hundred kilohoms or lower would excessively degrade the DC gain of the amplifier, impairing accuracy.

In these cases, a two-stage architecture is recommended. With a two-stage amplifier, the first stage is not directly connected to the load, so that its output resistance is not affected by the latter. In order to maintain a rail-to-rail output range, it is necessary to use common-source output stages. In the case of a

fully-differential amplifier it is necessary to add two common source amplifier, one for each output terminal. A possible architecture is shown in Fig.1.26, where the double common-source output stage is included in the gray box.

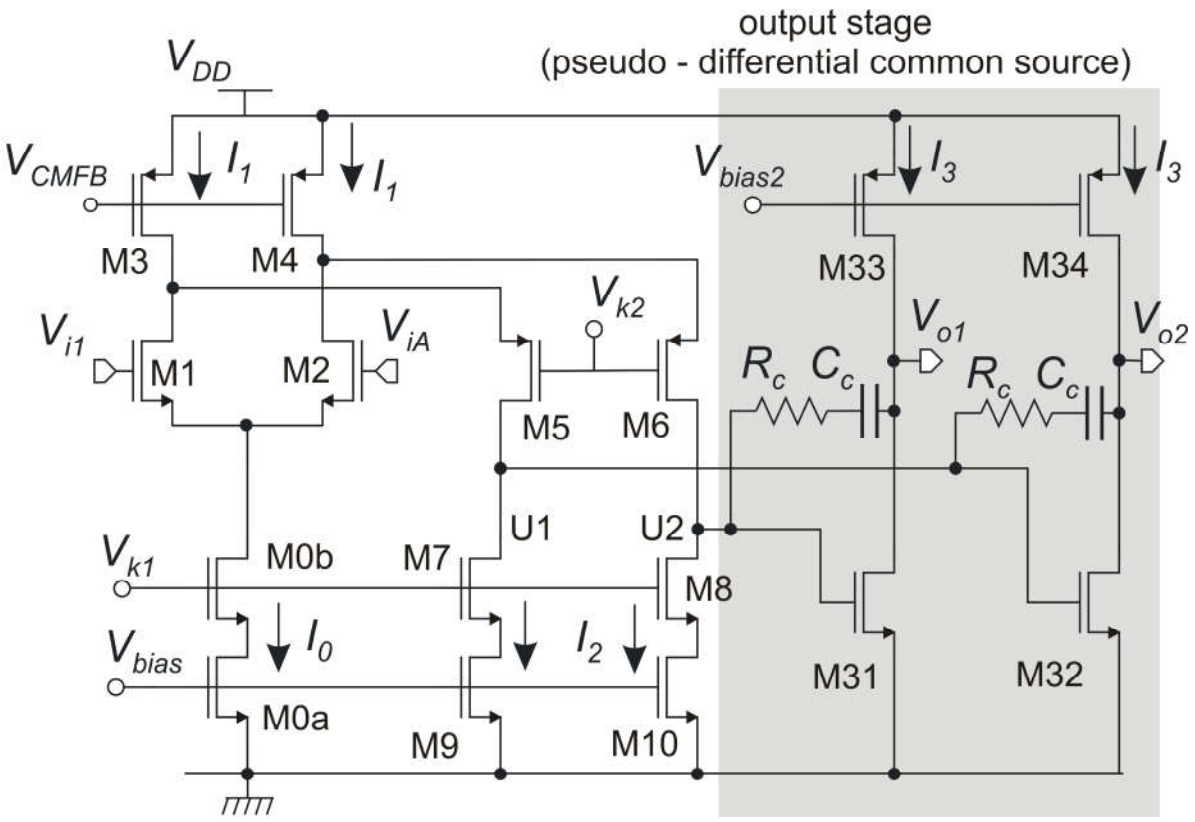

Fig.1.26. A two-stage fully-differential op-amp.

The double common-mode source is called "pseudo-differential", since it has also a large common-mode-to common mode gain. This is not a problem with this architecture, but is an advantage since it allows building a single CMFB control for the whole amplifier. As for the single stage amplifiers analyzed so far, the CMFB circuit will sense the output voltage V_{o1} and V_{o2} and modify I_1, until V_{oc} is equal to the desired target voltage (V_{CMO}). The only difference is that there is an inversion from the common mode voltage of the first stage (present at nodes U1 and U2) and the output common mode voltage of the second stage. For this reason, the relationship between I_1 and V_{oc} will be opposite with respect to the single-stage amplifier:

$$I_1 = k_1 I_B + g_m^* \left(V_{oc} - V_{CMO} \right) \tag{1.65}$$

Finally, note that Miller compensation (C_C, R_C series) is used to obtain stable closed loop operation of the amplifier and, at the same time, to stabilize the CMFB loop.

References

[1] P. Gray, P.J. Hurst, S.H. Lewis, R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th Edition, John Wiley and Sons, New York, 2001, Chap. 12.