1 Sensor Interfaces

1.1 Classification of sensors according to the output electrical quantity.

Output electrical quantity	Sensor type	Input physical or chemical quantity. The quantity that is directly measured by the sensor is indicated in boldface
Voltage	Thermoelectric sensors	**Temperature difference** Temperature Fluid flow rate Infrared radiation (bolometers) Gas concentration (catalytic sensors)
	Electrochemical sensors	**Ion concentration in electrolytes** Gas concentration (e.g.. "lambda probes")
	Hall sensors	**Magnetic Field** Position (Proximity) Current measurement
	Piezoelectric sensors	**Force** (not suitable for DC measurements) Acoustical pressure, acceleration.
Current	Optical sensors (photodiodes)	**Infrared, visible and Ultraviolet radiation** Imagers Proximity Opacity (e.g. smoke detectors)
Charge	CCD imagers	**Visible radiation**
	High energy particle detectors	**Ionizing radiation and particle detection**
Resistance	Thermistor and RTDs (Resistive Temperature Detectors)	**Temperature** Fluid flow rates Fluid velocity (e.g. hot wire anemometers) Gas concentration (catalytic sensors) Proximity
	Piezo-resistors	**Strain (strain gauges)** Force (e.g. electronic scales) Pressure (barometers) Altitude Acceleration
	Chemi-resistors	**Gas or vapor concentration (e.g. MOX gas sensors)**
	Magneto-resistors	**Magnetic field** Proximity Orientation (e.g. electronic compass)
	Photo resistors	**Visible radiation**
Capacitance	Capacitive sensors (mechanical)	Acceleration Angular velocity (gyroscopes) Pressure
	Capacitive sensors (chemical)	**Gas concentration (e.g. humidity sensors)**

Table **1**.1 Sensors of frequent use classified according the output electrical quantity.

1.2 General considerations on sensor interfacing.

Any sensor has an intrinsic maximum resolution and dynamic range that depend on the sensor sensitivity and noise. As we have seen, any successive block (AFE, ADC, Digital prost processor) can only degrade this theoretical limit, since additional noise components and range limitations are introduced. Optimal interface design means that the degradation is negligible, so that the theoretical performances of the sensor are preserved. This target has to be fulfilled taking into account also other constraints, such as power consumption, size, and fabrication costs. In a significant number of

cases, the design of an optimal interface requires also the development of non-standard readout approaches and dedicated topologies. However, it is possible to find a small number of universal interfaces and readout approaches that can be used to read a wide range of sensors, effectively. The following table indicates which is the typical AFE that is used for different sensor categories, classified on the basis of the output electrical quantity produced by the sensor.

Output quantity	AFE	Notes
Voltage	Instrumentation Amplifier (In-Amp)	
Resistance	Instrumentation Amplifier	Resistors should be mounted in a Wheatstone bridge configuration or biased by a current.
	Trans-Impedance Amplifier (TIA)	Resistor must be biased with a voltage in order to produce a current
Current	Trans-Impedance Amplifier (TIA)	
Capacitance	Trans-Impedance Amplifier (TIA)	Converting capacitance into a current by means of a periodic voltage waveform
	Charge amplifier (switched capacitor)	
Charge	Charge amplifier	

Table 1.2. Typical sensor interface front ends

In the following part of this section, we will analyze a few aspect related to the use of instrumentation amplifiers and TIAs. Here we will briefly recall the typical methods by which a resistance signal can be converted into a voltage signal.

The simplest and more straightforward technique is biasing the resistor with a constant current, as shown in Fig. 1.1 (a).

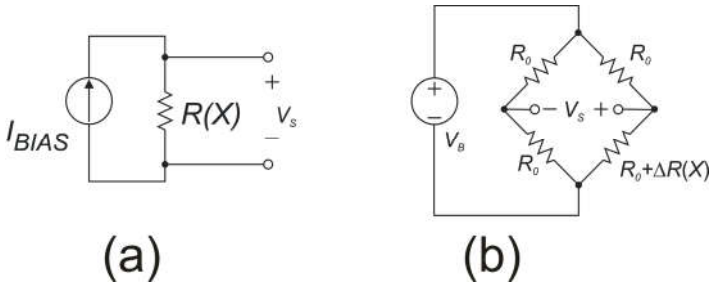

Fig. 1.1 Resistive sensor interfacing: (a) constant current biasing, (b) Wheatstone bridge configuration.

Let us express the resistance dependence on the input quantity x as:

$$R(x) = R_0 + \Delta R(x) \tag{1.1}$$

where R_0 is a constant resistance and $\Delta R(x)$ is the resistance variation assumed to be zero when $x=x_{min}$. With the constant current bias method, the output voltage is:

$$V_S = I_{BIAS} R_0 + I_{BIAS} \Delta R(x) \tag{1.2}$$

Note that the output voltage includes a constant term $I_{BIAS}R_0$. This term is affected by variations of both R_0 and I_{BIAS}, due to temperature drift or process spread. In addition, the noise component of I_{BIAS}, will be converted into an output noise. This condition is particularly disadvantageous when the

maximum variation of $\Delta R(x)$ is much smaller than R_0. In these cases, the solution shown in Fig. 1.2(b) is more convenient. The sensing resistor forms a Wheatstone bridge together with other resistors whose value is R_0. It can be easily shown that the output voltage V_S, for $\Delta R(x) << R_0$ is given by:

$$V_S \cong \frac{\Delta R(x)}{4R_0} V_B \tag{1.3}$$

Furthermore, if all resistors have the same temperature coefficient, temperature variations are cancelled for $\Delta R(x)=0$. This indicates that the Wheatstone bridge configuration is marked by small offset drift. In the case of integrated sensors, the whole Wheatstone bridge is fabricated on the same substrate as the sensing element. Another important fact is that the output signal is proportional to the voltage V_B applied to the bridge. Setting $V_B=V_{dd}$ the Wheatstone bridge becomes a ratiometric system.

1.3 Practical consideration on the use of Instrumentation Amplifiers.

An instrumentations amplifier has the following characteristics:

- Precise gain
- High input resistance
- Differential input

Furthermore, in order to be effectively used for sensor interfacing, the In-Amp should also exhibit:

- Low input referred offset voltage
- Low bias currents
- Low input referred voltage and current noise
- High CMRR

Fig. 1.2 shows the typical connection of an In-Amp to a differential input source (representing the sensor). V_{CM} is the common mode voltage of the source, while the ideal output signal of the sensor is $V_{S1}-V_{S2}$. Resistors R_{S1} and R_{S2} represent the internal resistances of the source. In the case of a balanced source, we have $R_{S1}=R_{S2}$. The In-Amp has been represented as an ideal amplifier (i.e. noiseless) with input noise voltage and current sources. The DC components of these sources represent the offset voltage and bias currents. In order to evaluate the effect of the noise sources on the voltage read by the interface, it is convenient to calculate the voltage at the input of the ideal amplifier:

$$v_{in} = V_{S1} - i_{B1}R_{S1} - v_n - \left(V_{S2} - i_{B2}R_{S2}\right) = V_{S1} - V_{S2} - v_{nt} \tag{1.4}$$

where v_{nt} is the total equivalent noise, given by:

$$v_{nt} = v_n + i_{B1}R_{S1} - i_{B2}R_{S2} \tag{1.5}$$

In the case of balanced source, defining $R_S \equiv R_{S1}=R_{S2}$, we have:

$$v_{nt} = v_n + R_S\left(i_{B1} - i_{B2}\right) \tag{1.6}$$

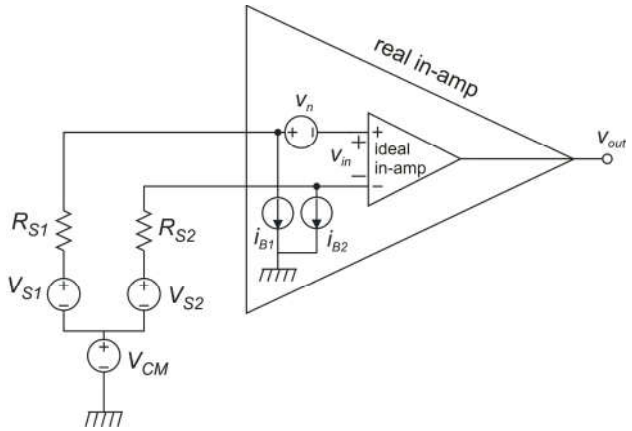

Fig. 1.2. Connection of an instrumentation amplifier to a differential voltage source, with indication of the input voltage and current noise sources.

Considering only the DC components, the total offset, v_{iot} is given by:

$$v_{iot} = v_{io} + R_S\left(I_{B1} - I_{B2}\right) = v_{io} + R_S I_{io} \tag{1.7}$$

where $I_{io}=I_{B1}-I_{B2}$ is the offset current. Note that, in modern instrumentation amplifier, the offset current is generally similar or even larger than the bias currents, due to the characteristics of the internal bias current compensation circuits.

Considering only the noise components, the total noise PSD, S_{vnt}, becomes:

$$S_{vnt} = S_{vn} + R_S^2\left(S_{I1} + S_{I2} - 2S_{I1I2}\right) \tag{1.8}$$

where S_{vn}, S_{I1} and S_{I2} are the PSDs of v_n, i_{n1} and i_{n1}, respectively, while S_{I1I2} is the Fourier transform of the cross correlation function of S_{I1} and S_{I2} (cross power spectrum). In most cases, we can consider that i_{n1} and i_{n2} are uncorrelated, so that $S_{I1I2}=0$ and that $S_{I1}=S_{I2}=S_I$, so that:

$$S_{vnt} = S_{vn} + 2R_S^2 S_I \tag{1.9}$$

Monolithic In-Amps are generally provided of additional terminals as shown in Fig. 1.3. The "GAIN" terminals are used to set the amplifier gain. The most common case is represented by a couple of terminals across which the user has to place a resistor. The value of the resistor sets the gain. In more advanced designs, the amplifier gain can be set through a digital interface, accessible via a serial line.

The REF terminal is used to shift the output voltage by a constant voltage. Indicating with V_{REF} the voltage applied to the REF terminal, the output voltage becomes:

$$V_{out} = G\left(V_{IN+} - V_{IN-}\right) + V_{REF} \tag{1.10}$$

where V_{IN+} and V_{IN-} are the voltages applied to the non-inverting and inverting terminals, respectively, and G is the amplifier gain.

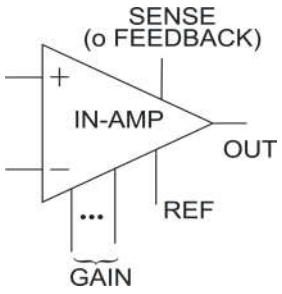

Fig. 1.3. Typical terminals available in monolithic In-Amps.

The SENSE terminal, sometimes indicated with FEEDBACK, is present only in the case that the In-Amp package has enough available pins. It can be used when the amplifier has to be followed by a stage that may introduce high non-linearity or other errors. This is the case of power amplifiers (PA) introduced past the In-Amp, in order to allow it to drive low resistive loads. Connecting the Sense terminal at the output of the PA, includes the latter into the internal feedback loop of the In-Amp. In this configuration, shown in Fig.1.4, the beneficial effects of negative feedback are extended to the PA and the result is a much more precise output voltage. In the case that no additional stages have to be cascaded to the In-Amp, the feedback terminal should be simply shorted to the output terminal.

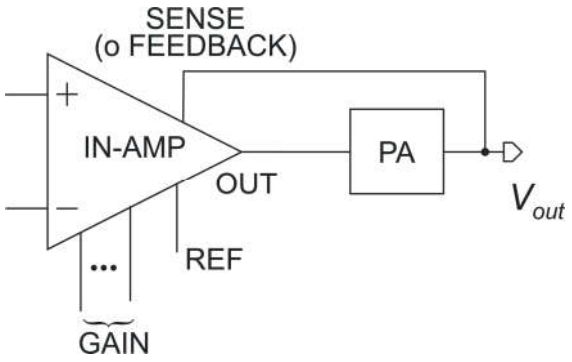

Fig. 1.4. In-Amp connection that exploits the sense terminal to reduce the inaccuracy of the power amplifier (PA).

Other peculiar aspect of monolithic In-Amps is the expression of the offset and noise voltage with two components, namely an input and an output component. This is different, for example, from the case of operational amplifiers, where only input referred quantities are reported. This is due to the fact that the gain of monolithic In-Amps can be varied over a wide range. The typical structure of a monolithic In-Amp is shown in Fig.1.5.

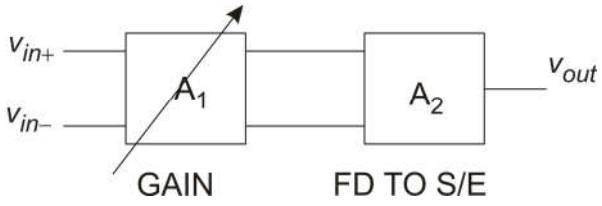

Fig. 1.5. Internal structure of a monolithic In-Amp.

The input stage, typically of fully differential (FD) type, provides the gain A_1. The second stage converts the signal from differential to single-ended (S/E). The gain of the second stage is generally

unity. If we indicate with v_{n1} and v_{n2} the input noise voltages of blocks A_1 and A_2, the total input referred noise voltage v_{nRTI} is given by:

$$v_{nRTI} = v_{n1} + \frac{v_{n2}}{A_1} = v_{n1} + \frac{v_{n2}}{G} \tag{1.11}$$

where we have considered that A_2=1, thus G=A_1. Since the effective input noise voltage depends on gain, which can be varied to meet the application requirement, it is necessary to specify both v_{n1} (called input noise) and v_{n2} (called output noise). The same rule applies to the offset, so that the datasheets specify an input and an output offset. The output voltages (noise and offset) are generally much larger than the input ones, because the second stage is not optimized for noise performances but more for output swing and load driving capabilities. As a result, the performance of monolithic amplifiers in terms of noise and offset significantly improves when high gains are selected.

The in-amp architectures strongly depends on the target applications. Nevertheless, many monolithic in-amps continue to use the "three Op-Amp" configuration shown in Fig.1.6.

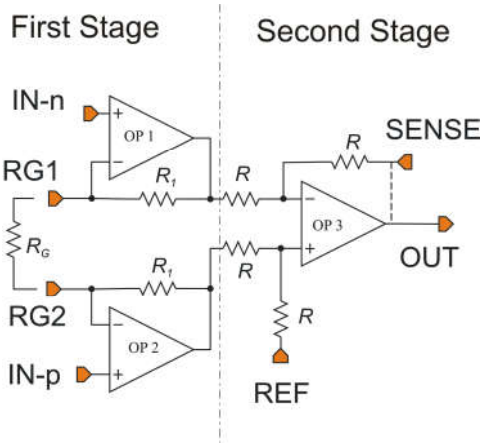

Fig. 1.6. Three-Op-Amp instrumentation amplifier. The integrated circuit pins are indicated in orange.

All components shown in the figures are integrated on the same chip. The only external component is, generally, resistor RG, which is varied to set the gain according to the equation:

$$G = 1 + \frac{2R_1}{R_G} \tag{1.12}$$

Note that the REF terminal is connected to a resistor that affects the transfer function of the second stage. If the source that provides V_{REF} is marked by an output resistance that is not negligible with respect to R, then the amplifier performance (first of all the CMRR) are strongly degraded. Therefore, V_{REF} should be provided by sources with very low output resistance, such as, for example, an op-amp in closed loop configuration. Finally, note that the sense and output terminals can be internally shorted (dashed line) in the case that the sense terminal is not provided.

1.4 Trans-Impedance Amplifier (TIA)

The trans-impedance amplifier is used to read sensors whose output is a current or can be easily converted into a current. Fig. 1.7(left) shows the Norton equivalent voltage of such a sensor: The signal to be read is indicated with i_s, while Z_S is the internal impedance of the signal source (output sensor impedance). The purpose of the TIA is converting the current is into a voltage. This cannot

be effectively accomplished by letting the current i_S flow into a resistance R, by simply connecting the resistance to the sensor output as in Fig.1.7 (right).

Fig. 1.7. Norton equivalent circuit of a source whose output of interest is a current (left); Direct connection of the sensor to a resistance, in order to operate current-to-voltage conversion.

The problem is that the current that actually flows into R is:

$$i_R = \frac{Z_S}{Z_S + R} i_S = \frac{1}{1 + \frac{R}{Z_S}} i_S \tag{1.13}$$

Therefore, i_R coincides with i_S only if $R << |Z_S|$. This is an important drawback, since R cannot be made too small, in order to maintain $v_R = i_R R$ to an acceptable value. Note that $|Z_S|$ always include capacitive components that make it decrease at high frequencies. If the signal has components at relatively high frequencies, $|Z_S|$ is so small that it is not possible to find a satisfactory value for R.

This limitation can be removed using the TIA shown in Fig.1.8. The sensor is represented by the Norton equivalent circuit, characterized by i_s and Z_S. The input impedance of the operational amplifier A is represented by Z_A, while Z is a feedback impedance of accurate value.

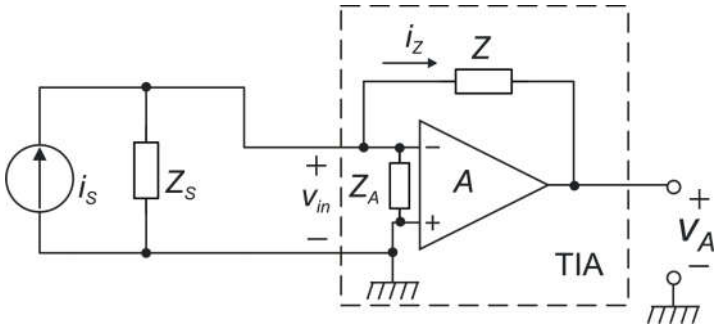

Fig. 1.8. An op-amp based Trans-Impedance Amplifier.

The TIA ideal behavior can be easily found considering that virtual ground is present at the inverting terminal of the Op-Amp. In these conditions, no current flows through Z_A and Z_S, thus the current i_Z that flows into Z coincides with i_S.

Then:

$$v_A = -Z \cdot i_S \tag{1.14}$$

If Z is a pure resistance, the output voltage is proportional to the current i_S. Eq. shows that the ideal sensitivity is $-Z$. In practice, operation of the TIA is marked by a series of non-idealities that have to be considered in the design phase. We will briefly analyze the following issues:

- Finite input impedance due to finite amplifier gain
- Noise

Finite input impedance.

Current i_Z coincides with i_S only if the input impedance of the TIA is zero. As far as virtual ground can be considered valid, the input impedance can actually be considered zero. Unfortunately, virtual ground is an approximation and the real input impedance should be calculated using the diagram in Fig.1.9.

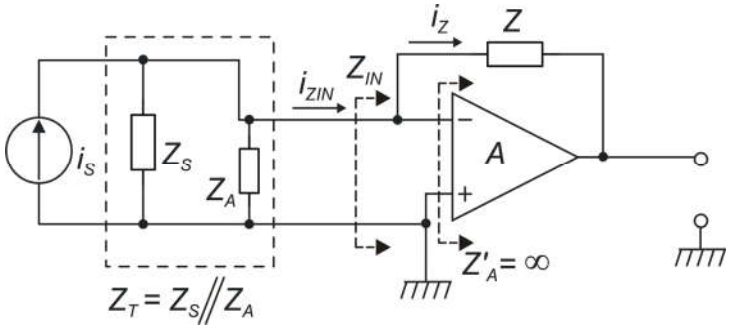

Fig. 1.9. Circuit schematization used to define the input impedance of the TIA (Z_{IN}).

We have separated the input impedance (Z_A) of the Op-Amp from the amplifier itself, so that now block A has infinite input impedance. Z_A, in parallel with Z_S forms the total impedance Z_T. The impedance Z_{IN} is defined as in Fig. 1.9. Since Z_A' is infinite, the whole current i_{ZIN} flows into Z, even if the virtual ground is not present.

Z_{in} can be calculated using the Miller theorem:

$$Z_{IN} = \frac{Z}{1 - K_M} = \frac{Z}{1 + A} \tag{1.15}$$

The frequency dependence of A can be expressed using a dominant pole approximation:

$$A = \frac{A_0}{1 + j\dfrac{f}{f_p}} \tag{1.16}$$

Substituting (1.16) into (1.15) gives:

$$Z_{IN} = Z\frac{1}{1 + \dfrac{A_0}{1 + j\dfrac{f}{f_p}}} = Z\frac{1 + j\dfrac{f}{f_p}}{1 + A_0 + j\dfrac{f}{f_p}} = \frac{Z}{1 + A_0}\frac{1 + j\dfrac{f}{f_p}}{1 + j\dfrac{f}{(1 + A_0)f_p}} \tag{1.17}$$

This expression can be re-written as:

$$Z_{IN} = \frac{Z}{1 + A_0}\frac{1 + j\dfrac{f}{f_p}}{1 + j\dfrac{f}{f_0}} \tag{1.18}$$

where $f_0=f_p(1+A_0) \sim f_0=f_pA_0$ is the gain-bandwidth product (GBW), which, for a dominant pole frequency response, coincides with the unity gain frequency of the operational amplifier.

The dependence of $|Z_{IN}|$ on frequency is represented in Fig.1.10.

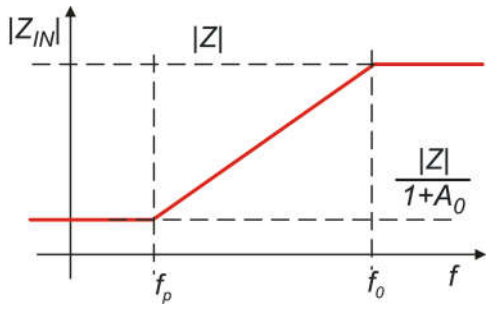

Fig. 1.10. Frequency dependence of Z_{IN} (modulus).

Note that the impedance is reduced by a factor equal to the amplifier DC gain (A_0) only for $f<f_p$. Since f_p is generally of the order of a few tens of Hertz, or, at most, a few hundreds of Hertz, this ideal behavior is generally not applicable to the whole signal bandwidth. For frequencies that approaches f_0, the input impedance tends to Z: at these frequencies the advantage of using an active circuit instead of the simple circuit of Fig.1.7 (right) vanishes. A useful approximation that can be used for frequencies that are between f_P and f_0, and satisfies the conditions:

$$f_P << f << f_0 \tag{1.19}$$

is the following:

$$Z_{IN} = jZ\frac{f}{f_0} \tag{1.20}$$

Once the value of Z_{in} is known, it is possible to estimate the fraction of current I_S that flows into Z. Fig.1.11 shows the equivalent circuit at the input of the TIA, referred to Fig.1.9. The current I_Z is given by:

$$I_Z = I_S\frac{Z_T}{Z_{IN}+Z_T} \tag{1.21}$$

A first order approximation of (1.21) gives:

$$I_Z \cong I_S\left(1-\frac{Z_{IN}}{Z_T}\right) \tag{1.22}$$

Since the ideal case require that $I_Z=I_S$, the relative error (modulus) is given by:

$$\varepsilon_A \cong \left|\frac{Z_{IN}}{Z_T}\right| \tag{1.23}$$

At this point, we have to calculate the amplifier output voltage, V_A. Considering that the amplifier gain is non-infinite, we have to consider also that input voltage, v_{in}, is not zero (imperfect virtual ground):

$$V_A = v_{in} - I_Z Z = \frac{-V_A}{A} - I_Z Z \tag{1.24}$$

Solving (1.24) for V_A, we easily find:

$$V_A = -\frac{I_Z Z}{1+\frac{1}{A}} \cong -I_Z Z\left(1-\frac{1}{A}\right) \tag{1.25}$$

Then we have an additional error term proportional to $1/A$ that adds to the error given by (1.23). It is possible to avoid this error by reading the voltage across the impedance Z by means of a differential amplifier. In this case, the only error source is that given by (1.23).

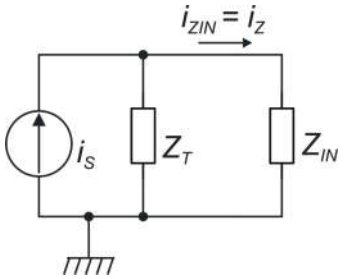

Fig. 1.11. Input equivalent circuit of the TIA, used to estimate the error on the current flowing into the feedback impedance *Z*.

Noise.

The output noise of the TIA can be calculated considering the circuit in Fig.1.12, where the following three noise sources have been indicated:

-) i_n: input current source of the operational amplifier. PSD: $S_{in}(f)$

-) v_n input noise voltage of the operational amplifier. PSD: $S_{vn}(f)$

-) v_{nR}: thermal noise source of the impedance, due to the resistive component. PSD:. $4kT\mathrm{Re}(Z)$

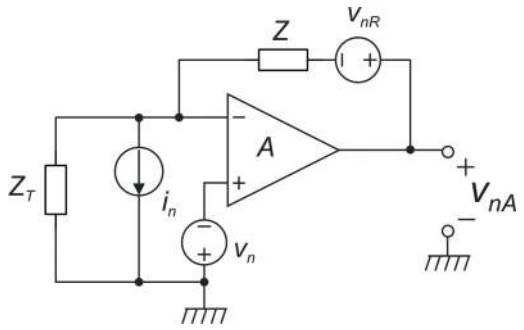

Fig. 1.12. TIA equivalent circuit for noise estimation.

By using the superposition theorem and the input virtual ground principle, it is possible to obtain the following expression for the output noise:

$$v_{An} \cong Z i_n - v_n\left(1+\frac{Z}{Z_T}\right) + v_{nR} \tag{1.26}$$

Since the input signal of TIA is a current, it is convenient to calculate the input referred noise current, $i_{n\text{-}RTI}$. This is accomplished by dividing the output voltage by the transfer function (block sensitivity), namely $-Z$. The following expression is found:

$$i_{n-RTI} \cong -i_n + v_n\left(\frac{1}{Z}+\frac{1}{Z_T}\right)-\frac{v_{nR}}{Z} \tag{1.27}$$

In conclusion, (1.27) indicates that, in order to reduce the noise, the modulus of Z should be chosen as large as possible. For $|Z| \to \infty$, the input noise current reduces to $-i_n+v_n/Z_T$. Unfortunately, a high value of Z increases Z_{IN}, as shown by (1.20). This, in turn, increases the relative error, through (1.23) This error (which is a gain error), is temperature and process sensitive, since Z_{IN} depends on parasitic component and on the amplifier GBW (f_0). This degrades the accuracy of the system. Therefore, a trade-off should be made between noise and gain accuracy.

1.5 Trans-impedance amplifier used as an interface for capacitive sensors

The TIA can be used to read differential capacitive sensors using the circuit in Fig. 1.13.

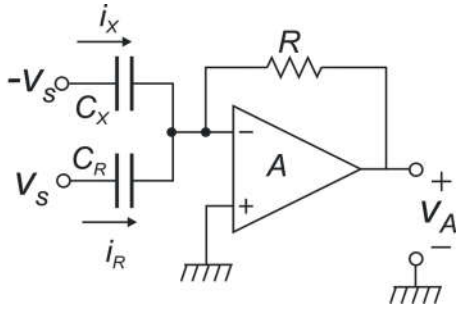

Fig. 1.13. Interface for capacitive sensors based on a TIA.

The sensor is constituted by the two capacitors C_X and C_R. The signal to be read is the difference:

$$\Delta C = C_X - C_R \tag{1.28}$$

Voltage v_s is a sinusoidal waveform given by:

$$v_S(t) = V_{SM}\cos(\omega_S t) \tag{1.29}$$

where $\omega_S=2\pi f_S$ and f_S is the stimulation frequency.

As Fig.1.14 shows, it is possible to derive the Norton equivalent circuit of the sensor, between the common terminal ("h" in Fig.1.14) and ground (node k). The short circuit current i_S and is given by:

$$i_S(t) = C_R\frac{dv_S}{dt} - C_X\frac{dv_S}{dt} = (C_X - C_R)V_{SM}\omega_S\sin(\omega_S t) \tag{1.30}$$

while the equivalent capacitance is:

$$C_S = C_X + C_R \tag{1.31}$$

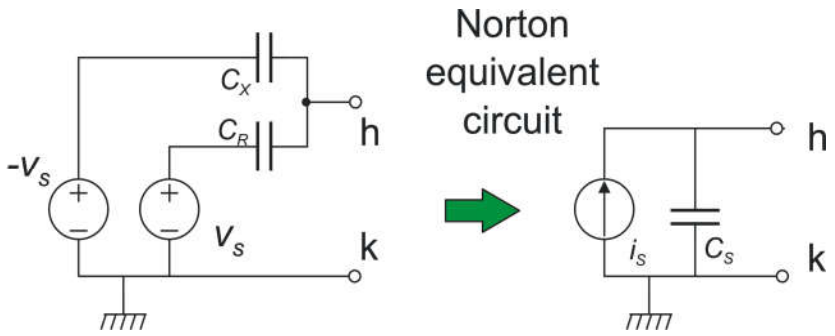

Fig. 1.14. Norton equivalent circuit of the capacitive sensor and the two stimulation sources v_S and $-v_S$.

Then, we can consider the interface of Fig.1.13 as a TIA, with $Z=R$ and the input current source given by the Norton equivalent circuit of Fig.1.14 with the expressions of i_s and C_S given by (1.30) and (1.31).

Therefore, in the ideal case of virtual ground at the TIA input, the following output voltage can be calculated:

$$v_A = -R \cdot i_S(t) = -\Delta C(t) \cdot R V_{SM} \omega_S \sin(\omega_S t) \tag{1.32}$$

Then, the output voltage is the input quantity, $\Delta C(t)$, modulated by a sinusoidal signal at frequency f_S. The target is obtaining a signal which is simply proportional to $\Delta C(t)$, therefore it is necessary to demodulate the signal v_A. We will consider this aspect later. Now let us calculate the gain error due to the finite TIA input impedance and the noise contribution. As far as the gain error is concerned, we consider for simplicity that the contribution given by the $(1+A)^{-1}$ factor in (1.25) is negligible, so that we can consider that the error coincides with the contribution (1.23) , calculated with:

$$Z_T = \frac{1}{j\omega_S C_T} \quad \text{with } C_T = C_S + C_A \tag{1.33}$$

where C_A is the input capacitance of the Op-Amp. In this schematization, we have also considered that the resistive component of Z_A is negligible. The equivalent input impedance of the TIA can be estimated by means of (1.20), with the hypothesis that condition (1.19) holds for f_S. This is reasonable, since f_S should be set as large as possible, to improve noise performances, as it will be shown later. Thus, f_S will be much larger than f_p. The stimulation frequency f_S will also be much lower than f_0, in order to maintain a sufficiently low input impedance Z_{IN}. Then:

$$\varepsilon_A \cong R \frac{f_S}{f_0} \frac{1}{\frac{1}{2\pi f_S C_T}} = \frac{f_S}{f_0} \cdot \frac{f_S}{\frac{1}{2\pi R C_T}} = \frac{f_S}{f_0} \cdot \frac{f_S}{f_\beta} \tag{1.34}$$

where f_β is defined as:

$$f_\beta \equiv \frac{1}{2\pi R C_T} \tag{1.35}$$

In order to keep the error low, it is desirable that f_S is much smaller than both f_0 and f_β. As it will be shown by the noise analysis, this in contrast with resolution specifications.

An expression of the equivalent input current noise can be found by substituting the expression of Z_T, given by (1.33) into (1.27), considering that $Z=R$.

$$i_{n-RTI} \cong -i_n + v_n\left(\frac{1}{R} + j\omega_S C_T\right) - \frac{v_{nR}}{R} \;=\; -i_n + v_n \cdot j\omega_S C_T\left(1 + \frac{1}{j\omega_S C_T R}\right) - \frac{v_{nR}}{R} \tag{1.36}$$

In terms of PSD, equation (25) becomes:

$$S_{I-RTI} \cong S_{In} + S_{Vn}\left(\omega_S C_T\right)^2\left(1 + \frac{1}{\left(\omega_S C_T R\right)^2}\right) + \frac{4kT}{R} \tag{1.37}$$

In order to estimate the error in terms of the input quantity, i.e. the capacitance ΔC, it is necessary to divide the current noise by the sensitivity related to the conversion of ΔC into current i_s. This is not straightforward, since this transformation implies also modulation of the input signal. Therefore, it is necessary also to specify what happens in the demodulation stage, where the signal is brought back to baseband.

The circuit in Fig. 1.15 implements synchronous demodulation: the stimulation waveform v_s and $-v_s$ are obtained from the local oscillator LO. The TIA output signal is demodulated by multiplying it by the local oscillator (LO) signal, after applying a $\pi/2$ phase shift. This is necessary to obtain a signal in-phase with the waveform that modulates ΔC, as shown by (1.32).

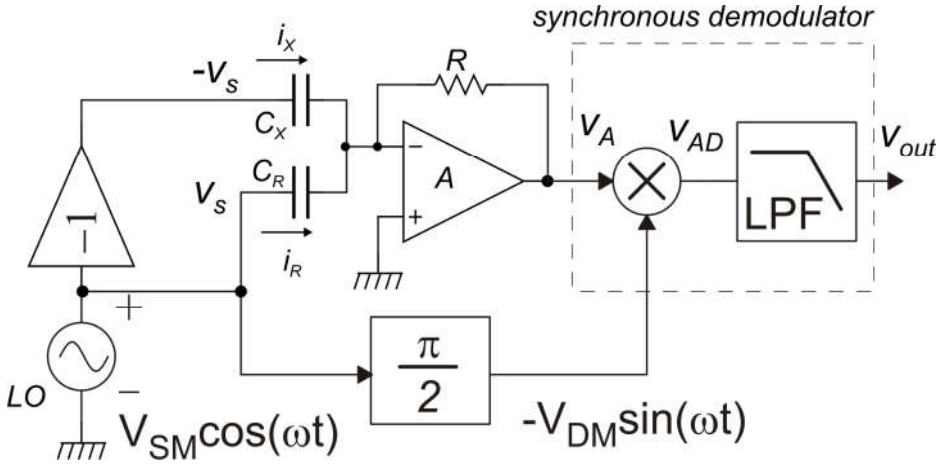

Fig. 1.15. TIA based interface for capacitive sensors, including the synchronous demodulator.

In order to study the circuit performance in terms of signal-to-noise ratio, it is convenient to track all operations made to the signal (and amplifier noise) in the frequency domain. The spectrum of current i_s, derived from (1.30) becomes:

$$I_S(f) = j\frac{V_{SM}\omega_S}{2}\left[\Delta C(f - f_S) - \Delta C(f + f_S)\right] \tag{1.38}$$

The operation described by (1.38) is illustrated in Fig.1.16.

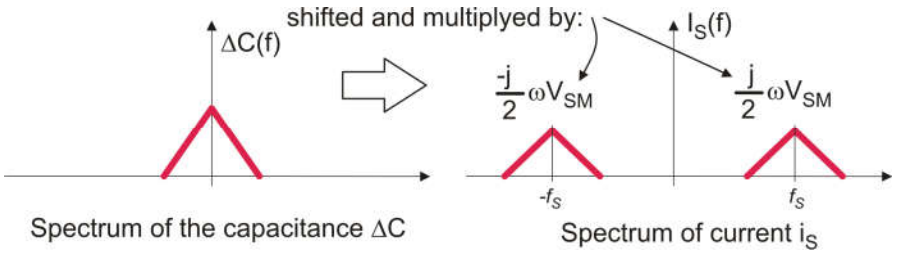

Fig. 1.16. Frequency domain representation of the intrinsic modulation occurring when voltages v_s and $-v_s$ are applied to the sensor in order to obtain a current signal.

Current i_S enters the TIA input together with the equivalent current noise given by (34). The PSD of the current noise is given by (1.37) Considering an ideal operation for the TIA amplifier, the signal and noise currents are both multiplied by the factor $-R$, producing the signal v_A. Demodulation consists in shifting again the spectrum of v_A, across frequencies f_S and $-f_S$. The passages from the current spectrum to the demodulated signal (v_{AD}) spectrum are represented in Fig.1.17. We have indicated the demodulator gain (depending on the multiplier gain) with K_D. The two replicas of the signal give a baseband component and a component at $-2f_S$ and $2f_S$. The baseband components are identical and therefore their sum gives a result that is two times the original contributions. Therefore, the combined effect of the TIA and the demodulator on the signal current produces a multiplication by a $2K_DR$ factor. Considering how the current spectrum is derived from the ΔC one, the baseband spectrum is given by:

$$V_{out}(f) = \Delta C(f)\omega_S V_{SM} R K_D \tag{1.39}$$

The sensitivity is then: $k_S=\omega_S V_{SM} R K_D$. The replicas at frequency $\pm 2f_S$ are eliminated by the LPF.

As far as noise is concerned, we have represented the input noise current PSD in Fig.1.17 with the typical spectrum, characterized by a low frequency region, where flicker dominates and by a high frequency region, were the spectral density is nearly constant. The actual current noise spectrum can be different, since a frequency dependence is present in the equivalent noise PSD given in (1.37). This effect has not been represented in Fig.1.17 , for simplicity.

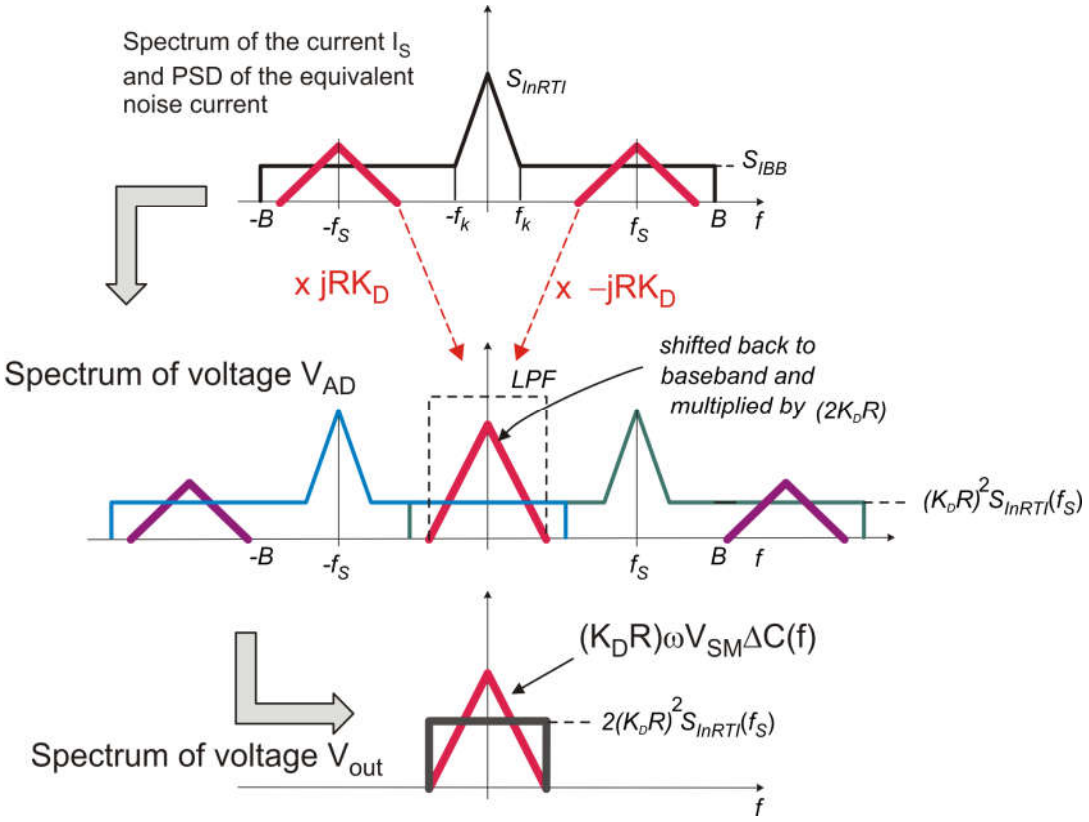

Fig. 1.17. Operation occurring to the signal and noise currents due to operation of the TIA and of the synchronous demodulator. Signal spectrums (Fourier transforms) and noise PSDs are represented in the same plots. Their dimensions are clearly different.

Demodulation brings also a portion of the noise spectrum around f_S back to baseband. Only contribution in the baseband, within the bandwidth of the LPF are to be considered. We can assume that the PSD of the input current noise is nearly constant around f_S. In this condition, the noise density in the baseband is nearly constant and equal to two times the density at f_S, since both contributions from f_S and $-f_S$ add up in the baseband.

As a result, the total noise density in the baseband is given by:

$$S_{Vn-out}(f) = 2\left(R \cdot K_D\right)^2 S_{In-RTI}(f_S) \tag{1.40}$$

This density can be referred to the input quantity, which is the differential capacitance ΔC. From (1.39) we observe that the sensitivity from ΔC to V_{out} is equal to

$$k_{S,Vout} = \omega_S V_{SM} R K_D \tag{1.41}$$

The capacitance noise spectral density is then:

$$S_{\Delta Cn}(f) = \frac{S_{Vout}(f)}{k_{S,Vout}^2} = S_{In-RTI}(f_S)\frac{2}{\left(\omega_S V_{SM}\right)^2} \tag{1.42}$$

Applying (1.42) to (1.37), we finally get:

$$S_{\Delta Cn} \cong 2\left[\frac{S_{In}}{\left(\omega_S V_{SM}\right)^2} + \frac{S_{Vn}}{V_{SM}^2}\left(C_T\right)^2\left(1+\frac{1}{\left(\omega_S C_T R\right)^2}\right) + \frac{4kT}{\left(\omega_S V_{SM}\right)^2 R}\right] \tag{1.43}$$

Equation (1.43) indicates that a way to reduce noise is increasing the working frequency, the feedback resistance R and the stimulation voltage. These three actions are limited by the following counter effects:

-) Increasing the frequency and/or the resistance increases the gain error, as shown by (1.34).

-) The stimulation voltage magnitude is limited by the power supply voltage, which, in turn, is set by the technology and application.

-) Increasing R has also another side-effect: stability. Indeed, resistor R is the feedback element, through which the output voltage is brought back to the input of the Op-Amp. Due to the presence of capacitor C_T, the transfer function from the amplifier output and the inverting input is of low pass type, characterized by a cut-off frequency equal to f_β , given by (1.35). The phase delay introduced by R and C_T, degrades the phase margin of the feedback loop, leading to the risk of instability. The problem is more serious if $f_\beta << f_0$, since the additional phase delay of the feedback network at f_0 gets close to the maximum ($\pi/2$). In order to reduce the phase margin degradation, f_β should be close to f_0, but this implies low R-values, and then, from (1.43), increased noise

Therefore, a trade-off should be sought in order to find the best combination between gain precision noise and phase margin.

1.6 General considerations about switched capacitor circuits

Switch-related random errors: the kT/C noise

This kind of noise occurs any time a voltage is sampled into a capacitor, as shown in Fig.1.18. When the switch S is closed, the voltage V_C is equal to the voltage of the source, indicated with V_0. For simplicity, we will consider that the voltage to be sampled is constant. When the switch opens (sampling instant t_c), the sampled voltage V_C is V_0+V_e, where V_ε is a random error.

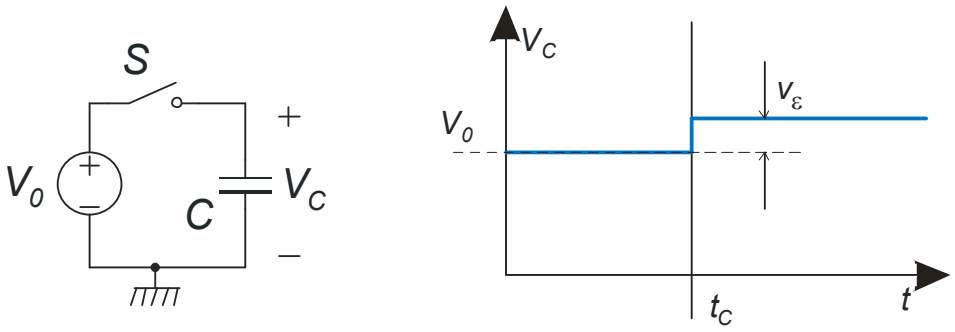

Fig.1.18. The simplest track and hold circuit.

Repeating the sampling operation, as in Fig.1.19, where we have shown also the clock signal that controls the switch, we obtain different error voltages ($v_{\varepsilon 1}$, $v_{\varepsilon 2}$, $v_{\varepsilon 3}$ ...), demonstrating the random nature of the phenomenon.

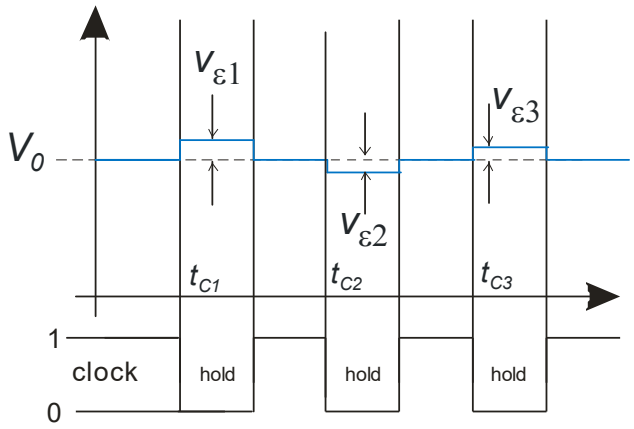

Fig. 1.19. A sequence of track and hold cycles, with the kT/C noise superimposed on the samples.

This error is named "*kT/C*" ("*kT* over *C*") noise, since it is marked by the following property:

$$< v_{\varepsilon}^2 > = \frac{kT}{C} \tag{1.44}$$

where *k* is the Boltzmann constant and *T* the absolute temperature. The distribution of *kT/C* noise is gaussian.

The reason of the existence of the *kT/C* noise is very simple. Voltage V_0 is never really constant, but it is affected by thermal noise, associated to the series resistance of the voltage source. The real circuit, which includes also this resistance (*R*), is shown in Fig.1.20. When the switch is closed, the thermal noise voltage source of resistor *R* is filtered by capacitor *C* that, together with *R*, forms a first order low pass filter. The power spectral density (PSD) of the noise source is *4kTR*, so that the PSD of the noise voltage superimposed to V_C (v_{nc}) is given by:

$$S_{VC} = 4kTR \frac{1}{1+\left(\frac{f}{f_p}\right)^2} \qquad \text{with} \qquad f_p = \frac{1}{2\pi RC} \tag{1.45}$$

The mean square voltage of v_{nc} is given by the integral of the spectral density shown in (10) from 0 to infinity. By simple calculations:

$$< v_{nc}^2 > = \int_0^{\infty} S_{VC}(f)df = \frac{kT}{C} \tag{1.46}$$

Note that the mean square voltage of v_{nc} is independent of *R*. At the sampling instant, switch S opens and the voltage stored in *C* is the last value assumed by V_C, which includes also the v_{nc} noise contribution. Sampling of v_{nc} gives the sequence $v_{\varepsilon i}$ of Fig.1.19. This sequence has the same mean square value of v_{nc}, that is *kT/C*. Fig.1.20 (right) shows what happens when we change the resistance *R*: if *R* is increased, the spectral density at low frequencies proportionally increases, but the pole frequency decreases of the same amount. The result is that the area below the curve (i.e. the integral) does not change. The inverse happens if the resistance is decreased). Therefore the *kT/C* noise depends only on the capacitor value (and, of course, temperature).

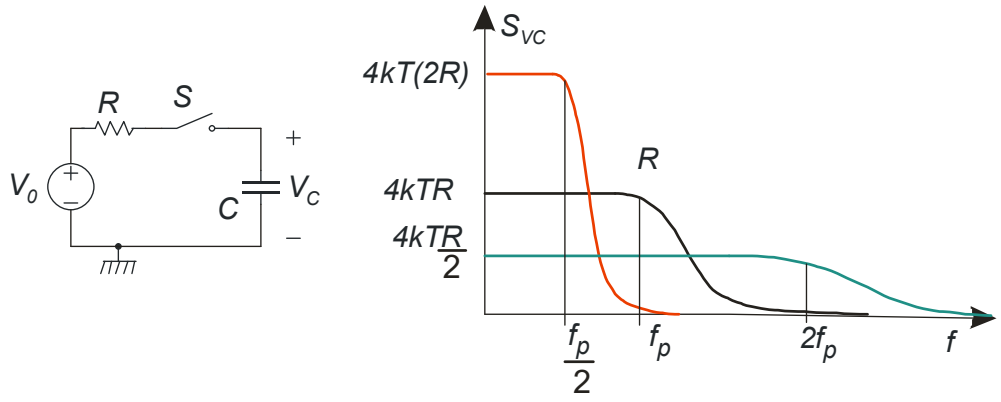

Fig.1.20. Track and hold circuit with series resistance and spectra obtained for different value of the resistance when the switch is colosed (track period).

Four important observations can be made at this point:

- The circuit of Fig.1.20 (left) may represent an equivalent circuit, i.e. a Thevenin equivalent of the network seen from the capacitor terminals of capacitor C. That network can be much more complex than in the simple example of Fig.1.20.
- In many cases, it is interesting to consider the charge that is stored into C after each sampling operation. In particular, we are interested in the charge variations with respect to the average, which is equal to CV_0. We can obtain the charge variations (i.e. the charge noise) by simply multiplying the voltage noise ve by C. In terms of mean square value we have to multiply the mean quare value of the voltage by C2. Then:

$$< Q_\varepsilon^2 > = \frac{kT}{C} C^2 = kTC \tag{1.47}$$

- The *kT/C* noise represents the minimum noise that is present on the sampled voltage. If the voltage to be sampled (V_0) is affected by other sources of noise, *kT/C* noise is combined to the other sources to form the total sampled noise. This occurs, for example, if we are sampling the output noise of an amplifier that is generally accompanied by a large amount of "excess" noise, which is additional noise with respect to the (unavoidable) thermal noise associated to its output resistance. In this case, the spectral densities of the two noise sources cannot be simply added but there is a sort of mixing that is not simple to model. However, the total noise cannot be smaller than the *kT/C* limit.
- One could argue that this phenomenon does not affect ideal voltage sources, as that shown in Fig.1.18, since they do not have an internal resistance that produces thermal noise. Actually, we can consider an ideal source as the limit of a real source when *R* tends to zero. Since for whatever small value of *R* the noise mean square voltage is still *kT/C*, then also the limit should be *kT/C*. Considering Fig.1.20, when *R* tends to zero the PSD gets lower and lower, but its bandwidth (e.g. f_p) extend to infinity, leaving the integral unchanged.

Switch-related systematic errors: the charge-injection phenomenon.

The phenomenon of charge injection is generally related to switches. In an ideal switch, the control signal simply opens and close the connection, with no side effects. In integrated circuits, switches are implemented with MOSFETs: the switch terminals are the source and drain, while the control

signal is applied to the gate. Since parasitic capacitances exist between the gate and both the drain and source, a parasitic interaction between the control signal and the switch terminals occurs. Figure 1.21 shows the equivalence between an ideal switch and the MOSFET-switch. Note that in a MOSFET-switch, as in an ideal switch, the current between the terminals can flow in both directions, thus it is not possible to decide *a priori* which terminal operates as the source and which as the drain. Thus, we have generically indicated with N_1 and N_2 the two terminals of the switch. Capacitive coupling between the control signal (*ck*) and terminals N_1 and N_2 is due to two different kind of capacitances:

- The intrinsic capacitance, due to modulation of the mobile charge in channel, represented by the blue "–" symbols in Fig. 1.21.
- The *extrinsic* capacitance due to the overlap between the gate and the drain / source diffusions, represented by the two capacitors C_{OV1} and C_{OV2} in Fig. 1.21.

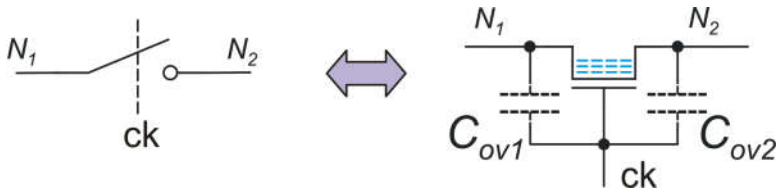

Fig.1.21. The MOSFET switch, with the overlap capacitors and the charge accumulated into the channel in the "on" state.

At any transition of the control signal, the charge accumulated in both types of capacitances undergoes a massive variation, so that a charge flows from the control terminal to the switch terminals N_1 and N_2. The portion of this charge that originates from the channel is generally referred to as "charge injection", while the portion due to the overlap capacitances is generally indicated as "clock feedthrough". The difference between the two phenomena is that the clock feedthrough, being due to almost ideal capacitors, is mainly linear, while the charge accumulated in the channel is a nonlinear function of the voltages. Since the effects are similar, we will simply use the term "charge injection" for both. Fig. 1.22 gives a simple representation of what happens when a switch, initially on, is turned off.

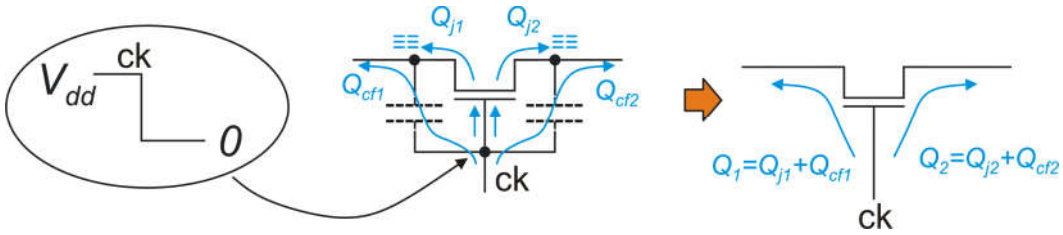

Fig.1.22. Charge transfer during occurring when an n-MOSFET-switch is turned off

The mobile charge accumulated into the channel is ejected into the switch terminals (charges Q_{J1} and Q_{J2}). At the same time, the transition of control voltage *ck* injects the charges Q_{cf1} and Q_{cf2} through the overlap capacitors. The net result, shown on the right side of the figure, is the injection of charges Q_1 and Q_2. For an n-MOSFET, these charges are negative. When the switch is turned on again, we have a similar phenomenon but the injected charges are positive.

The effect of charge injection can be easily understood considering the simple track and hold circuit of Fig. 1.23, which is the same as that of Fig. 1.18, but with the ideal switch replaced by an *n*.MOSFET. As the diagram on the right shows, the control signal passes from the high to the low value at instant t_c. As a consequence of this transition, the switch is turned off and the circuit passes from the track phase, where the output voltage is equal to the input voltage V_S, to the hold phase where the value of V_S sampled at t_c is maintained. The two charges $Q1$ and $Q2$ are injected into the respective switch terminals at the sampling instant. Note that only Q_2 produces an effect, since it is accumulated into capacitor C, altering the sampled value. On the contrary, Q_1 flows into the source V_S producing no effects on the output signal. The effect of charge injection Q_2 on the output voltage is represented in the plot with the variation ΔV_C that, in track and hold circuits is called "pedestal" voltage. The charge injected by MOSFET-switches of minimum size are of the order of a few fC (femto-Coulomb). The error $\Delta V_C = Q_2/C$ is then of the order of a few mV when C is 1 pF.

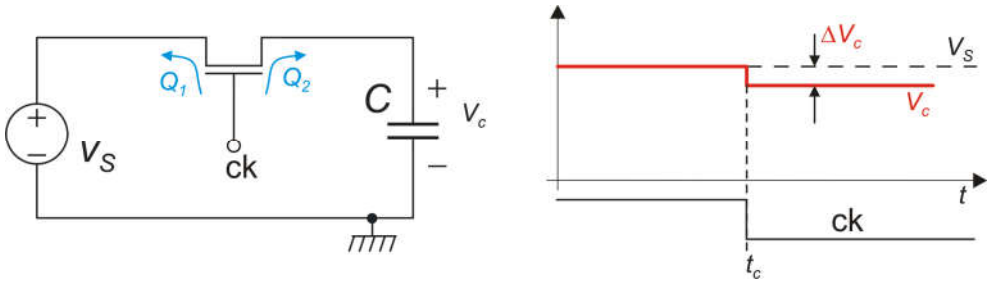

Fig.1.23. Charge transfer during occurring when an n-MOSFET-switch is turned off

In circuits that are more complicatd that the simple example of Fig. 1.23, both charges Q_1 and Q_2 can alter the output signal. Charge injection can be reduced by using switches of minimum area and choosing very large capacitors (e.g. C in Fig. 1.23). Unfortunately, this make the charging transients longer, thus reducing the maximum clock frequency. Furthermore, large capacitances are often not allowed by area occupation constraints. A method that is often used to compensate charge injection is the use of dummy switches, as shown in Fig. 1.24.

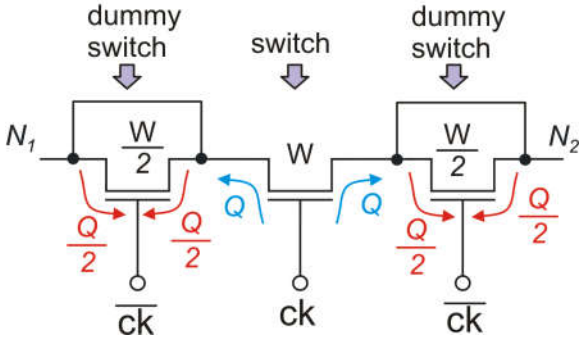

Fig.1.24. Use of dummy switches to compensate charge injection

The dummy switches are clocked with the inverse of the control signal, so that they inject a charge that is opposed to that of the main switch. Their terminals are short-circuited as shown in the figure, to prevent them from affecting the switching function (they have no effect in terms of connection). Note that the two charges injected by a dummy switches into its terminals are collected together onto the same terminal of the main switch. Therefore, to obtain charge compensation, their width

has to be half the main switch width. Note that charge compensation occurs only if the charges injected by the main switch into its two terminals are identical, i.e. Q_1=Q_2 in Fig. 1.23. This generally does not happen, since the ratio between Q_1 and Q_2 depends on several parameters, such as the impedances seen from the two terminals and the clock rise and fall times. Charge injection is difficult to model [1] and empirical recipes are often adopted. Furthermore, mismatches between the main switch and the dummy-switches contribute to prevent a perfect charge compensation. However, the dummy switch approach may contribute to reduce charge injection of at least one order of magnitude. In many cases, as that of Fig. 1.23, the circuit is sensitive to the charge injected only into one of the two switch terminals so that only one dummy switch is required.

The MOSFET-switch must be replaced by a complementary pass-gate (shown in Fig. 1.25), whenever the signals to be passed have a range that may get close to each rail. The pass-gate has the further advantage that its series resistance in the "on" state is more independent of the voltages applied to the switch terminals. The pass gate produces also a partial compensation of the charge injection, since the *n*-MOSFET and *p*-MOSFET that form it are driven by opposite control signals. Unfortunately, the charge present in the channel of the two transistors shows also an opposite dependence on the terminal voltage. For example, if the voltages applied to the terminals are close to ground, the charge in the *n*-MOSFET will be maximum, while the charge in the *p*-MOSFET vanishes. Therefore, charge compensation in a pass-gate cannot be based only on the *p*-*n* complementarity and dummy switch should be added to both the *n* and *p* devices.

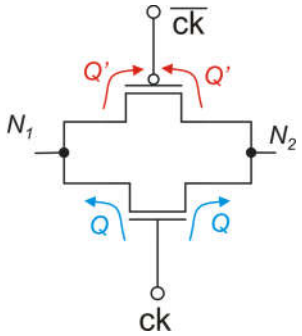

Fig.1.25. Charge injection in a complementary pass-gate: charges Q and Q' generally do not compensate.

Input voltage of Op-Amps in closed loop configuration: the imperfect virtual short-circuit.

The most frequently used switched capacitor circuits are based on combination of capacitors, switches and operational amplifiers. Thanks to the virtual ground enforced at the op-amp input, the charge of selected capacitors can be completely and precisely transferred to other capacitors. A residual voltage across the op-amp inputs (imperfect virtual ground, or imperfect virtual short-circuit), will result in an error in the mentioned charge transfer process. Fig.1.26 shows an operational amplifier connected to a generic feedback network such that:

$$v_{in} = \beta v_O + V_k \tag{1.48}$$

where β and V_k are constant quantities. We suppose that the amplifier response can be expressed as:

$$v_O = A(v_{in} - v_n) \tag{1.49}$$

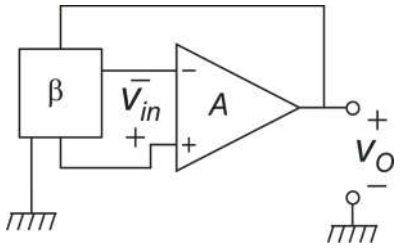

Fig. 1.26. Generic closed loop connection for the Op-Amp..

Substituting the v_O value given by (1.49) into (1.48) gives:

$$v_{in} = \beta A(v_{in} - v_n) + V_k \quad \Rightarrow \quad v_{in} = \frac{-\beta A}{1-\beta A} v_n + \frac{V_k}{1-\beta A} \tag{1.50}$$

If $|\beta A|$ is sufficiently high to make the term $V_k/(1\text{-}\beta A)$ negligible, then:

$$v_{in} \cong v_n \tag{1.51}$$

Note that approximation (1.51) is valid only for frequencies such that $|\beta A| >> 1$. Since βA is generally a low pass function, the factor $-\beta A/(1\text{-}\beta A)$ tends to zero at high frequencies. For this reason, we have to consider than v_{in} is actually a low pass filtered version of the input referred noise v_n. It can be easily shown that, if the frequency response of A is of dominant pole type and β is a negative constant, the cut-off frequency of function $-\beta A/(1\text{-}\beta A)$ is equal to $\beta \times GBW$. For simplicity, in the following part of this section we will consider that (1.51) holds true.

Indicating with v_{in+} and v_{in-} the non-inverting and inverting input terminals, respectively, we have:

$$v_{in-} \cong v_{in+} - v_n \tag{1.52}$$

Four different example of closed loop configurations are shown in Fig.1.27. In the first case, a configuration that is very important for switched capacitors circuits is shown. The amplifier is connected as a unity gain stage (voltage buffer), with the input connected to ground. In this case, (1.52) leads to $v_{in-} = -v_n$. The most interesting case is the fourth (lower right corner). Here, a source (voltage or current) is not connected to the network but V_k may be still different from zero. This is possible because an all-capacitive network retain memory of the previous states.

A general consideration that should be done, is that (1.52) does not hold when V_K is as large as to prevent the amplifier from working in the linear region, where (1.51) is applicable. This occurs, for example, when v_{in}, calculated from (1.50), exceeds the input linearity range of the amplifier. Finally, it should be remembered that the scheme in Fig.1.26 represents a high gain amplifier in closed loop configuration, so that stability should be guaranteed for (1.50) to occur.

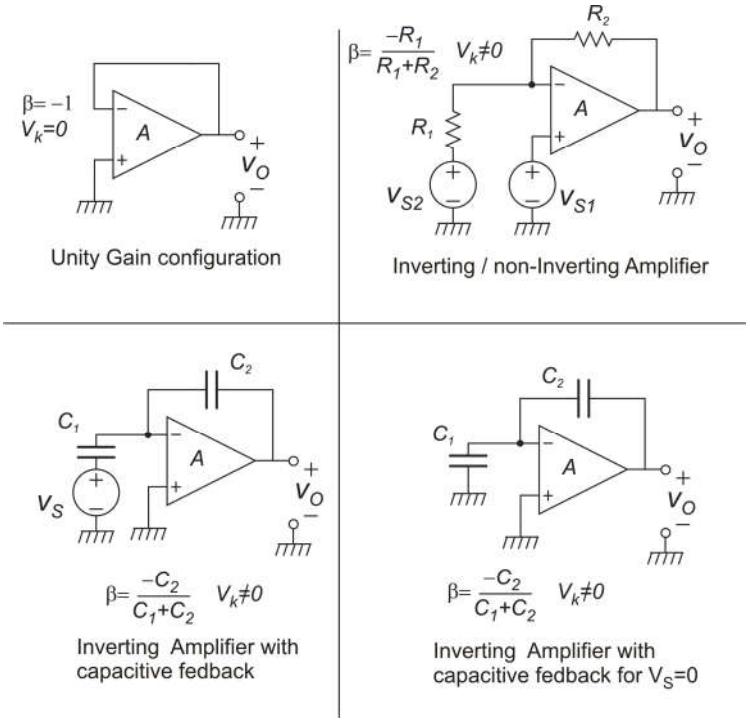

Fig. 1.27. Examples of closed loop configurations that can be represented by the general scheme of Fig.1.26.

Charge transfer through capacitors: conventions.

In switched capacitor circuits, the currents are replaced by their time integral, i.e. charges. Fig.1.28 represents a capacitor experiencing the passage of charge ΔQ in the time interval $[t_i,t_f]$.

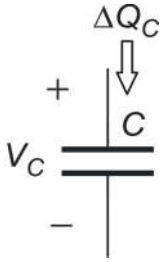

Fig. 1.28. Convention used for the signs of the voltage and charge transfer across a capacitor.

The following relationship occurs between the initial and final voltages, $V_C(t_i)$ and $V_C(t_f)$, respectively:

$$\Delta Q = C\left[V_C(t_f) - V_C(t_i)\right] \;\Rightarrow\; V_C(t_f) = V_C(t_i) + \frac{\Delta Q}{C} \tag{1.53}$$

Fig.1.28 also sets the relationship between the convention used to measure the voltage V_C and the one used to measure the charge passing through the capacitors. Finally, it is important to remind that the first Kirchhoff principle applies to the charge transfers, as in the case of currents.

1.7 Example of capacitive sensor interface based on a switched capacitor charge amplifier.

A simple switched capacitor charge amplifier, used for interfacing capacitive sensors is shown in Fig.1.29. The sensor is represented by capacitors C_X and C_R. The quantity to be sensed is $\Delta C = C_X - C_R$ (differential capacitance). V_R is a constant reference voltage.

The operating cycle is composed of two phases (phase 1 and phase 2). The numbers close to the switches indicate the position of the latter in the two phases. The conventions used to measure the voltages across the three capacitors are also specified in the figure.

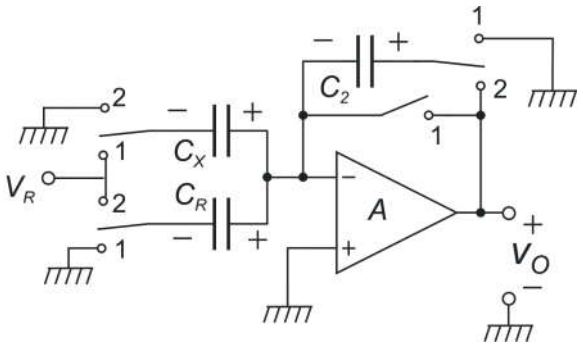

Fig. 1.29. Switched capacitor charge amplifier used to interface a capacitive sensor.

Let us start from phase 1, illustrated in Fig.1.30. Note that the voltage at the non-inverting input is given by (1.52) , with $v_{in+}=0$. Thus: $v_{in-} = -v_n$.

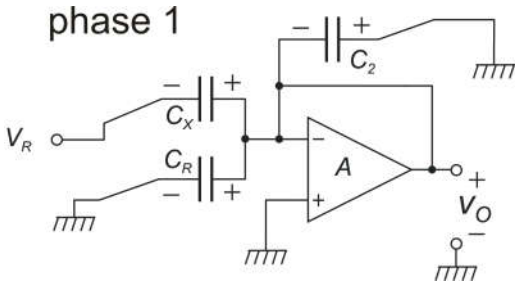

Fig. 1.30. Circuit configuration in phase 1.

In this configuration, the voltage across all capacitors is fixed and given by:

$$\begin{cases} V_{CX}^{(1)} = -v_n^{(1)} - V_R \\ V_{CR}^{(1)} = -v_n^{(1)} \\ V_{C2}^{(1)} = v_n^{(1)} \end{cases} \tag{1.54}$$

Where the superscript "(1)" indicates that these voltages refer to phase 1. Furthermore, the output voltage is given by:

$$v_O^{(1)} = v_{in-}^{(1)} = -v_n^{(1)} \tag{1.55}$$

In the transition between phase 1 and phase 2, the switches changes their position and create new connections. It is useful to consider that the switches do not change position immediately, but stay for a small time into an intermediate position, where they are connected neither to position "1" nor to position "2". In this "intermediate" phase, which will be indicated with the superscript "(i)", all the switches are open. In this way, all capacitors sample the voltage across them at the end of phase 1. The sampling operation introduces a "*kT/C*" error across each capacitor. Therefore, the following voltages are present across the capacitors in the intermediate phase:

$$\begin{cases} V_{CX}^{(i)} = -v_n^{(1)} - V_R + v_{\varepsilon X} \\ V_{CR}^{(i)} = -v_n^{(1)} + v_{\varepsilon R} \\ V_{C2}^{(i)} = v_n^{(1)} + v_{\varepsilon 2} \end{cases} \tag{1.56}$$

where v_{eX}, v_{eR}, v_{e2} are the *kT/C* noise components sampled by C_X, C_R and C_2, respectively. After having sampled the capacitor voltages, the switches close to position 2, starting phase 2. The circuit configuration in phase 2 is shown in Fig.1.31.

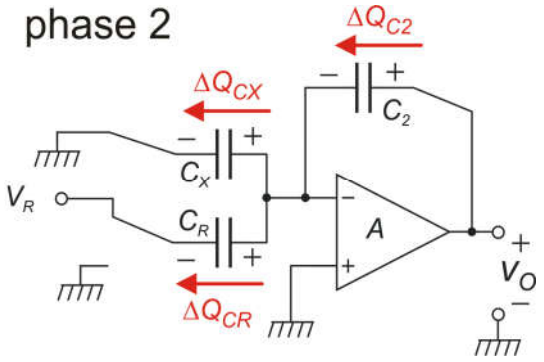

Fig. 1.31. Circuit configuration in phase 2. Charge transfers occurring in the transition between phase 1 and 2 are shown.

Voltages across capacitors C_X and C_R in phase 2 are given by:

$$\begin{cases} V_{CX}^{(2)} = -v_n^{(2)} \\ V_{CR}^{(2)} = -v_n^{(2)} - V_R \end{cases} \tag{1.57}$$

Voltage across C_2 can be calculated considering the total charge ΔQ_{C2} that flows through it in the transition from the intermediate phase, to phase 2:

$$V_{C2}^{(2)} = V_{C2}^{(i)} + \frac{\Delta Q_{C2}}{C_2} \tag{1.58}$$

Considering virtual ground at the amplifier input:

$$\Delta Q_{C2} = \Delta Q_{CX} + \Delta Q_{CR} = C_X\left[V_{CX}^{(2)} - V_{CX}^{(i)}\right] + C_R\left[V_{CR}^{(2)} - V_{CR}^{(i)}\right] \tag{1.59}$$

Substituting the V_{CX} and V_{CR} values given in (1.56) and (1.57) into (1.59) we find:

$$\begin{aligned}\Delta Q_{C2} &= C_X\left[-v_n^{(2)}-(-v_n^{(1)}-V_R+v_{\varepsilon X})\right]+C_R\left[-v_n^{(2)}-V_R-(-v_n^{(1)}+v_{\varepsilon R})\right]= \\ &= (C_X-C_R)V_R-(C_X+C_R)\left(v_n^{(2)}-v_n^{(1)}\right)-C_X v_{\varepsilon X}-C_R v_{\varepsilon R}\end{aligned} \tag{1.60}$$

The output voltage is given by:

$$v_O^{(2)} = -v_n^{(2)} + V_{C2}^{(2)} = -v_n^{(2)} + V_{C2}^{(i)} + \frac{\Delta Q_{C2}}{C_2} \tag{1.61}$$

Using (1.60) for ΔQ_{C2} and (1.56) for $V_{C2}^{(i)}$, we get:

$$v_O^{(2)} = -v_n^{(2)} + v_n^{(1)} + v_{\varepsilon 2} + \frac{(C_X-C_R)V_R}{C_2} - \frac{(C_X+C_R)}{C_2}\left(v_n^{(2)}-v_n^{(1)}\right) - \frac{C_X}{C_2}v_{\varepsilon X} - \frac{C_R}{C_2}v_{\varepsilon R} \tag{1.62}$$

We can then distinguish three components, collected into table 1.3. Note that the sensitivity is proportional voltage V_R. Therefore, a ratiometric behavior can be simply obtained by setting V_R=V_{dd}.

Signal	$\Delta C\frac{V_R}{C_2}$ (sensitivity: $\frac{dv_O}{d(\Delta C)} = \frac{V_R}{C_2}$)
Amplifier noise	$\left[1+\frac{(C_X+C_R)}{C_2}\right]\left(v_n^{(2)}-v_n^{(1)}\right) = \frac{C_X+C_R+C_2}{C_2}\left(v_n^{(2)}-v_n^{(1)}\right)$
kT/C noise	$-v_{\varepsilon 2}+\frac{C_X}{C_2}v_{\varepsilon X}+\frac{C_R}{C_2}v_{\varepsilon R}$

Table 1.3. Signal and noise components of the output voltage.

The noise contributions can be referred to the quantity to be measured, i.e. the differential capacitance ΔC, by dividing them by the sensitivity. The result is shown in table 1.4.

The typical acquisition cycle is shown in Fig.1.32. The switches are controlled by a digital clock signal, indicated with *ck* in the figure. The output signal in phase 1 is given by (1.55). The DC level in this phase is equal to $-v_n$, represented by only the offset component $-V_{io}$, in the figure. In phase 2, the output signal tends to the value given by (1.62), indicated with $V_{OUT\text{-}OK}$ in Fig.1.32. Clearly, a transient is present at the beginning of each phase, before the signal settles to the final value. For this reason, the output signal has to be sampled at the end of phase 2, where the transient is supposed to be finished.

Note that the amplifier noise component is proportional to the difference between two noise samples taken at two different time instants within the measurement cycle. For the discussion above, the two samples are taken at the end of phase 1 and at the end of phase 2, respectively.

Equivalent capacitance noise.	Amplifier contribution	$\frac{C_X+C_R+C_2}{V_R}\left(v_n^{(2)}-v_n^{(1)}\right)$
	kT/C contribution	$-\frac{1}{V_R}\left(C_2 v_{\varepsilon 2}-C_X v_{\varepsilon X}-C_R v_{\varepsilon R}\right)$

Table 1.4. Signal and noise components referred to the input quantity (capacitance Δ*C*).

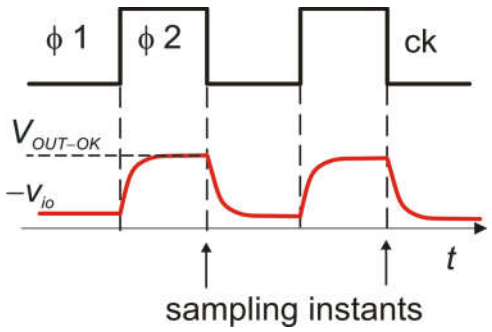

Fig. 1.32. Typical acquisition cycle. Phase 1 and 2 are indicated with ϕ_1 and ϕ_2, respectively.

Any constant components, such as the offset voltage, is cancelled. Noise components at frequency much lower than the clock frequency can be considered nearly constant across a clock period and are then strongly reduced. This corresponds to apply the correlated double sampling technique (CDS) to the amplifier noise. As it will be shown in Chap.2.3, the CDS technique effectively reduces only low frequency noise, but has an adverse impact on the broadband noise components.

1.8 Effect of kT/C noise on the circuit Dynamic Range.

While the amplifier noise can be reduced by a proper design of the amplifier, the *kT*/*C* noise components cannot be avoided with the circuit of Fig.1.29. In this section, we will calculate the Dynamic Range resulting from taking into account only *kT*/C noise components. Clearly, this is an optimistic estimate, since the amplifier noise is generally non-negligible, or, depending on the amplifier design constraints, it can even dominate.

From Table 1.4, considering that noise voltages $v_{\varepsilon X}$, $v_{\varepsilon R}$ and $v_{\varepsilon 2}$ are independent processes, the mean square value of the total input *kT*/*C* noise component is given by:

$$< (\Delta C_n)^2 > = \frac{1}{V_R^2}\left(C_2^2 < (v_{\varepsilon 2})^2 > + C_X^2 < (v_{\varepsilon X})^2 > + C_R^2 < (v_{\varepsilon R})^2 >\right) \tag{1.63}$$

Since:

$$< (v_{\varepsilon 2})^2 > = \frac{kT}{C_2}; \quad < (v_{\varepsilon X})^2 > = \frac{kT}{C_X}; \quad < (v_{\varepsilon R})^2 > = \frac{kT}{C_R} \tag{1.64}$$

with simple algebraic passages, we get:

$$< (\Delta C_n)^2 > = \frac{kT}{V_R^2}(C_2 + C_X + C_R) \tag{1.65}$$

The dynamic range is given by:

$$DR = \frac{\Delta C_{FS}}{\Delta C_{n-pp}} = \frac{\Delta C_{FS}}{4\Delta C_{rms}} = \frac{\Delta C_{FS}}{4\sqrt{\frac{kT}{V_R^2}\left(C_2 + C_X + C_R\right)}} \tag{1.66}$$

where ΔC_{FS} is the full scale value of the input differential capacitance, equal to $\Delta C_{max} - \Delta C_{min}$. With simple passages, we get:

$$DR = \frac{V_R}{4\sqrt{kT/\Delta C_{FS}}}\sqrt{\frac{\Delta C_{FS}}{\left(C_2 + C_X + C_R\right)}} \tag{1.67}$$

Therefore, in order to calculate the DR related to only the kT/C noise contribution, we can first calculate the ratio of the reference voltage V_R and the peak-to-peak kT/C noise calculated for a capacitor of value ΔC_{FS}. This value should then be multiplied by a factor given by the square root of the ratio $\Delta C_{FS}/(C_2+C_X+C_R)$. This factor can be maximized by choosing C_2 much smaller than C_X and C_R, but, since ΔC_{FS} is generally smaller than both C_X and C_R, it will remain smaller than unity.

[1] G. Wegmann, E.A. Vittoz, F. Rahali, “Charge injection in analog MOS Switches”, IEEE Journal of Solid State Circuits, vol. SC-22, No.6, December 1987, pp. 1091-1097.