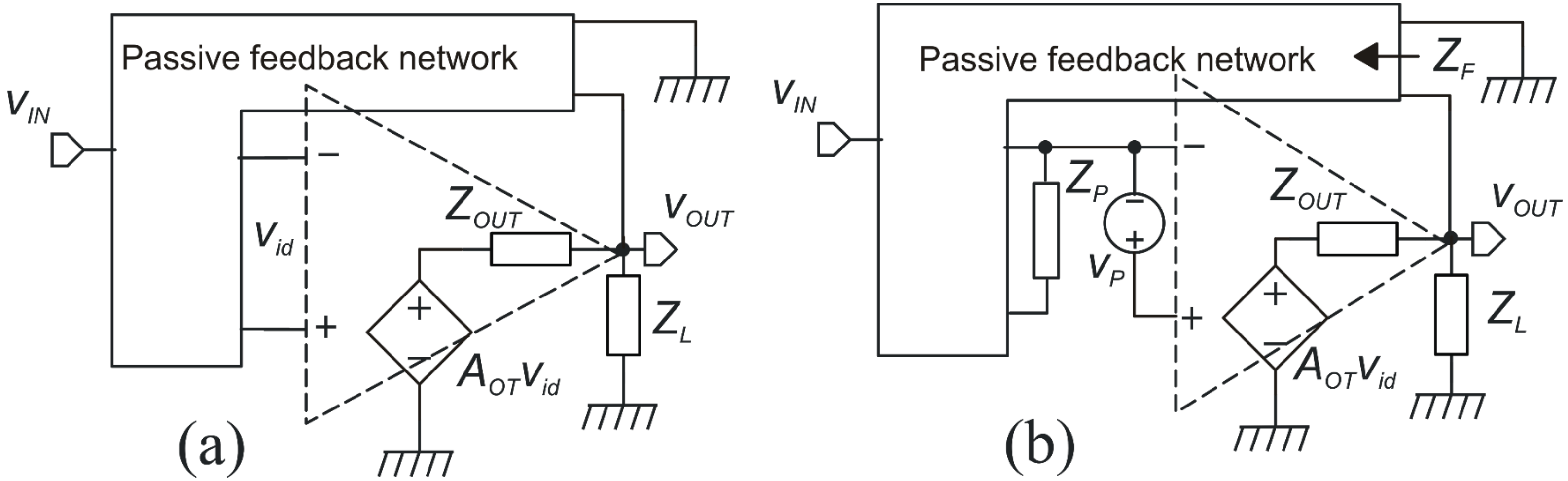
Output stages: specifications

A low output impedance is desirable, but not essential for operational amplifiers since they are designed to be used in closed loop configurations. where negative feedback strongly reduces the output impedance of the overall circuit.



What we need is only that:

$$|\beta A| > \frac{1}{|\varepsilon_{AL}|}$$

where ε_R is the maximum acceptable relative error ….

… and A takes into account of the attenuation caused by the non-negligible output impedance

$$A = \left.\frac{v_{out}}{v_p}\right|_{v_{in}=0} = A_{OT}\frac{Z_L // Z_F}{Z_L // Z_F + Z_{out}}$$

Output stages - characteristics

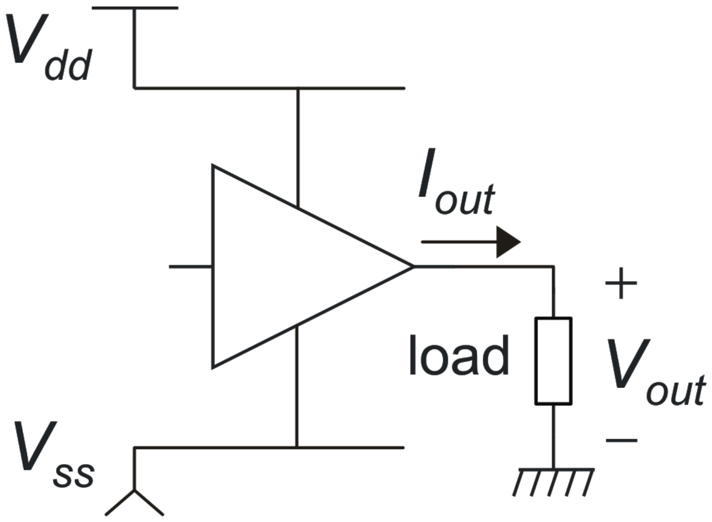
$$-I_{ON-\max} \leq I_{out} \leq I_{OP-\max}$$

Sink   Source

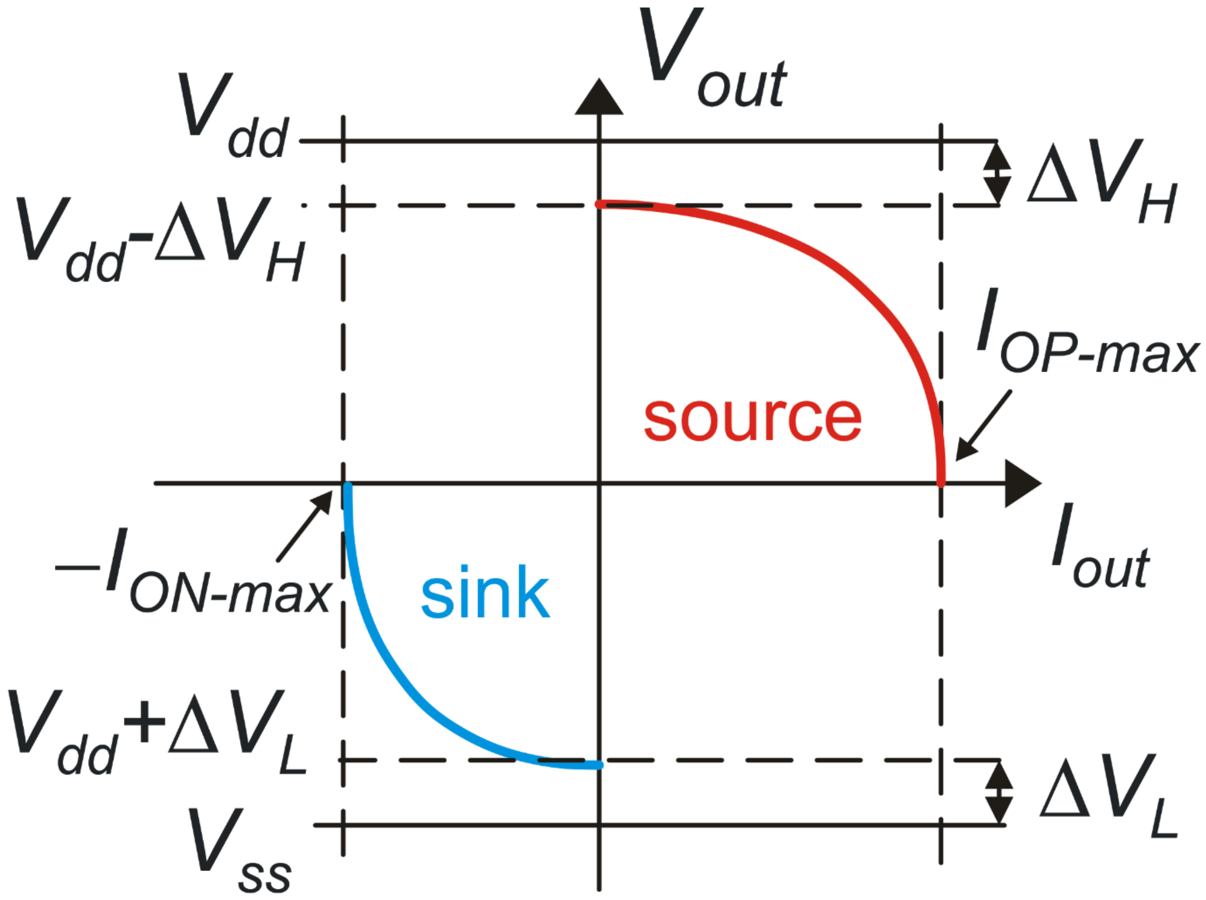
$$V_{out-\max} = V_{dd} - \Delta V_H \;\; ; \;\; V_{out-\min} = V_{ss} + \Delta V_L$$

Output stages: main specifications

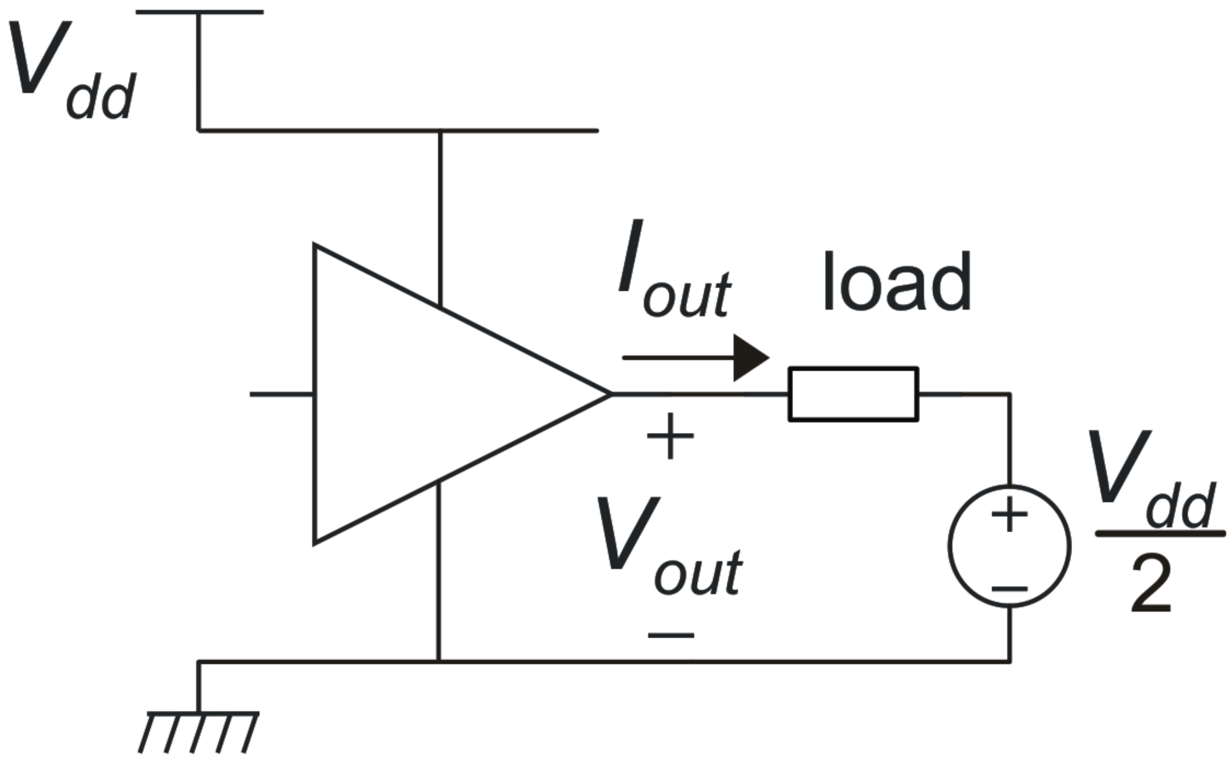
The real specifications concern the maximum output currents and voltages.



Dual power supply

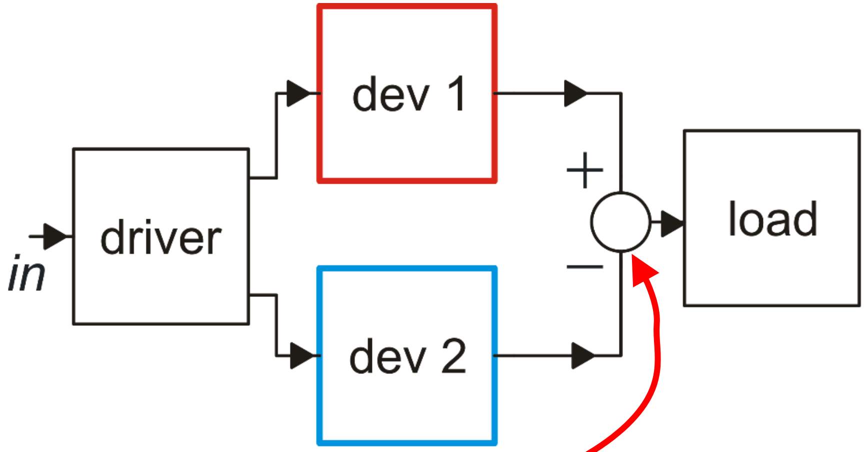


Single supply case

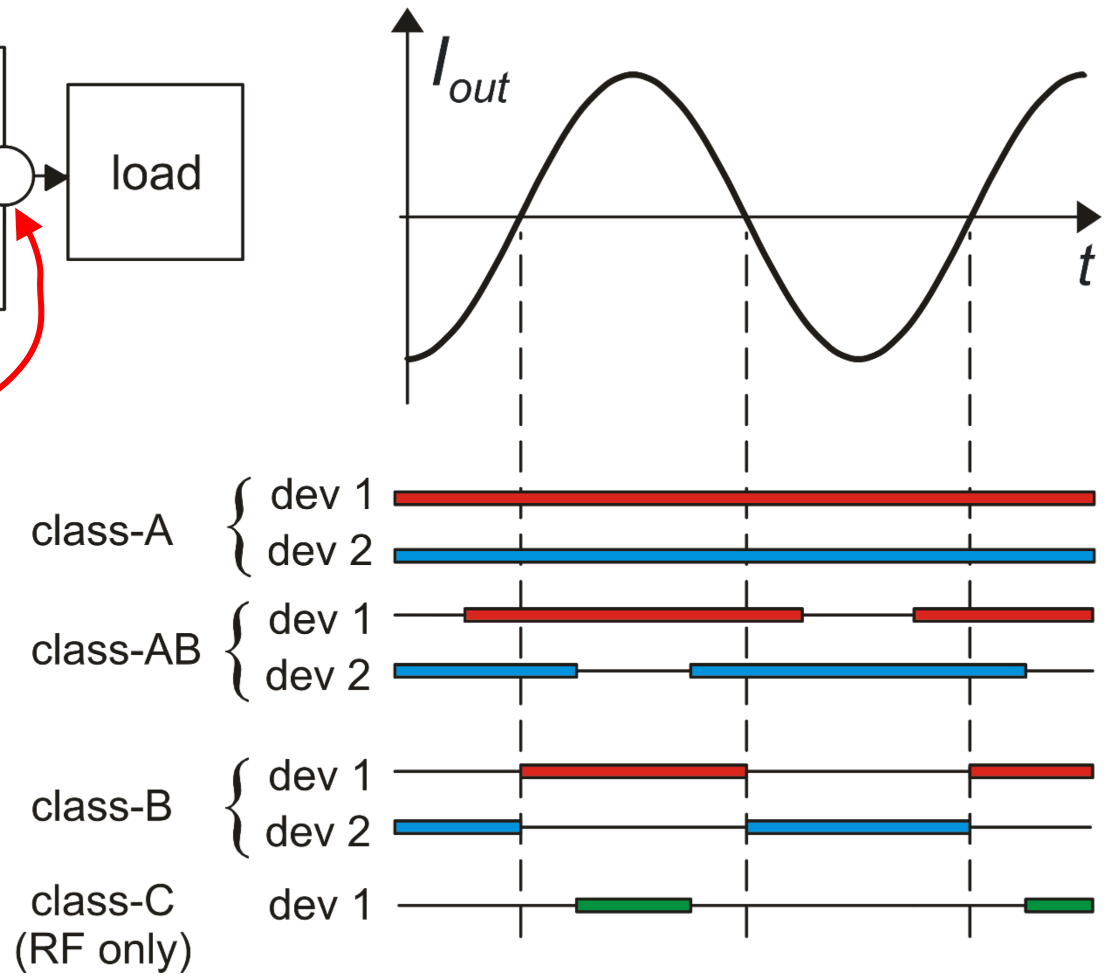


Single power supply

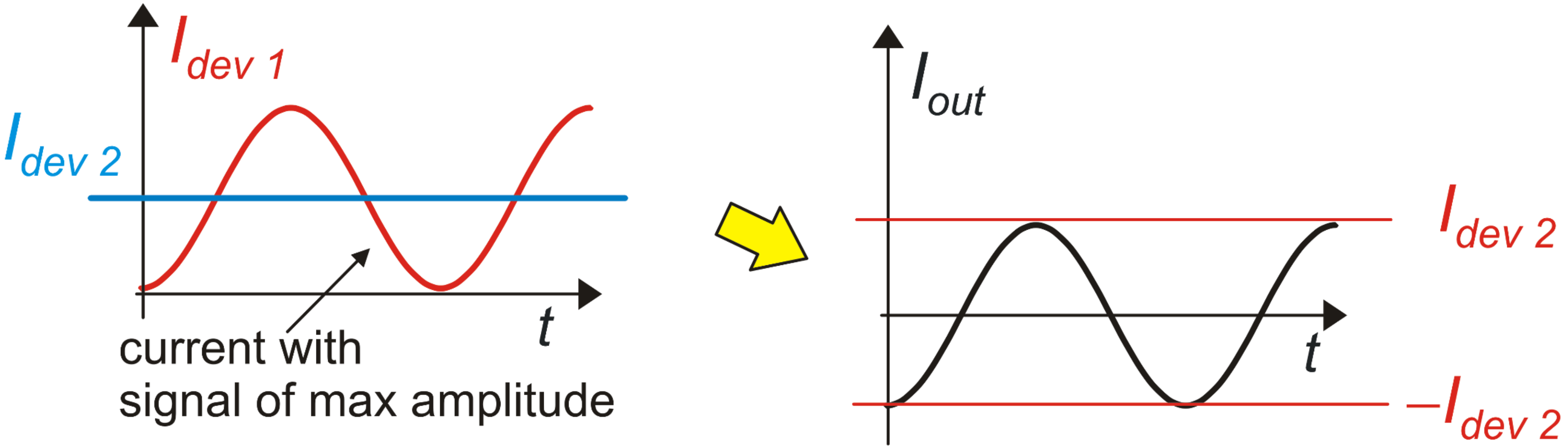
Oputput stage classes



By subtracting two unipolar currents, we obtain a bi-directional output current

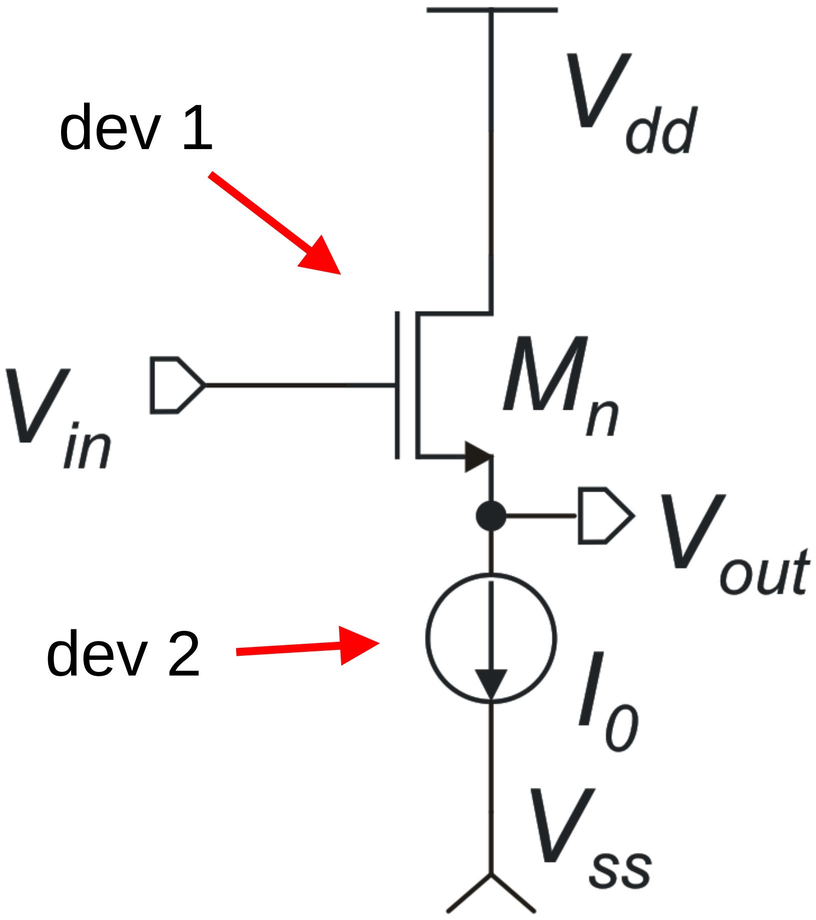


Low power efficiency of class A output stages



The maximum symmetrical current coincides with the Idev 2, which is a constant bias current.
Therefore, the maximum output current is smaller of the quiescent current absorption.

Class – A source followers



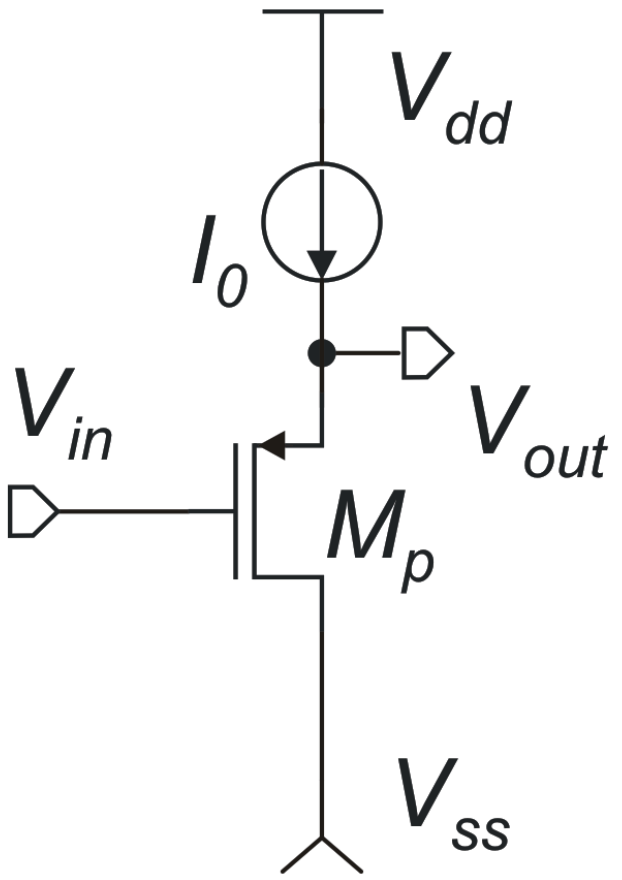
Limits:

$$V_{out} = V_{in} - V_{GS}$$

$$V_{out} < V_{dd} - \underline{V_{GS}}$$

Margin to Vdd
(too large for typical supply voltages used in modern CMOS processes)

p-type source follower

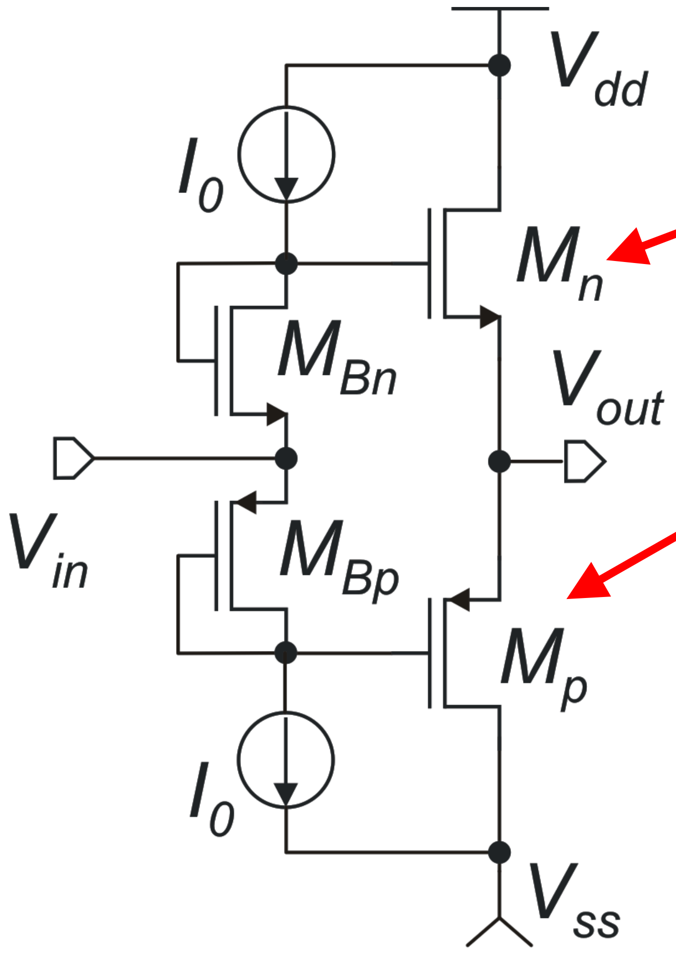


$$V_{out} = V_{in} + |V_{GS}|$$

$$V_{out} > V_{ss} + |V_{GS}|$$

Margin to Vss
(too large for typical supply voltages used in modern CMOS processes)

Class AB – push pull source follower

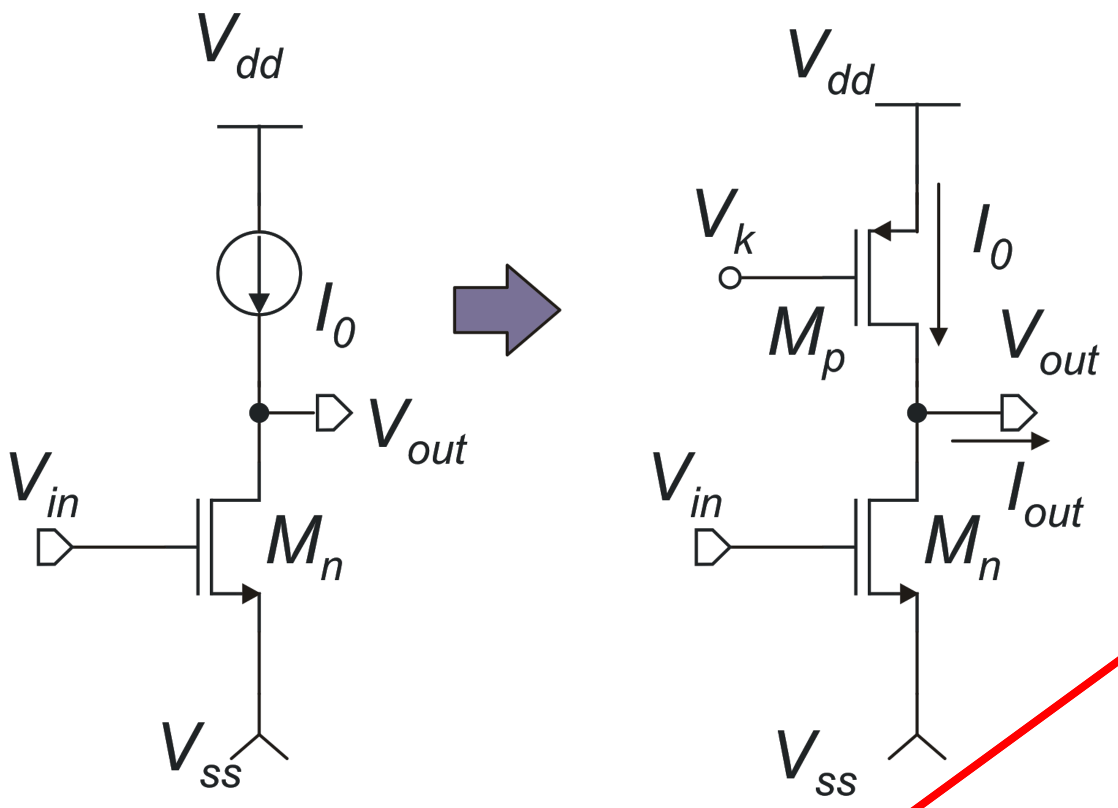


$$V_{out} < V_{dd} - V_{GS}$$

$$V_{out} > V_{ss} + |V_{GS}|$$

Practically useless for the low supply voltages used in modern analog circuits: $V_{dd} - V_{ss} < 3.3$ V

Common source output stages: class A case



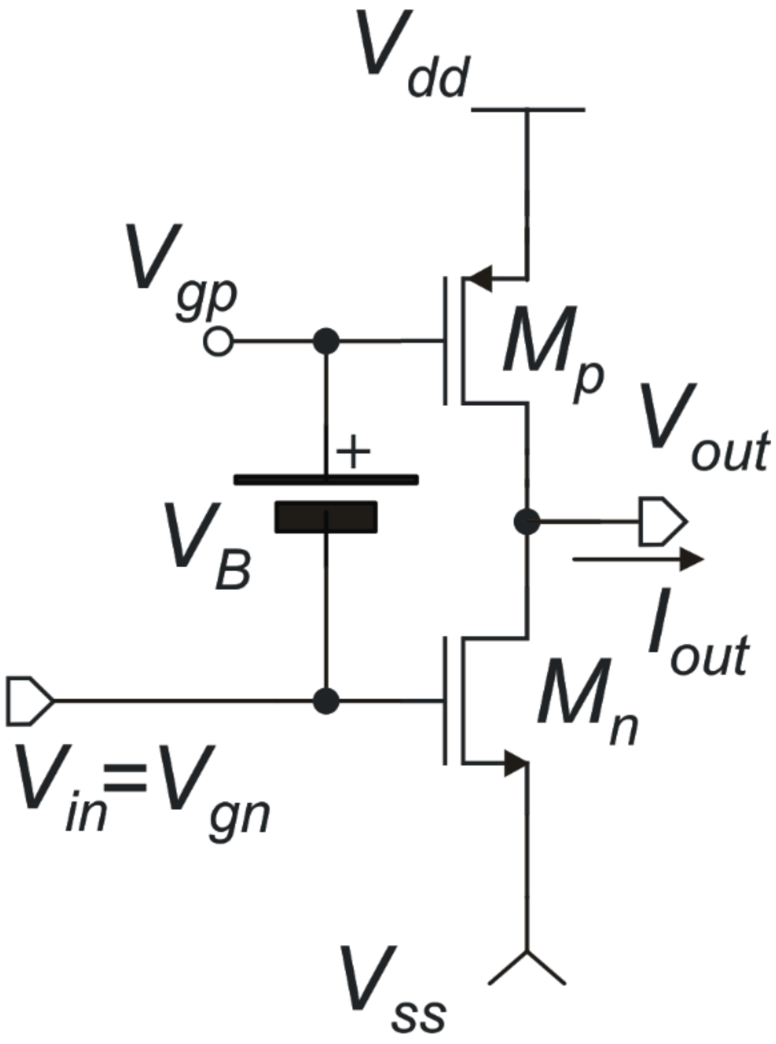
Margins to the rails are now only a V_{DSAT}, which is much smaller than a V_{GS}.

The common source output stage has a practically rail-to-rail output swing

$$V_{ss} + \left|V_{DSATp}\right| < V_{out} < V_{dd} - V_{DSATn}$$

But … it is a class A stage and $I_{OP\text{-}max}=I_0$.

Class –AB common source output stage

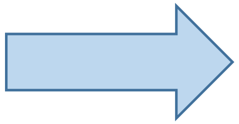


The difference from the class-A common source output stage is the fact that also Mp is driven by the input signal. This is obtained by driving the gate of Mp with a shifted version of the input signal. The voltage shifter is represented by battery V_B. For obvious reasons, a real battery is not used and a voltage shifter is used. There are several different way to implement the voltage shifter to be used to replace the battery V_B.

Depending on the architecture of the preceding stage and of the voltage shifter, the VGS of Mp and Mn can reach a maximum value that, together with the device size, determine the maximum output current. In particular:

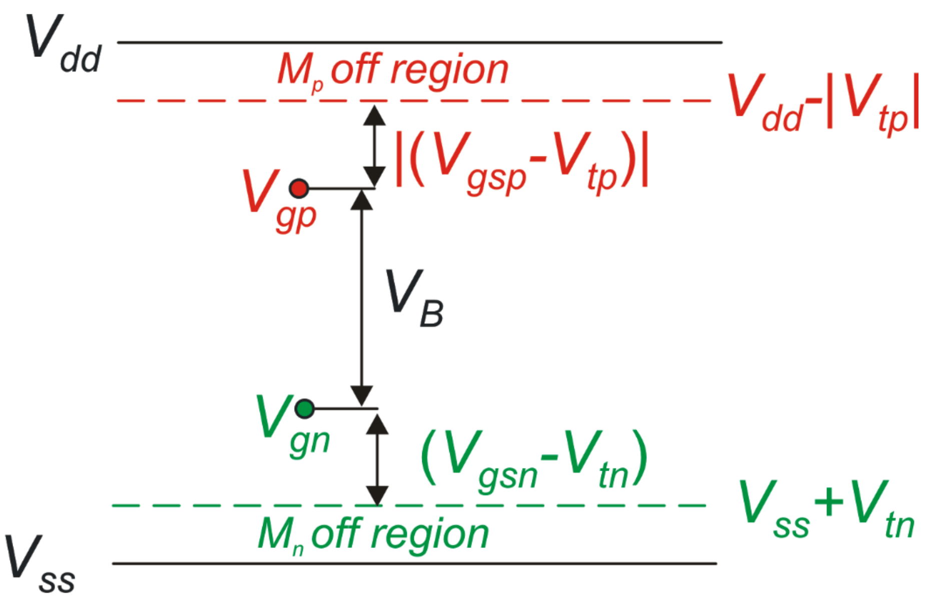
$$I_{ON-\max} = \frac{\beta_n}{2}\left(V_{GSn-\max} - V_{tn}\right)^2$$

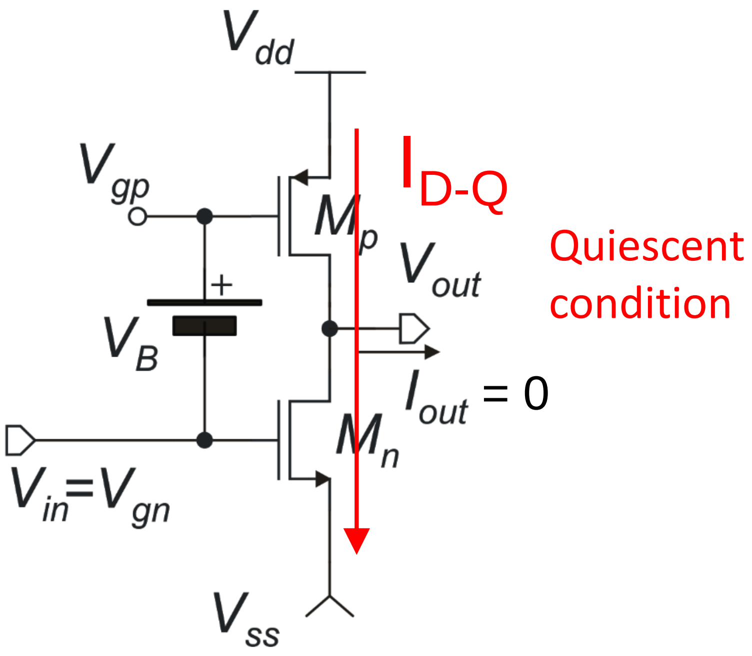
$$I_{OP-\max} = \frac{\beta_p}{2}\left(\left|V_{GSp-\max}\right| - \left|V_{tp}\right|\right)^2$$



β_p, β_n

Class-AB common source: Quiescent current



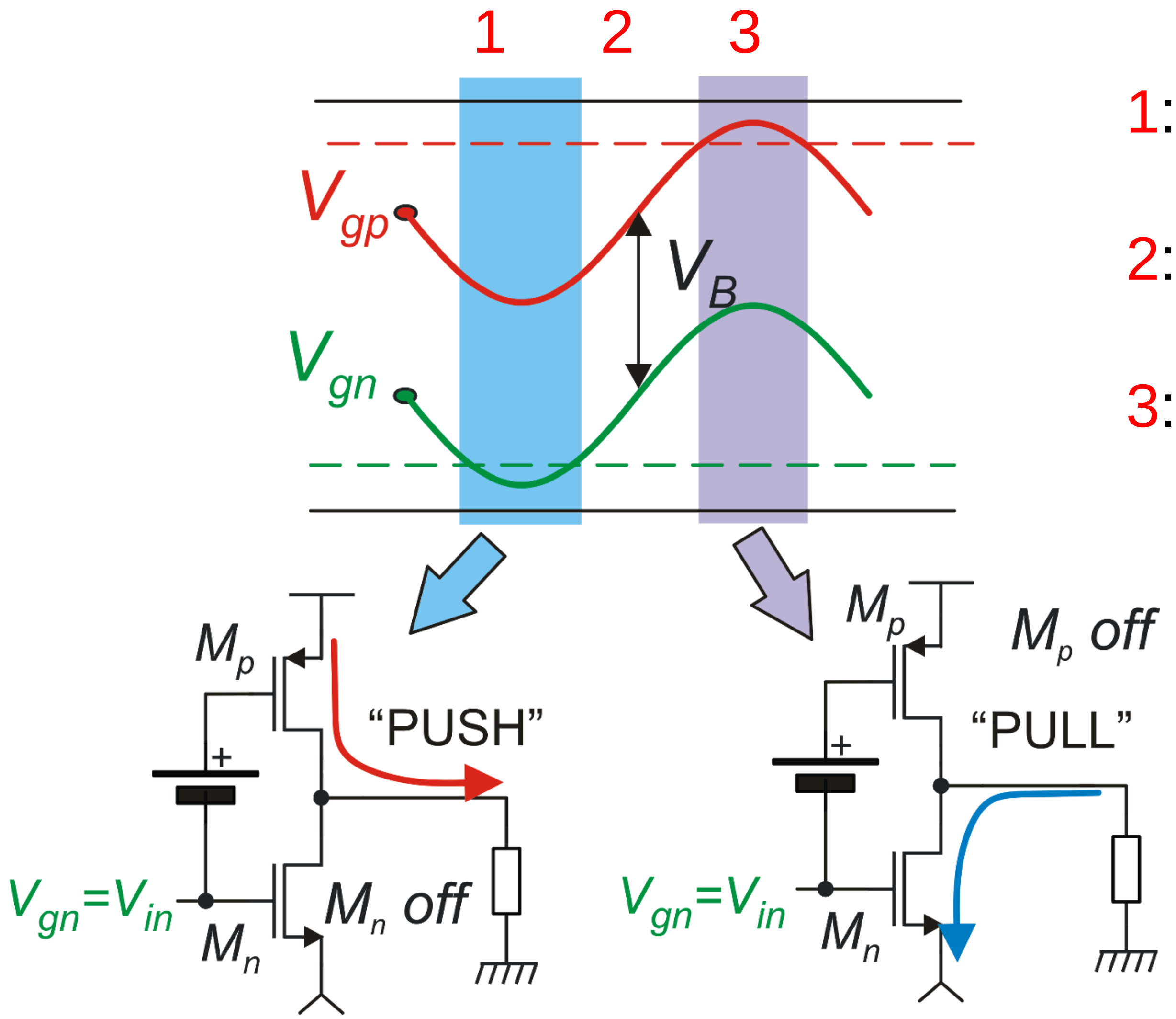


$$I_{DN-Q} = \frac{\beta_n}{2}\left(V_{GSn-Q} - V_{tn}\right)^2$$

$$I_{DP-Q} = \frac{\beta_p}{2}\left(\left|V_{GSp-Q}\right| - \left|V_{tp}\right|\right)^2$$

$I_{DN-Q} = I_{DP-Q} \equiv I_{D-Q}$ to have a zero output current in quiescent conditions. Since β_n and β_p have been already determined to set the maximum output currents, here, once the value of I_{DQ} has been chosen, we find the quiescent values of V_{GSn} and V_{GSp}.

Class-AB common source stage: large signals



1: M_n off, M_p on

2: Both M_p and M_n are on

3: M_n on, M_p off

Note: for small signals the stage remains in region 2, then M_n and M_p do not turn off during the whole signal cycle.