1 Fully differential circuits: system-level view

1.1 Fully differential systems: motivations.

Figure 1.1 illustrates the difference between a unipolar and fully differential architecture. In a unipolar system, signals consists in voltages between single nodes and ground. Ground is a special node of the circuit, which coincides with one of the power rails (i.e. one of the terminals of the power supply). Each input and output port of the various blocks coincides with a single terminal.

In a fully differential circuit, signals are represented by voltage differences between couples of nodes, none of which is ground. Clearly, a ground is still necessary for conveying the supply currents of all blocks. Thus, as usual, for each node pair we can define a differential voltage (which carries the information) and a common mode voltage. In single supply systems, a non-zero dc component is generally required for the common mode voltage, in order to meet the input common mode range of the blocks and maximize the signal swings.

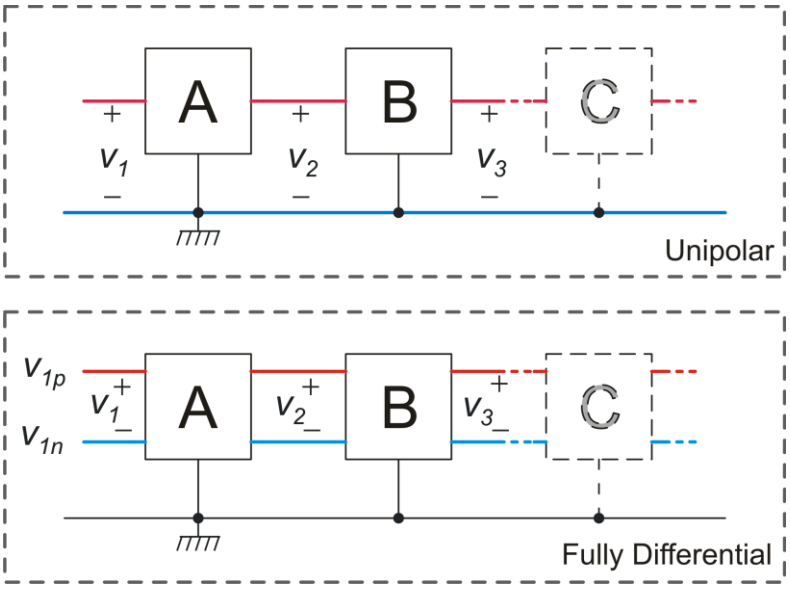

Fig.1.1. Unipolar (top) and fully differential (bottom) architectures.

In a fully differential architecture, all inputs and outputs consists of a couple of terminals. For example, an amplifier will have two input terminals and two output terminals.

The advantages of fully differential architectures can be divided into three categories:

1) Excellent immunity to interferences
2) Wider output ranges
3) Improved linearity

Immunity to interferences.

We will analyze four different causes of interference:

a) Non-uniform ground voltage
b) Non-uniform V_{dd} voltage
c) Capacitive coupling
d) Substrate noise

The problem deriving from non-uniform ground voltage is illustrated by Fig. 1.2 (a), showing a unipolar system. Impedance Z_G is due to unavoidable distributed inductances and resistances of the ground line. The supply current of block B and other blocks, not shown in the picture for simplicity, flows in the ground line, producing the voltage drop $Z_G I_G$ across the ground line impedance.

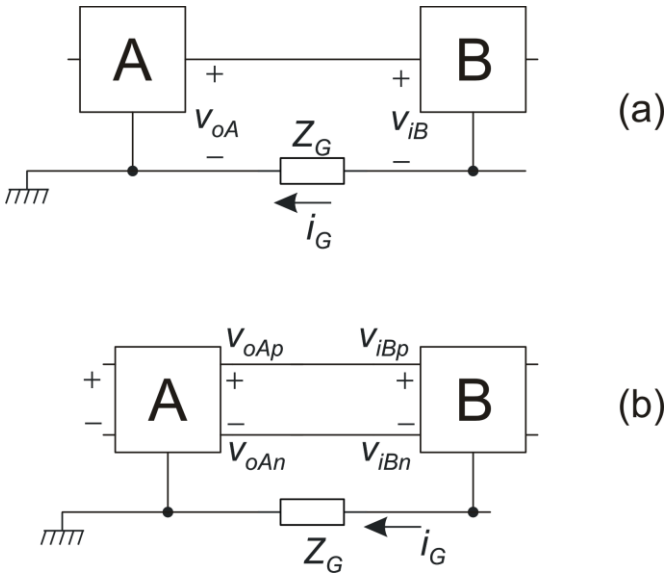

Fig.1.2. Non-uniform ground voltage for a unipolar (a) and differential (b) architecture.

As a result, block B receive an input voltage given by:

$$V_{iB} = V_{oA} - Z_G I_G \tag{1.1}$$

while, it was expected to receive only V_{oA}. In other words, the ground assumes different potentials across the system due to the current that flows through it. The blocks that form the system are connected to ground line at different points, so that they sense different ground potentials. In a unipolar system, these potential differences are summed up to the signal, as (1.1) clearly shows. This problem can be particularly serious when the ground current includes high frequency components. Examples of

blocks that inject high frequency components into the ground line are oscillators and digital sub-systems, which, due to continuous commutations, absorb an impulsive current through the power rails. This is always the case in mixed signal integrated circuits.

In a differential system, the potential differences present on the ground line affect the two voltages that form the signal in the same way, so that they produce only a common mode disturbance. On the other hand, the voltage difference is not altered, since no current flows through the lines that carry the signal and thus no voltage drop is produced across them. Clearly, all blocks should be marked by a good CMMR, which means that the magnitude of the transfer function from the input common mode to the output differential mode should be as small as possible.

Since the supply current flows also in the V_{dd} line, the supply voltage will also be non-uniform across the chip and subjected to impulsive variations. Furthermore, even if the V_{dd} could be uniformly distributed across the chip, its value would vary with time, as the result of the voltage drop occurring across the bonding wire that connects the V_{dd} pad to the case terminal. This voltage drop is, again, proportional to the current absorbed by the various blocks present in the chip and, as a result, may include high frequency components. The extent by which a variable $\underline{V_{dd}}$ affects the output of a giveb sub-circuit depends on its PSSR. Again, thank to symmetry, a V_{dd} variation produces mostly common mode errors in the output terminals of a fully differential block. As a result, the PSRR of fully differential systems is much better than the PMMR of unipolar systems. This is particularly notable at high frequencies, where parasitic components (mainly capacitances) cause a strong degradation of the PSSR of unipolar circuits. On the other hand, also parasitic components are symmetric in a fully differential circuit, so that the high PSSR is maintained even at high frequencies. Symmetry is also the reason of the excellent CMRR of fully differential circuits. In an ideal circuit, symmetry is perfect, leading to infinite CMRR and PSSR. In a real circuit, matching errors will introduce small asymmetries resulting in finite CMRR and PSSR. However, since matching errors are generally very small in integrated circuits, very high CMRR and PSSR can be easily obtained with fully differential architectures.

In a mixed signal integrated circuit, a method to reduce interferences from non-uniform ground and V_{dd} potentials can be the use of different ground and V_{dd} conductors for the analog (sensitive) and digital (noisy) sub-systems, as shown in Fig. 1.3. These strategies are essential in unipolar architectures, due to their higher sensitivity to ground and V_{dd} non-uniformity. In a fully differential circuit, such techniques can be used to reduce coupling of disturbances between analog and digital circuits even further.

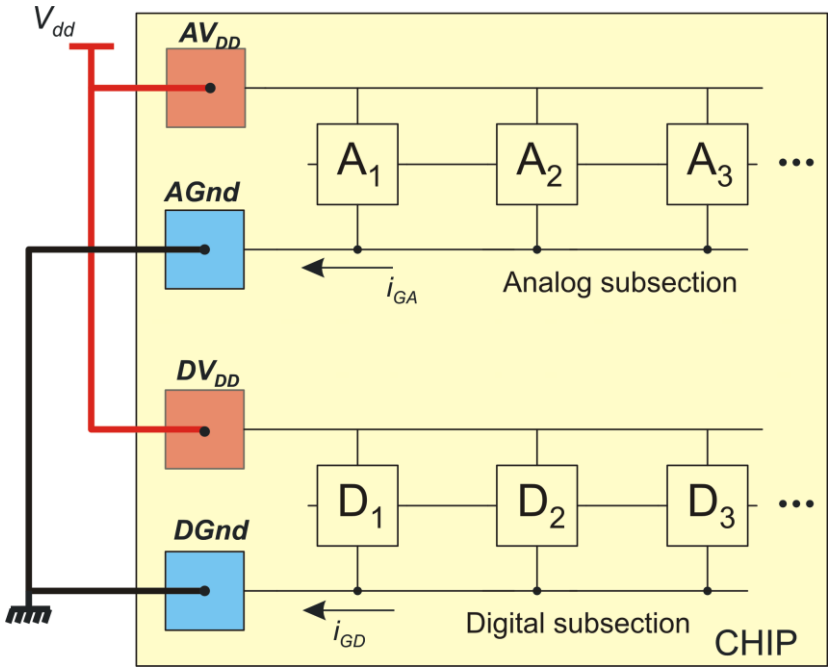

Fig.1.3. Typical architecture of a mixed signal integrated circuit, with separate ground and V_{dd} rails and pads.

Connection between the two power-line distributions can be made in a single point of the chip, so that the supply current of the digital system does not flow into the rails of the analog ones. A further improvement can be using different pads for the analog and digital rails and make the connections out of the chip, in a convenient place of the printed circuit board (PCB) that hosts the integrated circuit. Indeed, many mixed signal integrated circuits have distinct pins for both the analog and digital ground and V_{dd}, as shown in Fig. 1.3.

The case of interferences deriving from capacitive coupling is shown in Fig. 1.4 (a) for the unipolar architecture. The disturbing signal V_D, typically with high frequency components, is applied to a line (depicted in red in the figure), which is coupled with the signal line through capacitance C_a. The signal line has a path to ground through the output impedance (Z_{oA}) of the transmitting block (A) and the input impedance (Z_{iB}) of the receiving block (B). The interference picked-up by the signal line is given by:

$$V_{iB} = V_D \frac{Z_{oA} \| Z_{iB}}{Z_{oA} \| Z_{iB} + Z_a} = V_D \frac{1}{1 + \dfrac{Z_a}{Z_{oA} \| Z_{iB}}} \quad \text{with} \quad Z_a = \frac{1}{j\omega C_a} \tag{1.2}$$

where Z_a is the impedance of capacitor C_a at the frequency of the interference source V_D. Clearly, for a given coupling impedance Z_a, the interference will be smaller if the parallel of Z_{oA} and Z_{iB} is much smaller than Z_a. In many cases, it is not possible to guarantee that this occurs. On the other hand, due to its symmetry property, a fully differential circuit is much more immune also to this type of interference, since the nodes of the pair that carries the differential signal are affected in a similar way, so that the disturbance is mainly a common mode signal. Clearly, the two wires of the pairs cannot be coincident, thus they will exhibit different coupling capacitances towards the interfering line. As a result, a small

differential component can still be produced. To avoid this, it is possible to improve the symmetry by replicating the interfering line on both sides of the circuit, as shown in Fig. 1.4 (b).

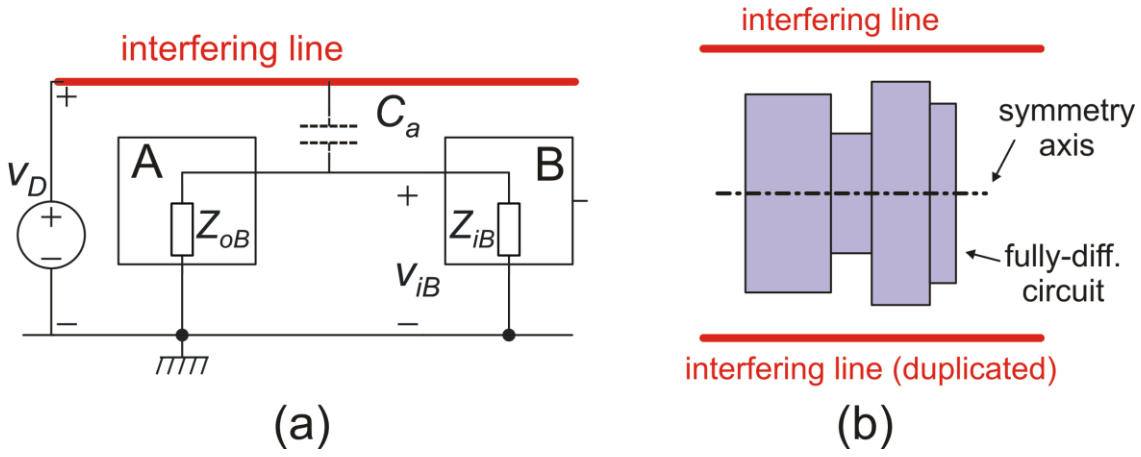

Fig.1.4. Equivalent circuit showing the mechanism of capacitive interference coupling (a); Duplication of the disturbing line in order to improve symmetry and enhance interference rejection.

Finally, let us consider substrate noise [1]. This expression is used to indicate the presence of fluctuations in the substrate potential, induced by interfering signals. The mechanism is illustrated in Fig. 1.5.

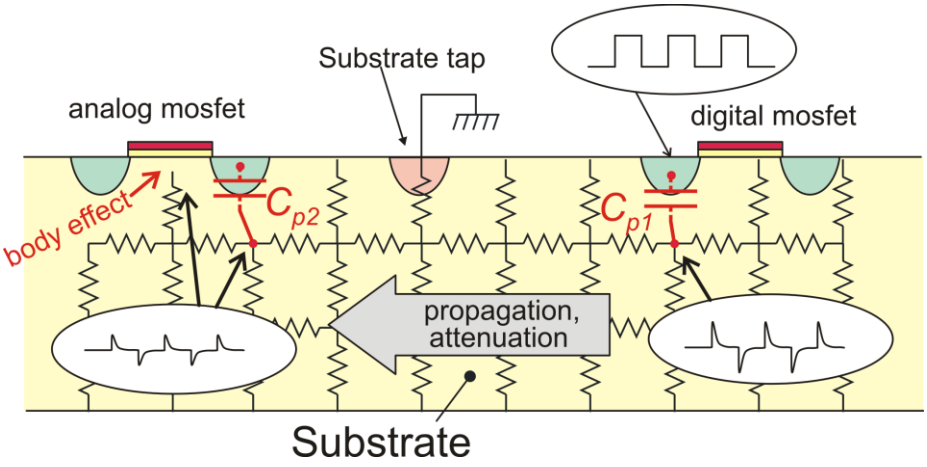

Fig.1.5. Cross-section illustrating generation and propagation of the substrate noise.

The device indicated as “digital mosfet” represents an electronic device that is subjected to large and fast voltage swing. Typical examples are transistors belonging to logical gates that perform frequent commutations. The square wave represent a possible signal present on the drain (or source) of the digital mosfet. This disturbing signal propagates into the substrate through the drain/body (or source/body) junction capacitance C_{p1}. Since any point of the substrate has a resistive path to ground (represented by the substrate tap in Fig. 1.5), the effect, in the proximity of the drain (source) diffusion, is high pass filtering, producing the impulsive signal shown in Fig. 1.5. This signal propagates along the resistive substrate, represented as a resistor mesh. Propagation is accompanied by strong attenuation, but voltage oscillations of several millivolts can be observed at relatively high distance from the digital mosfet. These oscillations can reach sensitive devices, represented by the “analog

mosfet". The disturbance affects the analog mosfet in two ways: first, it can be injected into the drain/source through the junction capacitance C_{p2}. Second, since the substrate forms the body of all n-type mosfets, substrate potential fluctuations produce variations of the threshold voltage, causing drain current fluctuations.

A possible remedy is enclosing the digital subsection into a ring of substrate taps, all tied to ground. This reduces the propagation of the disturbing signals produced by the numerous digital gates forming the digital circuit, since the contact ring short-circuits the currents injected into the substrate, making them flow to ground. A further improvement is obtained by enclosing also the analog circuits into a contact ring, as schematically shown in Fig. 1.6.

Fully-differential systems are also less prone to substrate noise. The reason is that, at a sufficient distance from the digital (noisy) devices, substrate noise is almost uniform over relatively large die portions, so that it produces practically only common mode effects, leaving differential signals almost unaltered.

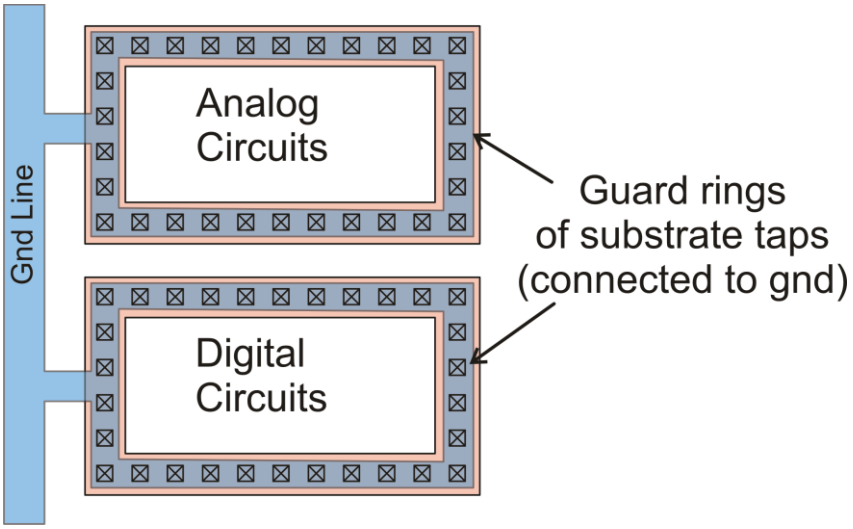

Fig.1.6. Substrate noise mitigation by means of substrate contact rings.

Wider signal ranges.

Consider a unipolar signal that can vary between two voltages, namely V_{MIN} and V_{MAX}, with $V_{MIN}<V_{MAX}$. The total full scale excursion will be $V_{FS}=(V_{MAX}-V_{MIN})$. In a single supply configuration (i.e. when the power supply is a single voltage source = V_{dd}), clearly $V_{FS}<V_{dd}$.

For a differential signal, we can consider that each node of the pair has the same range of a unipolar signal. Therefore, indicating with v_{op} and v_{on} the voltages of the nodes of the pair, we will have the following situations, summarized in table 1.1:

Voltage	Maximum positive signal	Maximum negative signal	V_{FS}
v_{op}	V_{MAX}	V_{MIN}	$(V_{MAX}-V_{MIN})$
v_{on}	V_{MIN}	V_{MAX}	$(V_{MAX}-V_{MIN})$
$v_{od}= v_{op} - v_{on}$	$(V_{MAX}-V_{MIN})$	$-(V_{MAX}-V_{MIN})$	$2(V_{MAX}-V_{MIN})$

Table 1.1: Excursion of v_{on}, v_{op} and v_{od}

It can be easily seen that the differential signal has a double range with respect to the individual voltages that represent it. Thanks to this property, in the case of single supply operation, a differential signal can achieve a full-scale range of at nearly $2V_{dd}$.

Improved linearity.

If we consider a dc trans-characteristic $V_{out}(V_{in})$, in the case of a fully-differential circuit we will have the following condition: $V_{out}(V_{in})=V_{od}(V_{in})=V_{on}(V_{in})-V_{op}(V_{in})$. For the symmetry property of a fully differential circuit, inverting the input signal is equivalent to swapping the positive and the negative halves, so that V_{op} and V_{on} are simply swapped.

Thus:

$$V_{out}(-V_{in}) = V_{op}(-V_{in}) - V_{on}(-V_{in}) = V_{on}(V_{in}) - V_{op}(V_{in}) = -V_{out}(V_{in}) \tag{1.3}$$

Therefore, an inversion of the input signal produce the inversion of the output signal (odd symmetry). This property is valid in the general case, i.e. also if the characteristic cannot be considered linear. This means that a Taylor expansion includes only odd terms, and then the characteristic is generally more linear than the two unipolar components $V_{op}(V_{in})$ and $V_{on}(V_{in})$ that form it, which, on the contrary, can include both odd and even terms.

In terms of harmonic distortion, if $V_{in}(t)$ is a sinusoidal waveform, the output differential voltage V_{out} will include only odd harmonics, and this is another indication of lower distortion, i.e. improved linearity.

These arguments are illustrated by Fig. 1.7, showing the possible dependence of the output unipolar voltages v_{on} and v_{op} on the input signal v_{in}, together with their difference v_{od}. Note that the individual signal v_{on} and v_{op} are generally not symmetrical with respect to the axis $v_{in}=0$, while, due to the symmetry of the fully-differential circuit, $v_{on}(v_{in})= -v_{op}(v_{in})$. This property is used in (1.3) to demonstrate the symmetry of v_{od}. Furthermore, Fig. 1.7 well shows how the differential signal achieves a double range with respect to the individual unipolar signals v_{on} and v_{op} that form it.

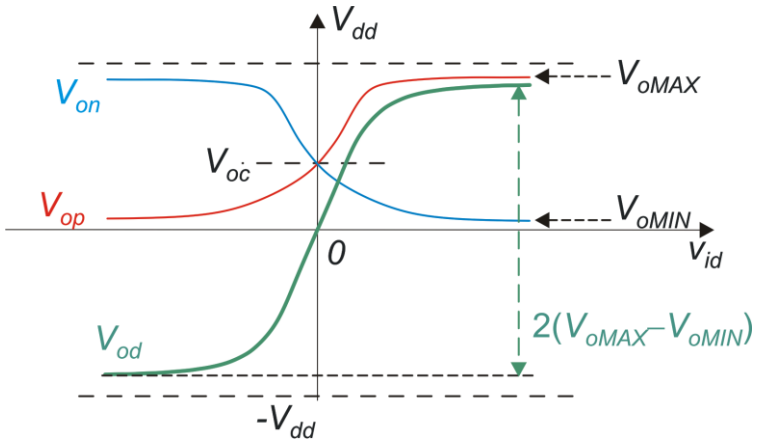

Fig.1.7. Possible dc transfer characteristics of a fully differential block, including both the differential signal v_{od} and the two unipolar signals v_{on} and v_{op} that form it.

Requisites for a correct fully differential transfer characteristic.

In a fully differential architecture, it is important that all the signals (i.e voltage pairs) present in the circuit have a constant common mode voltage. This is necessary to guarantee that the input common mode range of all blocks that receive those signals is not violated. As a result, the output common mode voltage of all block should be stabilized to a given value. This value can vary from block to block, but should be constant against process and temperature variations as well as input signal

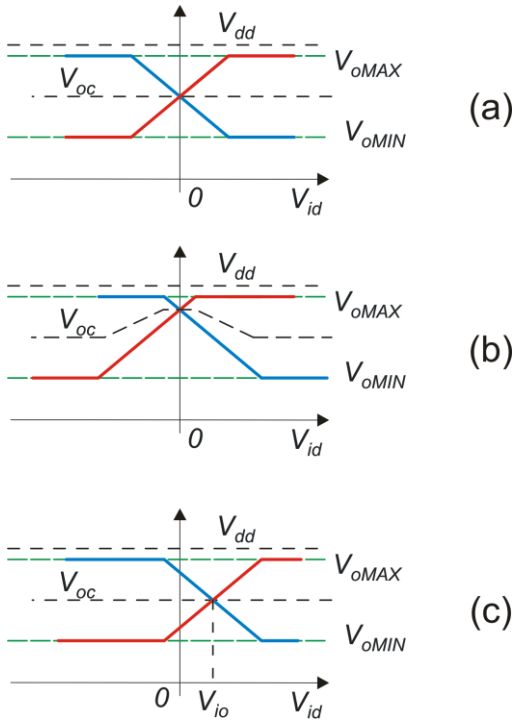

Fig.1.8. Ideal characteristic (a), misplaced output common mode voltage (b), presence of an input offset (c).

Figure 1.8 shows three possible d.c. transfer characteristics. The ideal characteristic is shown in Fig. 1.8 (a) where the output common mode voltage has been placed in the middle of the output range of the individual signals v_{op} and v_{on}. In this way, the output range where both outputs are in a linear region is maximized, i.e. the output linear range is maximized. In Fig. 1.8 (b), the output common mode voltage is set to a value that is too close to V_{oMAX}. The consequence is that the outputs have little room to increase and they saturate too early to V_{oMAX}. When one of the two outputs saturates, the differential-to-differential gain (A_{dd}) is halved and the output common mode voltage cannot be kept constant any longer. The third example shows a characteristic where the output common mode voltage has been set to an ideal value, but an offset V_{io} is present. This is a perfectly acceptable characteristic, since the maximum output swing is maintained. Since the presence of an offset is unavoidable, characteristic (c) is what we generally could aspire to obtain in practice.

To summarize, what is important is to guarantee that the output common mode voltage can be reliably set to a precise value, which is generally placed in the middle of the output range. In most fully differential blocks, this result is obtained by means of a proper feedback loop included inside the block itself (denominated CMFB: common mode feedback).

1.2 Fully differential operational amplifiers: functional properties and simple configurations

Definitions

The symbol of a fully differential amplifier is shown in Fig. 1.9. The ideal equation that ties the output and input differential mode voltages is:

$$V_{od} = AV_{id} \quad \text{with} \quad A \to \infty \tag{1.4}$$

A more realistic relationship that takes into account also the presence of an offset-noise input equivalent source (v_n) and of the finite gain is the following:

$$v_{od} = A(v_{id} - v_n) \quad \text{with} \quad A >> 1 \tag{1.5}$$

We have to add the following equation for the common mode voltage:

$$v_{oc} \equiv V_{CMO} = \textit{constant} \tag{1.6}$$

This characteristic is indicated in the amplifier symbol by a small reversed triangle placed close to the tip of the main triangle, as shown in Fig. 1.9.

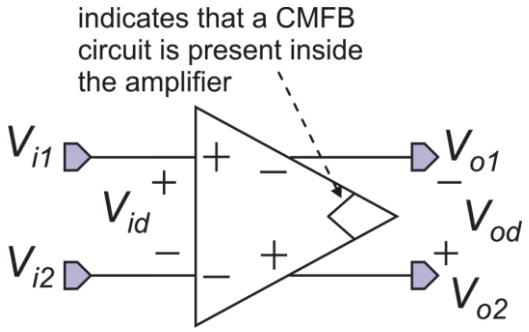

Fig.1.9. Symbol of the fully differential amplifier

Generic feedback configuration: differential mode voltage at the input port

The first case that we will analyze is the generic closed loop configuration shown in Fig. 1.10 (a). We consider that the transfer characteristic of network β is the following:

$$v_{id} = \beta v_{od} + V_k \tag{1.7}$$

We have already seen[1] that an equation of this kind, combined with (1.5) leads to the following approximation, provided that |βA|>>1 and the system is stable:

$$v_{id} \cong v_n' \equiv \frac{\beta A}{\beta A - 1} v_n \tag{1.8}$$

where v_n' is the input referred noise filtered by the $\beta A/(\beta A\text{-}1)$ transfer function (generally of low pass type). In the following discussion, we will use the symbol v_n to indicate also v_n', for simplicity, but it must be remembered that we are actually dealing with a filtered version of the input referred noise. In other words, we will assume that in the frequency band of interest.

$$v_n' \cong v_n \tag{1.9}$$

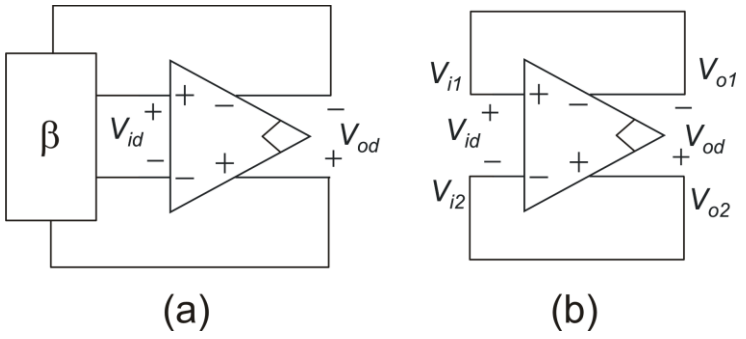

Fig.1.10. Generic feedback connection (a) and "unity gain" connection (b).

[1] see the chapter on sensor interfaces, section on switched capacitor circuits.

The "unity gain" configuration for a fully-differential op-amp

As a particular case, we consider the "unity gain" configuration shown in Fig. 1.10 (b). This is not properly a unity gain system, since there are no terminals available to apply an input signal. Nevertheless, it is an important configuration for switched capacitors circuits, where it represents a reset situation, where voltages across all capacitors assume a known value. This configuration is characterized by the following equations:

$$v_{id} = -v_{od} \; ; \quad v_{ic} = -v_{oc} \tag{1.10}$$

The first equation regards the differential voltages and is equivalent to (1.7) with β= -1 and V_k=0. Then:

$$v_{id} = v_n \quad v_{od} = -v_n \tag{1.11}$$

Using the second of (1.10) and (1.6), we easily find:

$$v_{i1} = V_{CMO} + \frac{v_n}{2}; \quad v_{i2} = V_{CMO} - \frac{v_n}{2} \tag{1.12}$$

and:

$$v_{o1} = V_{CMO} + \frac{v_n}{2}; \quad v_{o2} = V_{CMO} - \frac{v_n}{2} \tag{1.13}$$

Note that, without (1.6), only the differential voltages would have been determined, while the individual voltages at the input and output terminals would have been uncertain. This highlights once more the necessity of stabilizing the output common mode voltage to a known value.

Fully differential amplifier with resistive feedback

Let us now consider the amplifier of Fig. 1.11 (a), obtained applying a resistive feedback network to a fully differential op-amp.

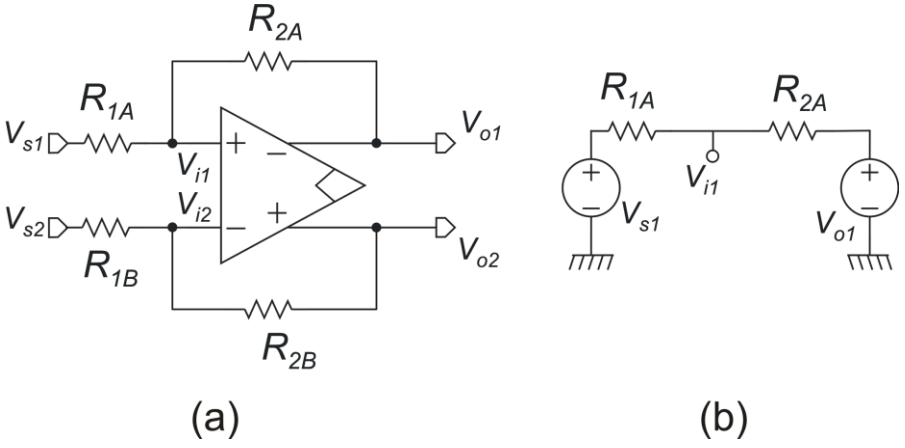

Fig.1.11. Fully differential amplifier with resistive feedback (a). Network used to calculate v_{i1} (b)

Nominally $R_{2A}=R_{2B} \equiv R_2$ and $R_{1A}=R_{2B} \equiv R_1$. In practice, mismatches are present and need to be taken into account. Considering the network of Fig. 1.11 (b), we can calculate v_{i1} as a function of V_{s1} and V_{o1}.

$$v_{i1} = v_{o1}\frac{R_{1A}}{R_{1A}+R_{2A}} + v_{S1}\frac{R_{2A}}{R_{1A}+R_{2A}} = v_{o1}\frac{R_{1A}}{R_{1A}+R_{2A}} + \left[1-\frac{R_{1A}}{R_{1A}+R_{2A}}\right]v_{S1} \tag{1.14}$$

With the same principle, we can calculate v_{i2}:

$$v_{i2} = v_{o2}\frac{R_{1B}}{R_{1B}+R_{2B}} + v_{S2}\left[1-\frac{R_{1B}}{R_{1B}+R_{2B}}\right] \tag{1.15}$$

We can introduce the following variables:

$$\beta_1 \equiv \frac{R_{1A}}{R_{1A}+R_{2A}};\quad \beta_2 \equiv \frac{R_{1B}}{R_{1B}+R_{2B}} \tag{1.16}$$

Clearly, in the nominal circuit $\beta_1=\beta_2 \equiv \beta=R_1/(R_1+R_2)$.

Then we can decompose β_1 and β_2 into a mean component, β_m and a mismatch error $\Delta\beta$:

$$\beta_1 = \beta_m + \frac{\Delta\beta}{2};\quad \beta_2 = \beta_m - \frac{\Delta\beta}{2} \tag{1.17}$$

Then, we can re-write (1.14) and (1.15) using (1.16) and (1.17):

$$v_{i1} = v_{o1}\left(\beta_m + \frac{\Delta\beta}{2}\right) + v_{S1}\left(1-\beta_m - \frac{\Delta\beta}{2}\right) \tag{1.18}$$

$$v_{i2} = v_{o2}\left(\beta_m - \frac{\Delta\beta}{2}\right) + v_{S2}\left(1-\beta_m + \frac{\Delta\beta}{2}\right) \tag{1.19}$$

Subtracting (1.19) from (1.18) we obtain.

$$v_{i2} - v_{i1} = v_{od}\beta_m - v_{oc}\Delta\beta + v_{Sd}\left(1-\beta_m\right) + v_{Sc}\Delta\beta \tag{1.20}$$

where v_{Sd} and v_{Sc} are the differential and common mode voltages of the source V_S, defined as:

$$v_{Sd} \equiv v_{S2} - v_{S1}\ ;\quad v_{Sc} \equiv \frac{v_{S2}+v_{S1}}{2} \tag{1.21}$$

In this analysis we will neglect the input noise / offset, so that (1.8) becomes, $v_{id}=v_{i1}-v_{i2}=0$. Thus:

$$v_{od} = v_{Sd}\frac{\left(1-\beta_m\right)}{\beta_m} - \left(v_{Sc}-v_{oc}\right)\frac{\Delta\beta}{\beta_m} \tag{1.22}$$

From (1.22) we find that the differential-to-differential gain A_{dd} is:

$$A_{dd} = \frac{(1-\beta_m)}{\beta_m} \underset{\text{nominal}}{=} \frac{(1-\beta)}{\beta} = \frac{R_2}{R_1} \tag{1.23}$$

Due to mismatch $\Delta\beta$ between the upper (R_{1A}, R_{2A}) and lower (R_{1B}, R_{2B}) part of the feedback network, the output differential voltage includes also a term that depends on the difference between the source common mode voltage (v_{sc}) and the output common mode voltage (v_{oc}). Since v_{oc} is fixed to the constant V_{CMO}, this means that the output differential voltage is sensitive to the source common mode voltage. Therefore, the common-to-differential mode gain (A_{cd}) will be given by $-\Delta\beta/\beta_m$ and the CMRR turns out to be [2]:

$$CMRR = \left|\frac{A_{dd}}{A_{cd}}\right| = |A_{dd}| \left|\frac{\Delta\beta}{\beta_m}\right|^{-1} \tag{1.24}$$

Since $\Delta\beta/\beta_m$ is going to be independent of the resistance values (it is a matching error that depends only on relative resistance mismatches), the higher A_{dd}, the higher the CMRR.

Equations (1.23) and (1.24) describe the behavior of the amplifier with respect to the output differential voltage. In a fully differential circuit, it is important also to study the behavior of the common mode component. Clearly, the output common mode voltage is known, since it is fixed to V_{CMO} by the internal CMFB circuit. Then, the quantity that has to be determined is the input common mode voltage of the operational amplifier, V_{ic}. In general, the reason of analyzing the common mode components is verifying that they do not exceed the corresponding ranges. Therefore, when analyzing the common mode components, the required degree of precision is usually much lower than for differential components. Then we will neglect the matching error $\Delta\beta$, and we will use the average components β_m that we will consider equal to the nominal value β. Summing up (1.18) and (1.18) and dividing the result by 2, we obtain:

$$V_{ic} = \beta V_{CMO} + (1-\beta) v_{Sc} \tag{1.25}$$

where v_{Sc} is the common mode voltage of the signal source, given in (1.21). For amplifications $A_{dd}>>1$, $\beta<<(1-\beta)$, so that V_{ic} is nearly equal to v_{Sc}. It is then important to check that for every possible value of v_{Sc} (that depends on the type of signal sources), V_{ic} stays inside the input common mode range of the amplifier.

Fully differential instrumentation amplifier based on the 3-op-amp architecture

A limitation of the amplifier of Fig. 1.11 (a) is its low input resistance. The differential mode input resistance is equal to $2R_1$, which cannot be made larger than a few MΩ, due to limitation on the feasible resistance values. Very often, noise and bandwidth considerations impose much smaller values for R_1, resulting in input resistances of a few kΩ. These values are definitely too small for an instrumentation amplifier. A possible solution is using the two-stage architecture shown in Fig. 1.12, representing the fully differential version of the well know three-opAmp architecture.

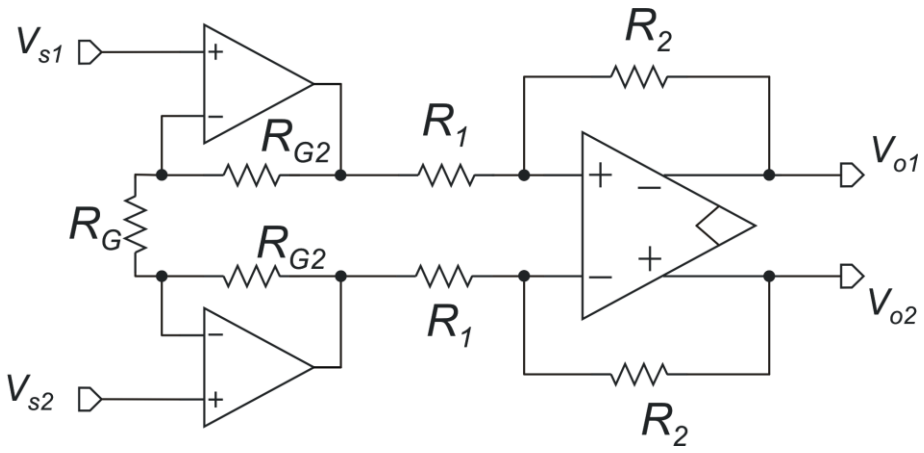

Fig.1.12. A three-OpAmp fully differential instrumentation amplifier.

The first stage, formed by the two single/ended op-amps, amplifies the input differential signal by $(1+2R_{G2}/R_{G1})$ but leaves the input common mode voltage unchanged. In ideal conditions ($\Delta\beta=0$), the second stage, formed by the fully differential amplifier, amplifies only the differential signal and reject the common mode one. The output common mode voltage is fixed to V_{CMO} and it does not depend on the input common mode voltage. It can be easily shown that this stage offers also a very high input resistance.

The difference differential amplifier (DDA)

We have obtained this result by adding two additional OpAmps of single-ended type. A possible question is whether it is possible to obtain a high resistance fully differential amplifier with precise gain using only a single fully differential amplifier. Note that in unipolar systems, a single-ended OpAmp can be used to build the non-inverting configuration, which has a high input resistance. Such a possibility does not exist for the in the fully differential domain, since the fully differential OpAmp does not perform the same function that the single-ended op-amp does in the unipolar domain. As Fig. 1.13 shows, in the unipolar domain, the single-ended op-amp accepts two distinct input signals, namely the inverting and non-inverting inputs. On the other hand, in the fully differential domain, each signal requires two connections, thus the op-amp accepts only one input signal. If we use that input for the feedback network, then there is not a free high resistance insertion point for connecting the amplifier to the signal source.

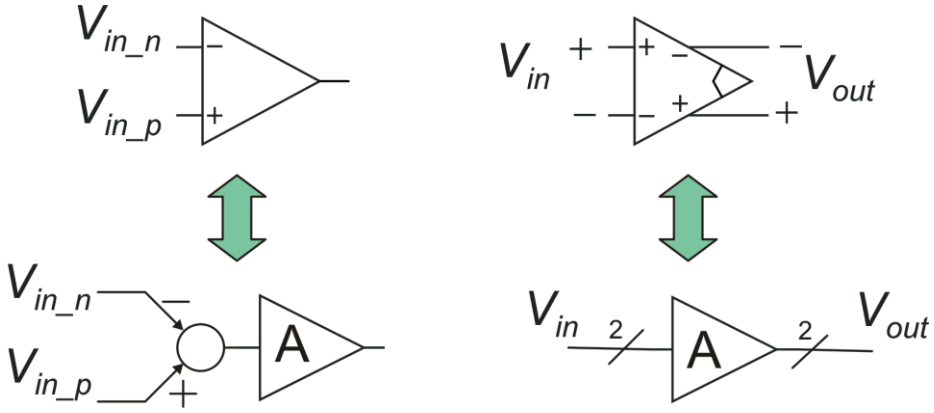

Fig.1.13. Equivalent block diagrams of the single ended (left) and fully differential (right) amplifier in the unipolar and fully differential domain, respectively.

In the fully differential domain, the equivalent of a differential amplifier is the DDA (Differential-Difference Amplifier) shown in Fig. 1.14.

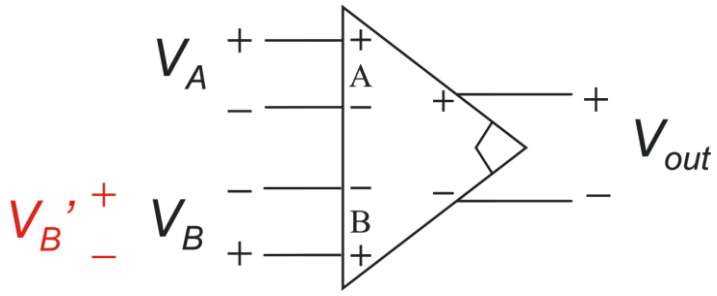

Fig.1.14. Symbol of the differential difference amplifier. The amplifier sums up signals V_A and V_B or, if the different convention of V_B' is used, subtracts V_B' from V_A.

The DDA is characterized by the following input/output ideal characteristic:

$$V_{od} = A(V_A + V_B) = A(V_A - V_B') \tag{1.26}$$

A DDA with a very high gain (ideally infinite) constitutes the DDA-OpAmp. It can be easily shown that, in terms of input and output signal, the DDA-OpAmp is the direct equivalent of the single-ended OpAmp: it is capable of amplifying the difference of two distinct signals (V_A and V_B'), and the input resistance at the two inputs can be made high by design (i.e. using a MOSFEF differential pair). An example of use of the DDA-op-amp is shown in Fig.1.15, where the architecture of an instrumentation amplifier is shown. Considering that no current flows into the input terminals, due to the very high resistance, then:

$$V_A = V_S; \qquad V_B = -\beta V_{od} \quad \text{with} \quad \beta = \frac{R_1}{R_1 + 2R_2} \tag{1.27}$$

Substituting (1.27) into (1.26) we get:

$$V_{od} = A(V_S - \beta V_{od}) \;\Rightarrow\; V_{od} = V_S \frac{A}{1+\beta A} \underset{A\to\infty}{=} V_S \frac{1}{\beta} = V_S\left(1+\frac{2R_2}{R_1}\right) \tag{1.28}$$

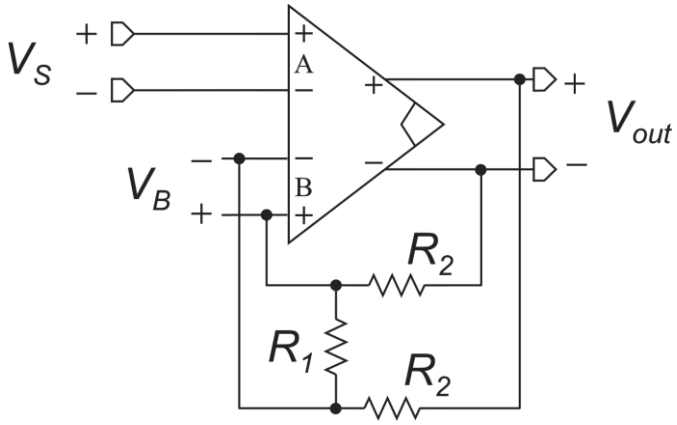

Fig.1.15. A DDA-based instrumentation amplifier

Since A>>1, the gain of this instrumentation amplifier is then $1+2R_2/R_1$. This architecture is frequently used in modern fully-differential integrated instrumentation amplifiers.

A switched capacitor, fully differential amplifier.

The switched capacitor approach can be used to obtain a fully differential amplifier capable of performing offset cancellation and flicker noise reduction by means of correlated double sampling (CDS). The schematic view of the amplifier is shown in Fig. 1.16.

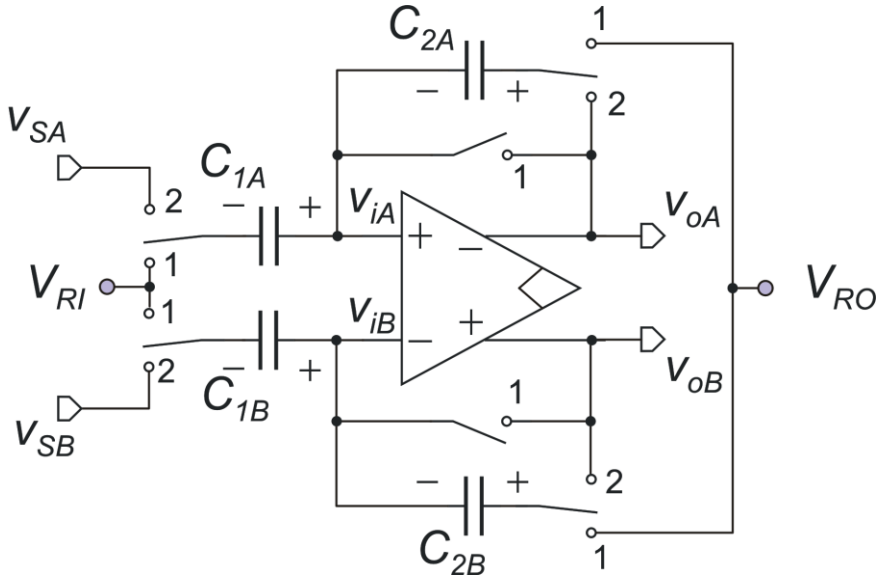

Fig.1.16. A fully differential switched capacitors amplifier.

The operating cycle is divided into two phases. Position of the switches in phase 1 and 2 is indicated by the numbers close to the terminals. V_{RO} and V_{RI} are constant voltages. In the following analysis we will assume that $C_{1A}=C_{1B}\equiv C_1$, $C_{2A}=C_{2B}\equiv C_2$. We will analyze the amplifier by first considering the situation in phase 1, shown in Fig. 1.17.

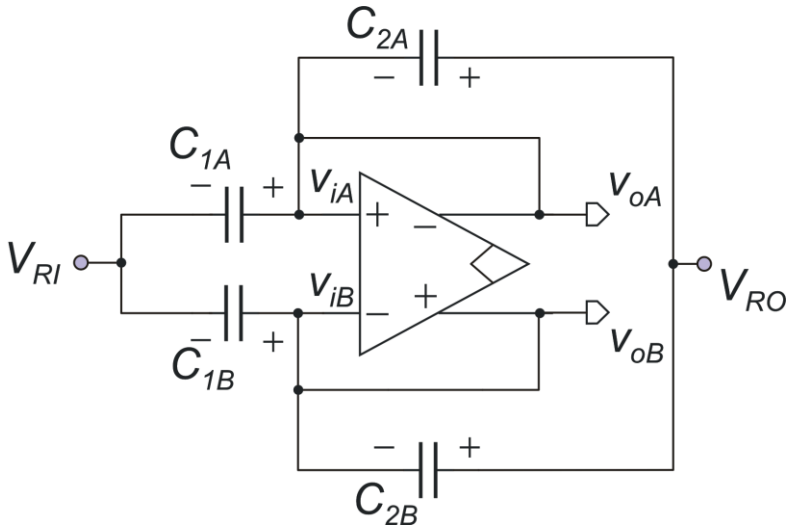

Fig.1.17. Switch configuration in phase 1.

It is a closed loop configuration already analyzed, for which:

$$v_{i1}^{(1)} = V_{CMO} + \frac{v_n^{(1)}}{2}; \quad v_{i2}^{(1)} = V_{CMO} - \frac{v_n^{(1)}}{2} \tag{1.29}$$

Voltages of the various capacitors can be easily found:

$$\begin{cases} v_{C1A}^{(1)} = V_{CMO} + \dfrac{v_n^{(1)}}{2} - V_{RI} \\ v_{C1B}^{(1)} = V_{CMO} - \dfrac{v_n^{(1)}}{2} - V_{RI} \\ v_{C2A}^{(1)} = V_{RO} - V_{CMO} - \dfrac{v_n^{(1)}}{2} \\ v_{C2B}^{(1)} = V_{RO} - V_{CMO} + \dfrac{v_n^{(1)}}{2} \end{cases} \tag{1.30}$$

In phase 1, the output differential voltage is given by:

$$v_{od} = V_{oB} - V_{oA} = -v_n^{(1)} \tag{1.31}$$

Then, only input referred noise voltage (including also the offset component) is present at the input.

At the end of phase 1, all the switches are first open, so that the voltage across all capacitors are sampled (sampling instant). The sampling operation involve the addition of *kT/C* noise contributions to all the capacitors. We will neglect these errors in the following analysis for simplicity. To see how *kT/C* noise affects the output voltage of a switched capacitor circuit, refer to the charge amplifier (interface for capacitive sensors) discussed in Chap. 2. Then, we will assume that the voltages in (1.30) are sampled. When the amplifier get into phase 2, the situation shown in Fig. 1.18 occurs.

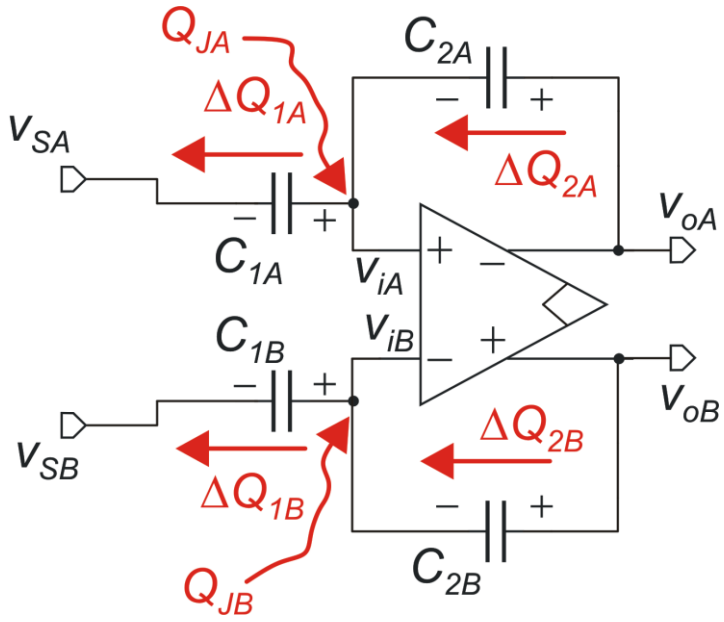

Fig.1.18. Switch configuration and charge transfer in phase 2.

First, note that the input common mode voltage of the amplifier is not immediately known as in phase 1. Its value will be calculated later; now, we will simply indicate it as V_{ic}. Then:

$$v_{i1}^{(2)} = V_{ic}^{(2)} + \frac{v_n^{(2)}}{2}; \qquad v_{i2}^{(2)} = V_{ic}^{(2)} - \frac{v_n^{(2)}}{2} \tag{1.32}$$

The voltage across capacitors C_{1A} and C_{1B} is given by:

$$\begin{aligned} v_{C1A}^{(2)} &= V_{ic}^{(2)} + \frac{v_n^{(2)}}{2} - V_{SA} \\ v_{C1B}^{(2)} &= V_{ic}^{(2)} - \frac{v_n^{(2)}}{2} - V_{SB} \end{aligned} \tag{1.33}$$

In phase 2, it is not possible to directly write the voltage across capacitors C_{2A} and C_{2B}, since they have one terminal connected to the output voltage, which is an unknown as well. We have to consider the charges ΔQ_{2A} and ΔQ_{2B} transferred into capacitors C_{2A} and C_{2B}, respectively and write:

$$\begin{cases} v_{C2A}^{(2)} = v_{C2A}^{(1)} + \dfrac{\Delta Q_{2A}}{C_2} \\ v_{C2B}^{(2)} = v_{C2B}^{(1)} + \dfrac{\Delta Q_{2B}}{C_2} \end{cases} \quad \text{where} \quad C_{2A} = C_{2B} \equiv C_2 \tag{1.34}$$

Due to the extremely high input resistance of the amplifier, the charges into C_{2A} and C_{2B} are the sum of the charges that flows into the corresponding amplifier input terminals. These charges come mainly

from capacitors C_{1A} and C_{1B}, due to the voltage change they experience in the transition from phase 1 to phase 2. Additional charges, which we have represented in Fig. 1.18 by Q_{JA} and Q_{JB}, derive from charge injection phenomena that will analyzed later.

Then, we can write:

$$\begin{cases}\Delta Q_{2A} = \Delta Q_{1A} - Q_{JA} = C_1\left(v_{C1A}^{(2)} - v_{C1A}^{(1)}\right) - Q_{JA} \\ \Delta Q_{2B} = \Delta Q_{1B} - Q_{JB} = C_1\left(v_{C1A}^{(2)} - v_{C1A}^{(1)}\right) - Q_{JA}\end{cases} \quad \text{where} \quad C_{1A} = C_{1B} \equiv C_1 \tag{1.35}$$

Using (1.30) and (1.34), we find:

$$\begin{cases} v_{C2A}^{(2)} = V_{RO} - V_{CMO} - \dfrac{v_n^{(1)}}{2} + \dfrac{C_1}{C_2}\left(V_{ic}^{(2)} + \dfrac{v_n^{(2)}}{2} - V_{SA} - V_{CMO} - \dfrac{v_n^{(1)}}{2} + V_{RI}\right) - \dfrac{Q_{JA}}{C_2} \\ v_{C2B}^{(2)} = V_{RO} - V_{CMO} + \dfrac{v_n^{(1)}}{2} + \dfrac{C_1}{C_2}\left(V_{ic}^{(2)} - \dfrac{v_n^{(2)}}{2} - V_{SB} - V_{CMO} + \dfrac{v_n^{(1)}}{2} + V_{RI}\right) - \dfrac{Q_{JB}}{C_2} \end{cases} \tag{1.36}$$

Finally, we can calculate the output voltages as:

$$\begin{cases} v_{oA}^{(2)} = v_{iA}^{(2)} + v_{C2A}^{(2)} \\ v_{oB}^{(2)} = v_{iB}^{(2)} + v_{C2A}^{(2)} \end{cases} \tag{1.37}$$

Then, using (1.36) and (1.32) we finally get the complete expression of the output voltages:

$$\begin{cases} v_{oA}^{(2)} = V_{ic}^{(2)} + \dfrac{v_n^{(2)}}{2} + V_{RO} - V_{CMO} - \dfrac{v_n^{(1)}}{2} + \dfrac{C_1}{C_2}\left(V_{ic}^{(2)} + \dfrac{v_n^{(2)}}{2} - V_{SA} - V_{CMO} - \dfrac{v_n^{(1)}}{2} + V_{RI}\right) - \dfrac{Q_{JA}}{C_2} \\ v_{oB}^{(2)} = V_{ic}^{(2)} - \dfrac{v_n^{(2)}}{2} + V_{RO} - V_{CMO} + \dfrac{v_n^{(1)}}{2} + \dfrac{C_1}{C_2}\left(V_{ic}^{(2)} - \dfrac{v_n^{(2)}}{2} - V_{SB} - V_{CMO} + \dfrac{v_n^{(1)}}{2} + V_{RI}\right) - \dfrac{Q_{JB}}{C_2} \end{cases} \tag{1.38}$$

Output differential voltage. Subtracting v_{oB} from v_{oA}, with simple algebraic passages, we find the following expression for the output differential voltage:

$$v_{od}^{(2)} = \frac{C_1}{C_2} V_{SD}^{(2)} - \left(v_n^{(2)} - v_n^{(1)}\right)\left(1 + \frac{C_1}{C_2}\right) + \frac{Q_{JA} - Q_{JB}}{C_2} \qquad V_{SD} \equiv V_{SA} - V_{SB} \tag{1.39}$$

The ideal behavior is that of an amplifier with gain A=C_1/C_2. A programmable gain can be easily obtained by using digitally programmable capacitors for C_1 and C_2. An example of programmable capacitor is shown in Fig. 1.19. Capacitor C is always connected since a configuration with zero capacitance is meaningless. The other capacitors, namely C_{00}, C_{01} and C_{02} can be added to the total capacitance by closing the corresponding switches, controlled by digital lines b_{0-2}.

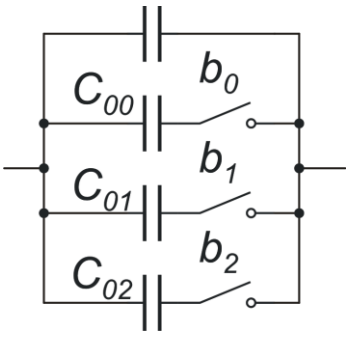

Fig.1.19. A digitally programmable capacitor.

In addition to the ideal output signal, we have two error contributions. One is due to the noise / offset voltage of the amplifier, v_n, which appears as the difference between two samples taken at two different instants, and then undergoes correlated double sampling (CDS). The other error term, is due to charge injection. It is useful to refer both contribution to the amplifier input, by simply dividing the output error by gain A. The result is summarized in table 1.2:

	Output contribution	Referred to the input
Amplifier noise	$-\left(v_n^{(2)} - v_n^{(1)}\right)(1+A)$	$-\left(v_n^{(2)} - v_n^{(1)}\right)\left(\frac{1+A}{A}\right)$
Charge injection	$\frac{Q_{JA} - Q_{JB}}{C_2}$	$\frac{Q_{JA} - Q_{JB}}{C_1}$

Table 1.2. Output and input referred error contribution for the switched capacitors amplifier

It is important to state two points:

-) For large values of A, the input referred noise of the amplifier coincides with the input referred noise of the OpAmp, after application of correlated double sampling.

-) The charge injection contribution depends on the difference of the charges injected on the negative and positive side of the differential structure. Due to symmetry, the two charge components tend to compensate each other and the residual component will be only a matching error of the charges.

Input common mode voltage. In a fully differential system, it is important to analyze also the common mode value of every node pair that represents the signals. This analysis is aimed to check that the common mode voltages do not experience variations that could exceed the input or output ranges of the block involved in the system. Therefore, no particular precision is required and broad approximations can be used

In the case of the switched capacitor amplifier, the output common mode voltage is fixed to V_{CMO}, while the source common mode voltage, V_{SC}, is fixed by the characteristics of the source itself. Therefore, the only unknown is the common mode voltage of the operational amplifier inputs, i.e. V_{ic}.

Summing up the expressions of v_{oA} and v_{oB} given in (1.38) and dividing the result by two, we obtain:

$$V_{CMO} = V_{ic}^{(2)} + V_{RO} - V_{CMO} + \frac{C_1}{C_2}\left(V_{ic}^{(2)} - V_{SC} - V_{CMO} + V_{RI}\right) - \frac{Q_{JA} + Q_{JB}}{C_2} \tag{1.40}$$

Neglecting the charge injection term, which is not important due the low precision requirements, and solving (1.40), we get:

$$V_{ic}^{(2)} = V_{CMO} + \frac{V_{CMO} - V_{RO}}{1 + A} + \frac{A}{A+1}\left(V_{SC} - V_{RI}\right) \tag{1.41}$$

Note that in phase 1, V_{ic} was equal to V_{CMO}. It is desirable that this value is maintained also phase 2, or, at least, small variations with respect to V_{CMO} are produced by the transition. To obtain this result V_{RO} is set equal to V_{CMO} and V_{RI} as close as possible to V_{SC}. In the case that it is not possible to predict the common mode voltage of the signal source, it is important to guarantee that, for none of the possible V_{SC} values, V_{ic} goes out of the input common mode range of the Op-Amp.

The origin of charges Q_{jA} and Q_{jB}.

Charges Q_{jA} and Q_{jB} have two main origins:

- Charge injection from the switches
- Charge induced by variation of the input common mode voltage of the amplifier (*Vic*).

In this section, we will simply describe the second of the two causes, since the first one, namely charge injection from the switches, is a much more general problem for switched capacitor circuits and will be discussed in next section.

The effect of a change of the input common mode voltage in the transition between phase 1 and phase 2 is depicted in Fig. 1.20. The figure represent the amplifier with the parasitic capacitances between the input terminals and ground (common mode input capacitances). The other elements of the circuit, and, in particular, the feedback network have been omitted for the sake of simplicity.

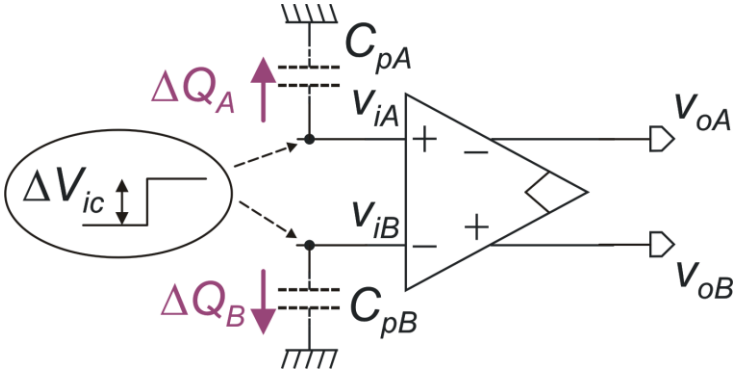

Fig.1.20. Input charges deriving from input common mode variation across phase 1 and 2

If the common mode undergoes a variation ΔVic, then the following charges flows through the parasitic capacitors C_{p1} and C_{p2}:

$$\Delta Q_A = \Delta V_{ic} C_{pA} \;; \quad \Delta Q_B = \Delta V_{ic} C_{pB} \tag{1.42}$$

Since there will be an unavoidable mismatch between C_{p1} and C_{p2}, charges ΔQ_A and ΔQ_B will be slightly different, and the effect of this difference will introduce a contribution to the charge injection error reported in table 1.2. To minimize this effect it is important to keep V_{ic} variation across phase 1 and phase 2 transition as small as possible.

1.3 The switch charge-injection phenomenon.

The phenomenon of charge injection is generally related to switches. In an ideal switch, the control signal simply opens and close the connection, with no side effects. In integrated circuits, switches are implemented with MOSFETs: the switch terminals are the source and drain, while the control signal is applied to the gate. Since parasitic capacitances exist between the gate and both the drain and source, a parasitic interaction between the control signal and the switch terminals occurs. Figure 1.21 shows the equivalence between an ideal switch and the MOSFET-switch. Note that in a MOSFET-switch, as in an ideal switch, the current between the terminals can flow in both directions, thus it is not possible to decide *a priori* which terminal operates as the source and which as the drain. Thus, we have generically indicated with N_1 and N_2 the two terminals of the switch. Capacitive coupling between the control signal (ck) and terminals N_1 and N_2 is due to two different kind of capacitances:

- The intrinsic capacitance, due to modulation of the mobile charge in channel, represented by the blue "–" symbols in Fig. 1.21.
- The *extrinsic* capacitance due to the overlap between the gate and the drain / source diffusions, represented by the two capacitors C_{OV1} and C_{OV2} in Fig. 1.21.

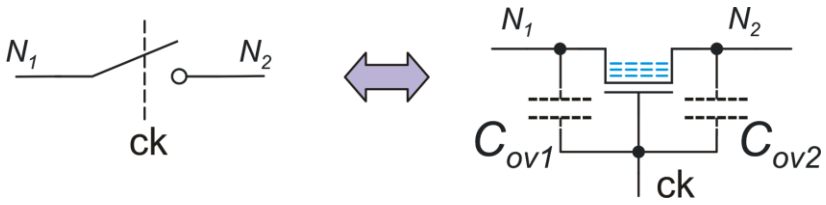

Fig.1.21. The MOSFET switch, with the overlap capacitors and the charge accumulated into the channel in the "on" state.

At any transition of the control signal, the charge accumulated in both types of capacitances undergoes a massive variation, so that a charge flows from the control terminal to the switch terminals N_1 and N_2. The portion of this charge that originates from the channel is generally referred to as "charge injection", while the portion due to the overlap capacitances is generally indicated as "clock feedthrough". The difference between the two phenomena is that the clock feedthrough, being due to almost ideal capacitors, is mainly linear, while the charge accumulated in the channel is a nonlinear function of the voltages. Since the effects are similar, we will simply use the term "charge injection" for both. Fig. 1.22 gives a simple representation of what happens when a switch, initially on, is turned off.

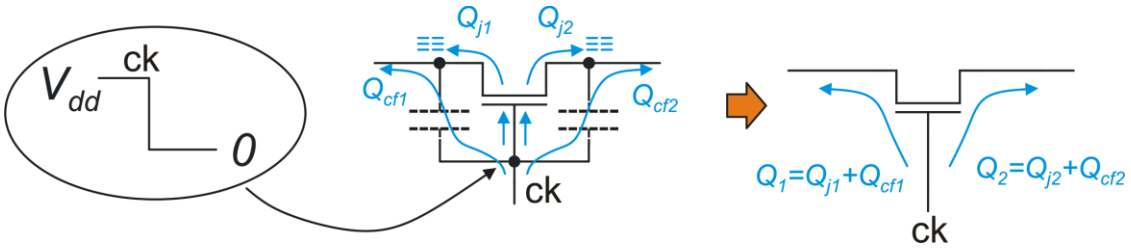

Fig.1.22. Charge transfer during occurring when an n-MOSFET-switch is turned off

The mobile charge accumulated into the channel is ejected into the switch terminals (charges Q_{J1} and Q_{J2}). At the same time, the transition of control voltage *ck* injects the charges Q_{cf1} and Q_{cf2} through the overlap capacitors. The net result, shown on the right side of the figure, is the injection of charges Q_1 and Q_2. For an n-MOSFET, these charges are negative. When the switch is turned on again, we have a similar phenomenon but the injected charges are positive.

The effect of charge injection can be easily understood considering the simple track and hold circuit of Fig. 1.23. As the diagram on the right shows, the control signal passes from the high to the low value at instant t_c. As a consequence of this transition, the switch is turned off and the circuit passes from the track phase, where the output voltage is equal to the input voltage V_S, to the hold phase where the value of V_S sampled at t_c is maintained. The two charges Q1 and Q2 are injected into the switch terminal at the sampling instant. Note that only Q_2 produces an effect, since it is accumulated into capacitor C, altering the sampled value. On the contrary, Q_1 flows into the source V_S producing no effects on the output signal. The effect of charge injection Q_2 on the output voltage is represented in the plot with the variation ΔV_C that, in track and hold circuits is called "pedestal" voltage. The charge injected by MOSFET-switches of minimum size are of the order of a few fC (femto-Coulomb). The error $\Delta V_C = Q_2/C$ is then of the order of a few mV when C is 1 pF.

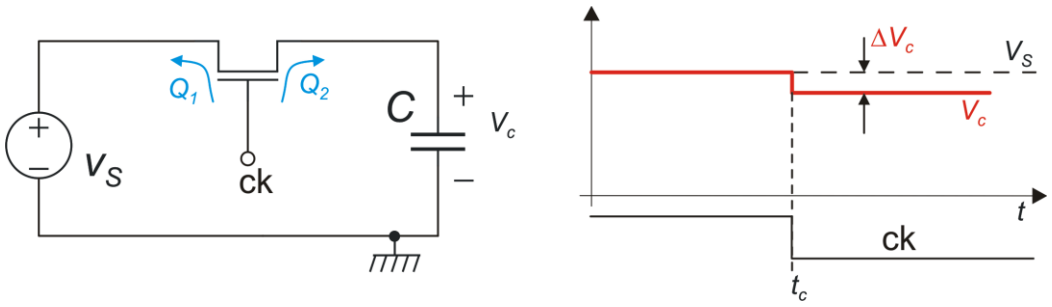

Fig.1.23. Charge transfer during occurring when an n-MOSFET-switch is turned off

In a more complex circuit, such that of Fig. 1.16, it is not simple to study the role of all the switches in determining charges Q_{jA} and Q_{jB}. but the concept is just the same. For example, the switches that, in phase 1, close the amplifier in unity gain configuration, inject charges directly into the amplifier input nodes.

Charge injection can be reduced by using switches of minimum area and choosing very large capacitors (e.g. *C* in Fig. 1.23, C_1 and C_2 in Fig. 1.16). Unfortunately, this make the charging transients longer, thus reducing the maximum clock frequency. Furthermore, large capacitances are often not allowed by area occupation constraints. A method that is often used to compensate charge injection is the use of dummy switches [3] as shown in Fig. 1.24.

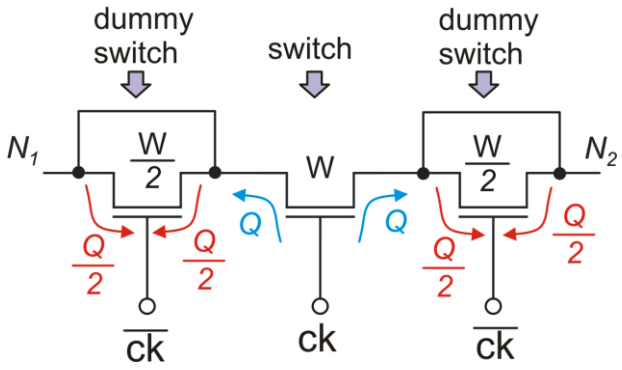

Fig.1.24. Use of dummy switches to compensate charge injection

The dummy switches are clocked with the inverse of the control signal, so that they inject a charge that is opposed to that of the main switch. Their terminals are short-circuited as shown in the figure, to prevent them from affecting the switching function (they have no effect in terms of connection). Note that the two charges injected by a dummy switches into its terminals are collected together onto the same terminal of the main switch. Therefore, to obtain charge compensation, their width has to be half of the main switch width. Note that charge compensation occurs only if the charges injected by the main switch into its two terminals are identical, i.e. $Q_1=Q_2$ in Fig. 1.23. This generally does not happen, since the ratio between Q_1 and Q_2 depends on several parameters, such as the impedances seen from the two terminals and the clock rise and fall times. Charge injection is difficult to model [4] and empirical recipes are often adopted. Furthermore, mismatches between the main switch and the dummy-switches contribute to prevent a perfect charge compensation. However, the dummy switch approach may contribute to reduce charge injection of at least one order of magnitude. In many cases, as that of Fig. 1.23, the circuit is sensitive to the charge injected only into one of the two switch terminals so that only one dummy switch is required [3].

The MOSFET-switch should be replaced by a complementary pass-gate (shown in Fig. 1.25), whenever the signals to be passed have a range that may get close to each rail. The pass-gate has the further advantage that its series resistance in the "on" state is more independent of the voltages applied to the switch terminals. The pass gate produces also a partial compensation of the charge injection, since the *n*-MOSFET and *p*-MOSFET that form it are driven by opposite control signals. Unfortunately, the charge present in the channel of the two transistors shows also an opposite dependence on the terminal voltage. For example, if the voltages applied to the terminals are close to ground, the charge in the *n*-MOSFET will be maximum, while the charge in the *p*-MOSFET vanishes. Therefore, charge compensation in a pass-gate cannot be based only on the *p*-*n* complementarity and dummy switch should be added to both the *n* and *p* components.

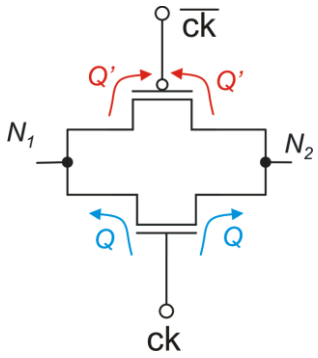

Fig.1.25. Charge injection in a complementary pass-gate: charges Q and Q' generally do not compensate.

1.4 References

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