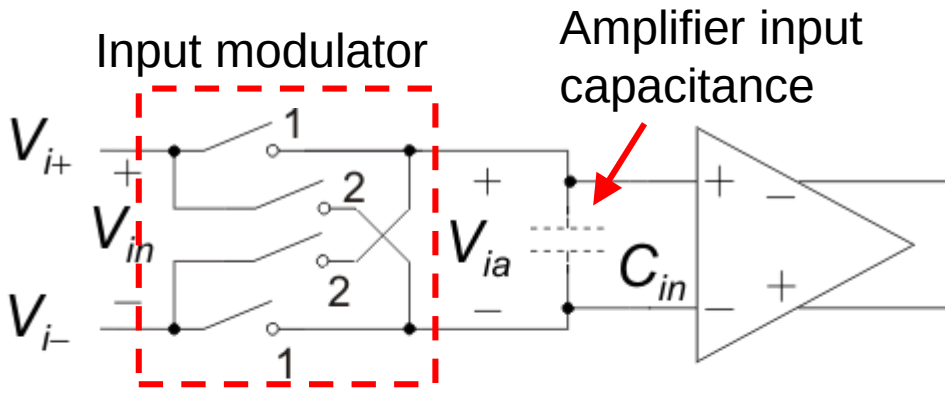
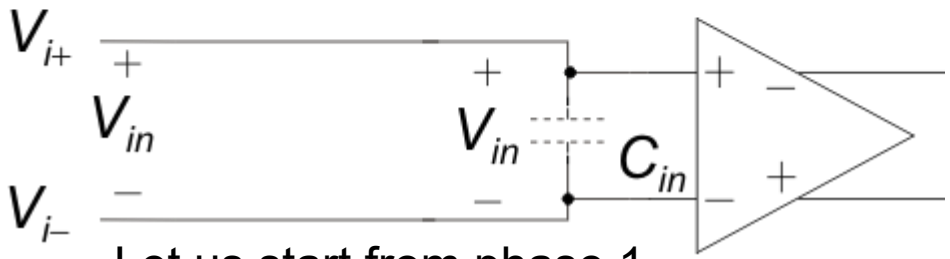
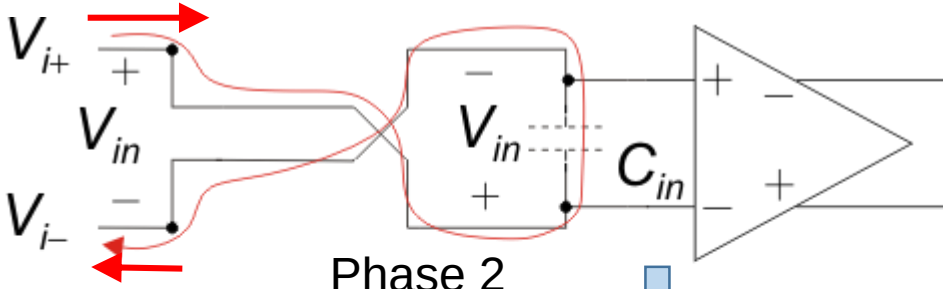
Finite input resistance of chopper amplifiers





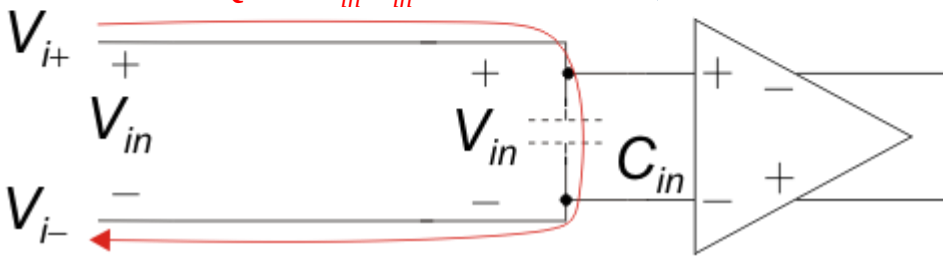
Let us start from phase 1 …

$\Delta Q = (V_{end} - V_{start})C_{in} = 2V_{in}C_{in}$

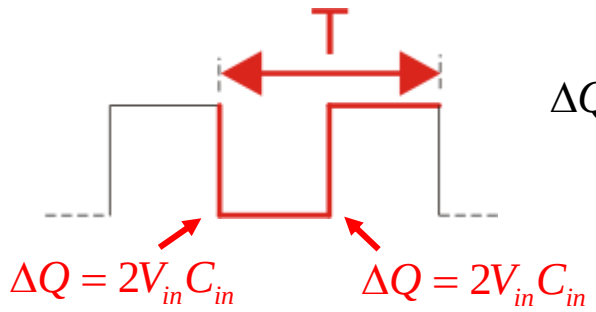


Phase 2

$\Delta Q = 2V_{in}C_{in}$



Phase 1 again



$\Delta Q_{tot} = 4V_{in}C_{in}$ (one period)

$$I_{eq} = \frac{4V_{in}C_{in}}{T} = 4V_{in}C_{in}f_{ck}$$

$$R_{eq} = \frac{V_{in}}{I_{eq}} = \frac{1}{4C_{in}f_{ck}}$$

A recently introduced chopper op-amp

ANALOG DEVICES

Precision, Ultralow Noise, RRIO, Zero-Drift Op Amp

Data Sheet **ADA4528-1/ADA4528-2**

Very low offset voltage

Note: residual offset and flicker noise shifted at the clock frequency

FEATURES

- Low offset voltage: 2.5 µV maximum
- Low offset voltage drift: 0.015 µV/°C maximum
- Low noise
  - 5.6 nV/√Hz at f = 1 kHz, A_V = +100
  - 97 nV p-p at f = 0.1 Hz to 10 Hz, A_V = +100
- Open-loop gain: 130 dB minimum
- CMRR: 135 dB minimum
- PSRR: 130 dB minimum
- Unity-gain crossover: 4 MHz
- Gain bandwidth product: 3 MHz at A_V = 100
- −3 dB closed-loop bandwidth: 6.2 MHz
- Single-supply operation: 2.2 V to 5.5 V
- Dual-supply operation: ±1.1 V to ±2.75 V
- Rail-to-rail input and output
- Unity-gain stable

APPLICATIONS

- Thermocouple/thermopile
- Load cell and bridge transducers
- Precision instrumentation
- Electronic scales
- Medical instrumentation
- Handheld test equipment

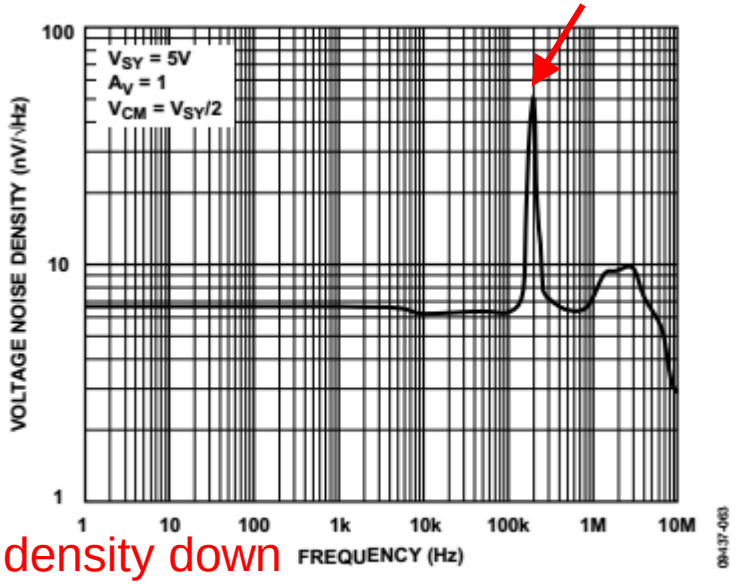


Figure 3. Voltage Noise Density vs. Frequency

Very low noise density down to low frequencies

PIN CONNECTION DIAGRAMS

NOTES
1. NIC = NO INTERNAL CONNECTION.

Figure 1. ADA4528-1 Pin Configuration, 8-Lead MSOP

Note: relatively high bias currents for a CMOS amplifier: effect of charge injection from the input switches

Note: relatively low input resistance (effect of alternating Vin and –Vin across the input capacitance)

V_{SY} = 2.5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 2.5 V		0.3	2.5	µV
		−40°C ≤ T_A ≤ +125°C, MSOP package			4	µV
		−40°C ≤ T_A ≤ +125°C, LFCSP package			4.3	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C, MSOP package		0.002	0.015	µV/°C
		−40°C ≤ T_A ≤ +125°C, LFCSP package			0.018	µV/°C
Input Bias Current	I_B			220	400	pA
		−40°C ≤ T_A ≤ +125°C			600	pA
Input Offset Current	I_{OS}			440	800	pA
		−40°C ≤ T_A ≤ +125°C			1	nA
Input Voltage Range			0		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	135	158		dB
		−40°C ≤ T_A ≤ +125°C	116			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 2.4 V	130	140		dB
		−40°C ≤ T_A ≤ +125°C	126			dB
ADA4528-1		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	125	132		dB
		−40°C ≤ T_A ≤ +125°C	121			dB
ADA4528-2		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	122	132		dB
		−40°C ≤ T_A ≤ +125°C	119			dB
Input Resistance						
Differential Mode	R_{INDM}			225		kΩ
Common Mode	R_{INCM}			1		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			15		pF
Common Mode	C_{INCM}			30		pF

AD 4528 equivalent block diagram (from AN-1114 application note of Analog Design)

Chopper modulation is applied only to the first stage

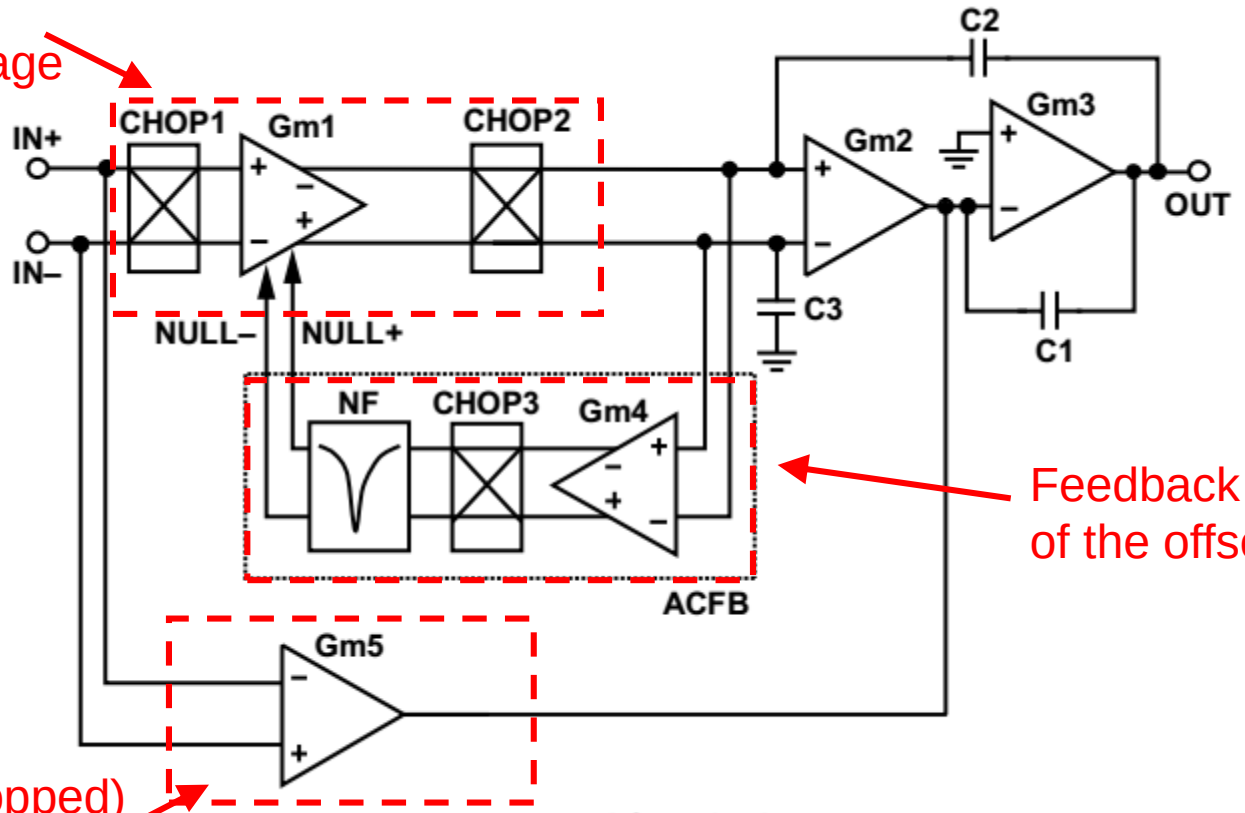


Figure 1. Amplifier Block Diagram

Feedback loop for reduction of the offset ripple

High frequency path (not chopped) to obtain a wide bandwidth