1 Advanced properties of CMOS current mirrors

1.1 Current Mirrors: Frequency response.

Current mirrors are often used to process signals in the form of variable currents. In these cases, it is important to know the frequency response between the input and the output currents. The typical configuration is shown in Fig.1.1. The input current is provided by an ideal current source, while the output current flows into the ideal voltage source V_{out}. In terms of small signal analysis, this means that we are considering the output short circuit current. In real cases, the output terminal of the mirror is connected to a non-zero load impedance, so that a current divider is formed by the output impedance of the mirror and the load impedance. Whenever the load impedance is much smaller than the mirror output impedance, we can consider that the whole output short circuit current actually flows into the load.

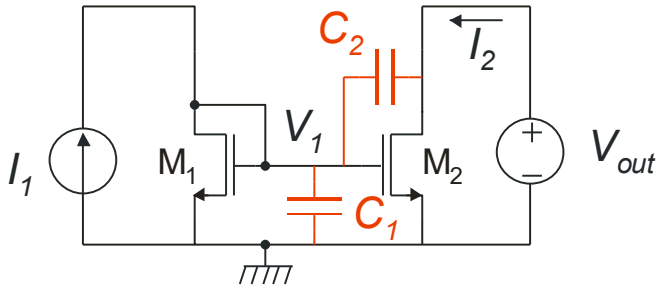

Fig.1.1. Simple MOSFET current mirror with parasitic capacitances.

In order to study the frequency response, the parasitic capacitors C_1 and C_2 shown in Fig. 1.1 should be taken into account. They are given by:

$$C_1 = C_{GS1} + C_{GS2} + C_{DB1}$$
$$C_2 = C_{GD2} \tag{1.1}$$

The small signal model of the mirror is shown in Fig.1.2, where the diode-connected device M_1 has been replaced by its equivalent resistance, given by the parallel of $1/g_{m1}$ with r_{d1}, which is nearly equal to $1/g_{m1}$

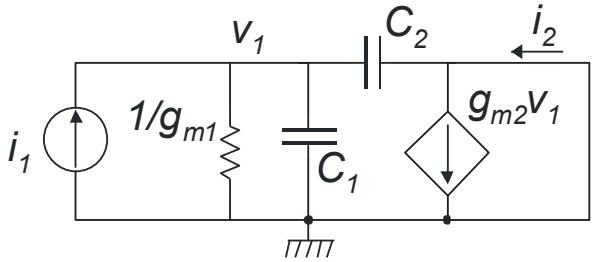

Fig. 1.2. Small signal equivalent circuit of a current mirror

The following expression for voltage v_1 and current i_2 can be easily found:

$$v_1 = i_1\left(\frac{1}{g_{m1} + s(C_1 + C_2)}\right) \tag{1.2}$$

$$i_2 = v_1 g_{m2} - v_1 s C_2 \tag{1.3}$$

Substituting v_1 into (1.3), we get the transfer function $A_I = i_2/i_1$ (small-signal current-gain of the mirror):

$$A_I = \left(\frac{g_{m2} - sC_2}{g_{m1} + s(C_1 + C_2)}\right) = \frac{g_{m2}}{g_{m1}}\left(\frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}\right) = A_I(0)\left(\frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}\right) \tag{1.4}$$

The pole (ω_p) and zero (ω_z) angular frequencies are given by:

$$\omega_p = \frac{g_{m1}}{C_1 + C_2} \cong \frac{g_{m1}}{C_1} \qquad \omega_z = \frac{g_{m2}}{C_2} \tag{1.5}$$

The approximation of ω_p is due to the fact that, considering (1.1), typically: $C_2 << C_1$. The ratio g_{m2}/g_{m1} is the DC gain of the mirror, indicated with $A_I(0)$, which, in the ideal case, is equal to the nominal gain k_M of the mirror, where $k_M = W_2L_1/W_1L_2$. Clearly, due to systematic (e.g. effect of r_{d1}) and random non idealities, the actual DC gain $A_I(0)$ and the nominal gain may be slightly different.

The frequency response of the current gain is then represented by the asymptotic curves shown in Fig.1.3 (bode plots), where it has been assumed that $A_I(0)$, is greater than one. Note that the zero is positive, so that it gives a negative phase contribution, like the pole. The total asymptotic phase delay of a current mirror is then 180°. When the frequency tends to infinity, v_1 tends to zero, and so does the current $g_{m2}v_1$. Therefore, the high frequency limit of the gain, $A_I(\infty)$, is due only to the capacitive current divider formed by C_1 and C_2, so that

$$|A_I(\infty)| = \frac{C_2}{C_1 + C_2} << 1 \tag{1.6}$$

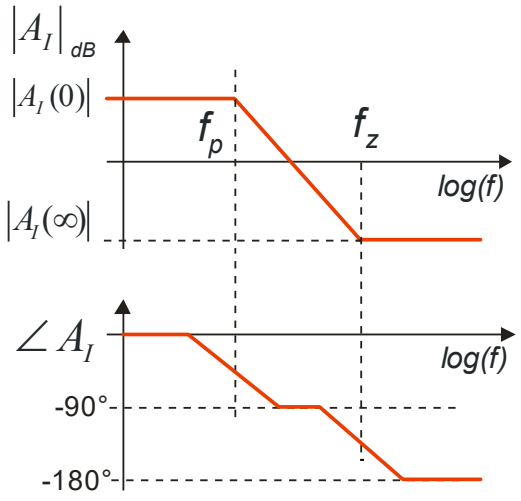

Fig. 1.3 Typical asymptotic magnitude and phase response of a current mirror.

As a result, if the DC gain of the mirror is greater than one or even slightly lower than one, the frequency of the pole is lower than that of the zero. Mirrors with a unity current gain represent the most frequent case of current mirror applications: they are characterized by a frequency response similar to that of Fig.1.3, with only the exception that $A_I(0)$ is 0 dB. Only in the case of mirrors designed to have a gain much smaller than one the pole and zero may be swapped along the frequency axis, as shown in Fig.1.4.

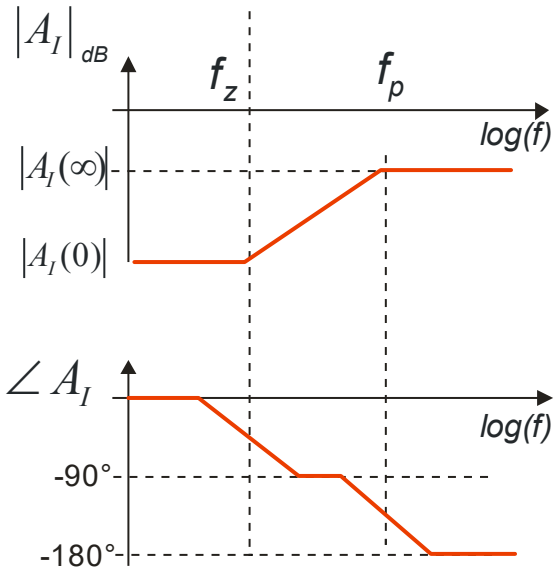

Fig.1.4. Frequency response of current mirror in the case that the nominal current gain is <<1

As mentioned above, in most cases the singularity with lower characteristic frequency is the pole, so that the upper frequency limit of the mirror is given by the pole frequency f_p.

Considering Eq. (1.5) and using the strong inversion approximation for g_{m1}:

$$f_p = \frac{\omega_p}{2\pi} \cong \frac{1}{2\pi}\frac{g_{m1}}{C_1} = \frac{1}{2\pi}\frac{\mu C_{OX}\frac{W}{L}(V_{GS}-V_t)}{C_1} \tag{1.7}$$

Neglecting C_{DB} with respect to $C_{GS1}+C_{GS2}$ in the expression of C_1, we get the expression:

$$f_p \cong \frac{1}{2\pi}\frac{\mu C_{OX}\frac{W_1}{L_1}(V_{GS}-V_t)}{\frac{2}{3}C_{OX}(W_1L_1+W_2L_2)} = \frac{\frac{3}{4\pi}\mu\frac{1}{L_1^2}(V_{GS}-V_t)}{\left(1+\frac{W_2L_2}{W_1L_1}\right)} = \frac{f_{T1}}{\left(1+\frac{W_2L_2}{W_1L_1}\right)} \tag{1.8}$$

Where f_{T1} is the transition frequency of M_1, i.e. the frequency at which the current gain of M_1 becomes one. Note that the actual pole frequency is slightly lower than the value given by (1.8), due to the fact that we have neglected the drain-body capacitance of M_1 and capacitance C_2, equal to C_{db2}.

In the case of a mirror with nominal unity current gain, M_1 and M_2 are identical, so that the upper band limit is half the transition frequency. For mirrors with current gains different from one, we need to know how M_1 and M_2 are designed. An important case is that of precision mirrors, where M_1 and M_2 have the same length. In this case, indicating with k_M the nominal current gain of the mirror, we have:

$$L_1 = L_2 \Rightarrow \begin{cases} k_M = \dfrac{W_2}{L_2}\dfrac{L_1}{W_1} = \dfrac{W_2}{W_1} \\ \dfrac{W_2 L_2}{W_1 L_1} = \dfrac{W_2}{W_1} = k_M \end{cases} \tag{1.9}$$

Therefore, for precision mirrors, (1.8) becomes:

$$f_p \cong= \frac{f_{T1}}{(1+k_M)} \tag{1.10}$$

To summarize:

- The frequency response of a current mirror is marked by a pole and a positive zero. The total asymptotic phase delay introduced by the pole-zero pair is 180°. This aspect should be carefully taken into account when current mirrors are present in the signal path. Critical stability issues may occur in feedback loops that include currant mirrors.
- In most current mirrors, including the frequent case of mirrors with unity nominal gain, the pole frequency is lower than the zero one, so that the upper frequency limit is given by f_p, which is of the same order of magnitude as the transition frequency of M_1.
- The transition frequency shows an inverse proportionality to L_1^2, so that mirrors formed by long MOSFETs have a poor frequency response. In order to improve the frequency response, V_{GS}-V_T should be made large, with obvious drawbacks in terms of minimum output voltage (V_{min}).
- If M_1 and M_2 have the same length, as typically occurs when precise current gains (k_M) are required, the pole frequency is given by f_T divided by $1+k_M$. Therefore: the higher the current gain, the lower the mirror bandwidth.
- Mirrors with a particularly low nominal DC gain may be marked by a zero frequency lower than the pole one ($f_z<f_p$). Since, in terms of phase delay, the zero behaves like the pole, the upper band limit will be given by the zero. This fact should be taken into account when designing feedback loops that include mirrors with a gain much lower than one.

1.2 Current Mirrors: noise.

The output current noise of a current mirror can be calculated with the small signal circuit of Fig. 1.5, where the noise currents i_{n1} and i_{n2} of M_1 and M_2, respectively, have been highlighted. Comparison with the circuit of Fig.1.1 shows that the input source I_1 has been removed, since here we are concerned with the effects of noise sources. The voltage source V_{out} has also been replaced with a short circuit to ground, since we are dealing only with small signals. Parasitic capacitances have been neglected since only noise components at frequencies much lower than the upper frequency limit are considered.

The output current is given by:

$$i_2 = i_{n2} - A_I(0) i_{n1} \tag{1.11}$$

The power spectral density (PSD) of the output current i_2, indicated with S_{Iout}, is given by:

$$S_{Iout}(f) = S_{In2}(f) + \left|A_I(0)\right|^2 S_{In1}(f) \quad \cong \quad S_{In2}(f) + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{In1}(f) \tag{1.12}$$

where S_{In1} and S_{In2} are the PSDs of i_{n1} and i_{n2}, respectively.

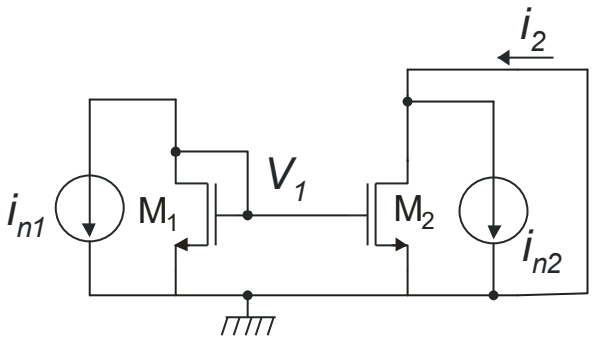

Fig.1.5. Current mirror with noise sources of the input and output device

In the case of thermal noise, the following expression for the MOSFET current noise PSD will be assumed:

$$S_{In}(f) = \frac{8}{3} kTg_m \qquad \text{(thermal noise component)} \tag{1.13}$$

where k is the Boltzmann constant and T the absolute temperature. Substituting (1.13) into (1.12) for both currents i_1 and i_2, the total thermal noise PSD of the output current (S_{ITh}) becomes:

$$S_{ITh}(f) = \frac{8}{3} kTg_{m2} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \frac{8}{3} kTg_{m1} = \frac{8}{3} kTg_{m2}\left(1 + \frac{g_{m2}}{g_{m1}}\right) \tag{1.14}$$

Considering that $g_{m2} / g_{m1} \cong A_I(0) \cong k_M$, Eq. (1.14) becomes:

$$S_{ITh}(f) = \frac{8}{3} kTg_{m2}\left(1 + k_M\right) \tag{1.15}$$

Substituting: $g_{m2}=I_{D2}/V_{TE2}=I_{out}/V_{TE2}$ we get:

$$S_{ITh}(f) = \frac{8}{3} kT \frac{I_{out}}{V_{TE2}}\left(1 + k_M\right) \tag{1.16}$$

In the case of flicker noise, the following expression of the MOSFET current noise PSD can be adopted:

$$S_{In}(f) = g_m^2 \frac{N_f}{WL} \frac{1}{f} \qquad \text{(flicker noise component)} \tag{1.17}$$

where N_f is the flicker noise constant (process parameter). The flicker component (S_{IF}) of the output noise PSD is given by:

$$\begin{aligned} S_{IF}(f) &= g_{m2}^2 \frac{N_f}{W_2 L_2} \frac{1}{f} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 g_{m1}^2 \frac{N_f}{W_1 L_1} \frac{1}{f} = \\ &= \frac{g_{m2}^2 N_f}{f}\left(\frac{1}{W_2 L_2} + \frac{1}{W_1 L_1}\right) = g_{m2}^2 \frac{N_f}{W_2 L_2}\left(1 + \frac{W_2 L_2}{W_1 L_1}\right)\frac{1}{f} \end{aligned} \tag{1.18}$$

In the case that $L_1=L_2$, considering relationships (1.9), Eq.(1.18) can be rewritten:

$$S_{IF}(f) \;=\; g_{m2}^2 \frac{N_f}{W_2 L_2}\left(1 + k_M\right)\frac{1}{f} \tag{1.19}$$

Similarly to the case of thermal noise, we write g_{m2} as a function of I_{out} and V_{TE2}, obtaining:

$$S_{IF}(f) \;=\; \frac{I_{out}^2}{V_{TE2}^2} \frac{N_f}{W_2 L_2}\left(1 + k_M\right)\frac{1}{f} \tag{1.20}$$

Equations (1.16) and (1.20) give the thermal and flicker components of the output currents. We will discuss them later. Here, we will focus on another important performance parameter, which is pertinent when the mirror is used to process signals. This parameter is the dynamic range (DR), given by the ratio:

$$DR = \frac{i_{out-FS}}{i_{np-p}} \tag{1.21}$$

where $i_{out\text{-}FS}$ is the full scale excursion of the input current, while $i_{np\text{-}p}$ is the peak-to-peak value of the output noise current. Figure 1.6 shows a possible time diagram of the output current, including the signal (supposed to be sinusoidal) superimposed to a quiescent value $I_{out\text{-}Q}$ (operating point current).

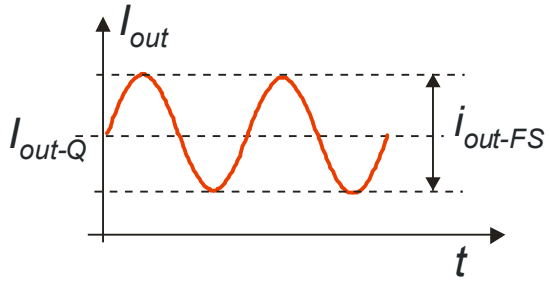

Fig.1.6. Quiescent and signal components of the output current

It can be easily understood that the theoretical maximum full scale current is $2I_{out\text{-}Q}$. However, to reach this value we should accept that the mirror current gets very close to zero when the signal is at its negative peaks. Generally, this is not possible, since the g_m of the input devices would also tend to zero and, considering Eq.(1.5), the singularities (pole and zero) would shift to very low frequencies, thus slowing down the mirror response. The consequence would be high distortion and prolonged settling times. For this reason, the full scale current should be represented by:

$$i_{out-FS} = \alpha I_{out-Q} \tag{1.22}$$

with $\alpha < 2$. In order to guarantee a wide margin and moderate parameter variations, $\alpha \leq 1$. If a value of exactly equal to 1 is used, then the DR coincides with the ratio between the quiescent current and the current noise. This is pertinent when the mirror has only to provide a constant current for biasing purposes. In this particular case, the DR indicates how many times the noise is smaller than the output d.c. current.

The peak-to-peak noise can be approximated to:

$$i_{np-p} = 4i_{n-rms} = 4\sqrt{\int_{f_L}^{f_H} S_{Iout}(f)df} \tag{1.23}$$

where f_L and f_H are the lower and upper frequency limits of the signal frequency band, respectively. We will consider two different cases, corresponding to the presence of pure flicker or pure thermal noise.

In the case of thermal noise, using (1.16):

$$(DR)^2 = \frac{i_{out-FS}^2}{i_{n-pp}^2} = \frac{\alpha^2 I_{out-Q}^2}{16\frac{8}{3}kT\frac{I_{out-Q}}{V_{TE2}}(1+k_M)B_S} = \frac{3}{128}\frac{V_{TE2}\alpha^2 I_{out-Q}}{kTB_S(1+k_M)} \tag{1.24}$$

where B_S=f_H-f_L.

In the case of flicker noise, using Eq.(1.20):

$$(DR)^2 = \frac{\alpha^2 I_{out-Q}^2}{16\frac{I_{out-Q}^2}{V_{TE2}^2}\frac{N_f}{W_2L_2}(1+k_M)\ln\left(\frac{f_H}{f_L}\right)} = \frac{\alpha^2 V_{TE2}^2 W_2 L_2}{16N_f(1+k_M)\ln(f_H/f_L)} \quad (1.25)$$

The results obtained so far are summarized in Table 1.1.

	Output current PSD	DR^2
Thermal Noise	$\frac{8}{3}kT\frac{I_{out}}{V_{TE2}}(1+k_M)$	$\frac{3}{128}\frac{V_{TE2}\alpha^2 I_{out-Q}}{kTB_S(1+k_M)}$
Flicker noise	$\frac{I_{out}^2}{V_{TE2}^2}\frac{N_f}{W_2L_2}(1+k_M)\frac{1}{f}$	$\frac{\alpha^2 V_{TE2}^2 W_2 L_2}{16N_f(1+k_M)\ln(f_H/f_L)}$

Table 1.1

Final considerations:

- The output noise PSD can be written as the product of the noise PSD of the output transistors, multiplied by a factor depending on the mirror gain. High current gains (k_M) result in higher noise factors. Currents obtained by magnification of a much smaller current are more prone to noise than currents obtained by mirroring a current of the same value.

- For both thermal and flicker noise, higher currents are accompanied by higher noise levels.

- For both thermal and flicker noise, the higher V_{TE}, the lower the noise. This means that the best option in terms of noise is biasing currents mirror in strong inversion with large V_{GS}-V_T values. This recommendation improve also the frequency response but leads to worse voltage ranges.

- As far as DR is concerned, both thermal and flicker noise benefit from large V_{TE} values. The behavior is different in terms of quiescent current: the DR due to thermal noise can be increased by using large bias currents ($I_{out\text{-}Q}$), while, in the case of pure flicker noise, the DR is independent of $I_{out\text{-}Q}$ and the only way to improve DR is using large gate areas (WL) for both M_1 and M_2.

1.3 Noise in cascode current mirrors.

The small signal circuit of a Cascode mirror, with the noise current sources of all MOSFETs, is shown in Fig.1.7. It is necessary to calculate the effect of each noise source on the output current i_2.

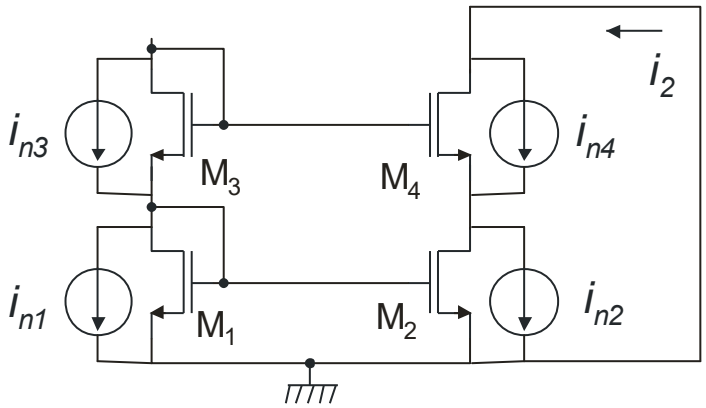

Fig.1.7. Cascode current mirror with noise sources

Current i_{n2}: It is split into two components: one flowing into the drain of M2 (resistance r_{d2}), the other into the source of M_4 (resistance $1/g_{m4}$). Only the latter affects i_2. The contribution to i_2 is then:

$$i_2(i_{n2}) = i_{n2}\frac{r_{d2}}{r_{d2}+1/g_{m4}} = \frac{i_{n2}}{1+\dfrac{1}{g_{m4}r_{d2}}} \cong i_{n2} \tag{1.26}$$

Current i_{n1}: It flows from the source to the drain of M_1, and it is mirrored into M_2 (multiplied by the current gain A_I of the mirror, nearly equal to $=g_{m2}/g_{m1}$). This current is transferred from the drain of M_2 to the output with a mechanism similar to that of i_{n2}, the difference being only the sign. Therefore:

$$i_2(i_{n1}) \cong -A_I i_{n1} \tag{1.27}$$

Current i_{n4}: This source has not a grounded terminal, so that it should be treated in different way from i_{n1} and i_{n2}. To simplify the analysis, we can split this source into two equivalent sources i_{n4}' and i_{n4}'', both with a grounded terminal, as shown in Fig. 1.8.

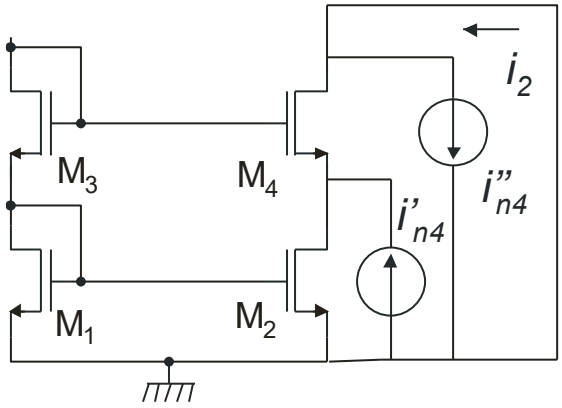

Fig.1.8. Splitting of floating current source i_{n4} into two components referred to ground

Clearly, the condition to be respected is that i_{n4}' and i_{n4}'' are equal to i_{n4}. In this way, we can separately consider the effects of the two sources and then sum up the effects. Source i_{n4}'', being connected to the output terminal (which is shorted to ground), gives a contribution to i_2 equal to its value, i.e. i_{n4}. Source i_{n4}'produces the same effect as i_{n2}, so that the total effect of i_{n4} is:

$$i_2(i_{n4}) = i_{n4}''-i_{n4}'\frac{r_{d2}}{r_{d2}+1/g_{m4}} = i_{n4}\left(1-\frac{r_{d2}}{r_{d2}+1/g_{m4}}\right) = \frac{i_{n4}}{1+g_{m4}r_{d2}} \tag{1.28}$$

Current i_{n3}. This current flows only into the diode-connected MOSFET M_3. The effect is an increase of M_3 V_{GS} equal to $-i_{n3}/g_{m3}$. This variation is applied to the gate of M_4, which operates like a source follower, loaded by M_2, i.e. by r_{d2}. The variation on M_2 drain voltage is then:

$$v_{d2} = -\frac{i_{n3}}{g_{m3}}\frac{g_{m4}r_{d2}}{(1+g_{m4}r_{d2})} \tag{1.29}$$

Thus, the contribution to i_2 is v_{d2}/r_{d2}, equal to:

$$i_2(i_{n3}) = -i_{n3}\frac{g_{m4}}{g_{m3}}\frac{1}{(1+g_{m4}r_{d2})} \tag{1.30}$$

Note that cascode Mirrors are generally designed in such a way that $\beta_2/\beta_1=\beta_3/\beta_4$, in order to make the overdrive voltages of M3 and M4 equal. In these conditions $g_{m4}/g_{m3}=g_{m2}/g_{m1}=A_I(0)$

Final considerations.

- The effect of MOSFETS M_1-M_2 is practically equal to that of a simple (non-cascode) current mirror, that is Eq.(1.11) and the following discussion are applicable to also noise currents i_{n1} and i_{n2}.

- The noise currents of M_3 and M_4 reach i_2 through a coefficient $1/(1+g_{m4}r_{d2})$, therefore, as long as $g_{m4}r_{d2} >> 1$, their effects are strongly attenuated. As a result, their contribution can be neglected in most practical cases.

1.4 Wide swing cascode with precise current gain.

Conventional cascode mirrors based on the topology of Fig. 1.7 suffer from two important drawbacks, namely (i) relatively high minimum output voltage ($V_{min}=V_{GS}+V_{DSAT}$) and (ii) quite high input voltage ($V_{in}=2V_{GS}$). The six MOSFET mirror shown in Fig. 1.9 solves the problem of the output voltage range, since V_{min} can be designed to be as small as $2V_{DSAT}$. Unfortunately, its precision is poor, since M_2 and M_1 has different V_{DS}. Furthermore, the input voltage is still $2V_{GS}$.

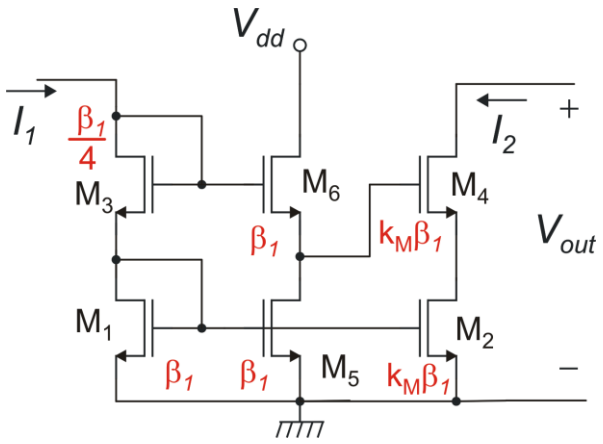

Fig.1.9. Low precision, wide swing cascode current mirror

The cascode mirror shown in Fig.1.10 (a) solves all these problems. It requires an auxiliary voltage, V_k, to bias the gates of M_3 and M_4. To study this circuit, we can start by writing V_{DS1} and V_{DS2}:

$$\begin{aligned} V_{DS1} &= V_k - V_{GS3} \\ V_{DS2} &= V_k - V_{GS4} \end{aligned} \tag{1.31}$$

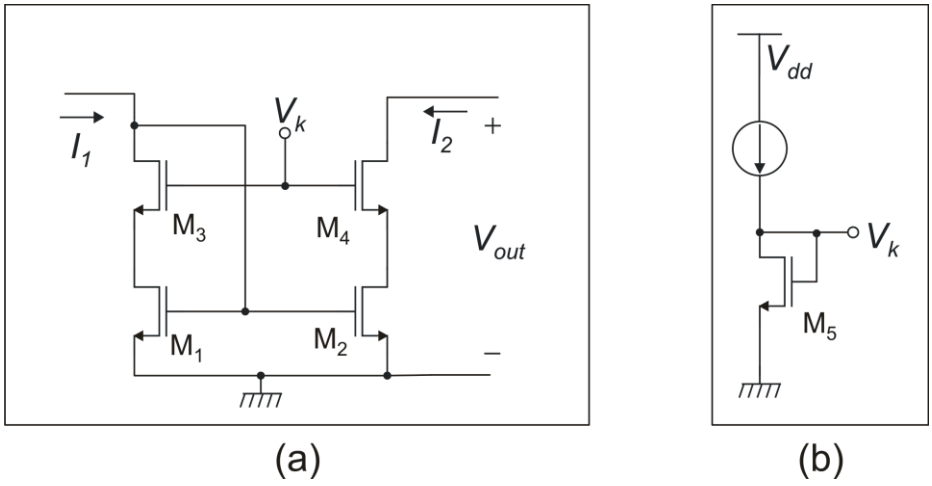

Fig.1.10. (a) High precision, wide swing cascode current mirror with low input voltage. (b) Generation of bias voltage V_K

Choosing $\beta_4/\beta_3=\beta_2/\beta_1=k_M$, we obtain $V_{GS3}=V_{GS4}$, as in a conventional cascode, so that $V_{DS1}=V_{DS2}$. This relationship guarantees that the mirror is precise, in the sense that the actual current gain is equal to the ratio β_2/β_1. Voltage V_k should be chosen to keep M_1 and M_2 in saturation region. Therefore:

$$V_k \geq V_{DSAT2} + V_{GS4} \tag{1.32}$$

Voltage V_k can be properly chosen to make V_{DS1} and V_{DS2} close to the transition to triode region, so that:

$$V_{DS2} \cong V_{DSAT2} = V_{GS2} - V_t \quad \Rightarrow \quad V_{\min} \cong V_{DSAT2} + V_{DSAT4} \tag{1.33}$$

In this way, V_{min} is only equal to $2V_{DSAT}$. The condition on V_k becomes:

$$V_k = V_{DS2} + V_{GS4} = (V_{GS} - V_t)_2 + (V_{GS} - V_t)_4 + V_{t4} \tag{1.34}$$

Voltage V_k can be produced by the circuit shown in Fig.1.10 (b). Considering Eq.(1.34) we can write:

$$V_k = V_{GS5} = V_{t5} + (V_{GS} - V_t)_5 = (V_{GS} - V_t)_2 + (V_{GS} - V_t)_4 + V_{t4} \tag{1.35}$$

Note that the source of M_5 is grounded, while M_4 source is at potential V_{DS2}, which, being close to V_{DSAT2}, is of the order of a few hundred millivolts. Therefore, the body effect on V_{t4} is small and we can consider that $V_{t4} \cong V_{t5}$. Then:

$$(V_{GS} - V_t)_5 = (V_{GS} - V_t)_2 + (V_{GS} - V_t)_4 \tag{1.36}$$

Current I_{bias} and M_5 aspect ratio (W/L) should be properly designed to obtain equality (1.36). Voltage V_k should also keep M_3 in saturation region. Note that $V_{D3}=V_{GS1}$. Therefore, we must guarantee that:

$$V_{D3} = V_{GS1} \geq V_k - V_{t3} \quad = \; V_k - V_{t4} \tag{1.37}$$

where $V_{t3}=V_{t4}$ derive from the property $V_{S3}=V_{S4}$. Substituting the expression of V_k from (1.35) we obtain the condition:

$$V_{GS1} \geq \left(V_{GS}-V_t\right)_1 + \left(V_{GS}-V_t\right)_3 \tag{1.38}$$

which can be further simplified in:

$$V_{t1} \geq \left(V_{GS}-V_t\right)_3 \tag{1.39}$$

With the typical value of the threshold voltages in CMOS processes (hundred millivolts), condition (1.39) can be easily satisfied by setting $(V_{GS}\text{-}V_t)_3$ = 100 mV, i.e. by biasing M3 at the boundary between strong and weak inversion.

Finally, we note that the input voltage is simply equal to V_{GS1}, like in simple current mirrors.

Final considerations.

- The wide-swing cascode current mirror shown in Fig.1.10 offers a low V_{min} ($V_{min}=2V_{DSAT}$), relatively low input voltage ($V_{in}=V_{GS}$), and also a precise current gain.
- This mirror requires accurate design in order to satisfy (1.33) over the whole range of input currents.