Analog to Digital Converters

- **ADC general aspects**
  - Applications, quantization error and static non idealities (offset, gain error, DNL and INL)
  - Nyquist-rate and Oversampled ADCs
  - Quantization noise: power and power spectral density, SQNR
  - Dynamic non idealities (SNR, SINAD, SFDR) and ENOB parameter
- **Nyquist-rate ADCs architectures, emphasis on the SAR ADC**
- **Effects of oversampling (OSR) on quantization noise**
- **The dithering technique**
- **Delta-Sigma ADCs:**
  - Delta-Sigma modulation principle
  - Analysis of a first-order modulator: signal and noise transfer functions, shaping, output noise and SQNR
  - Switched-capacitor implementation with a single-bit quantizer
  - Increasing the modulator order

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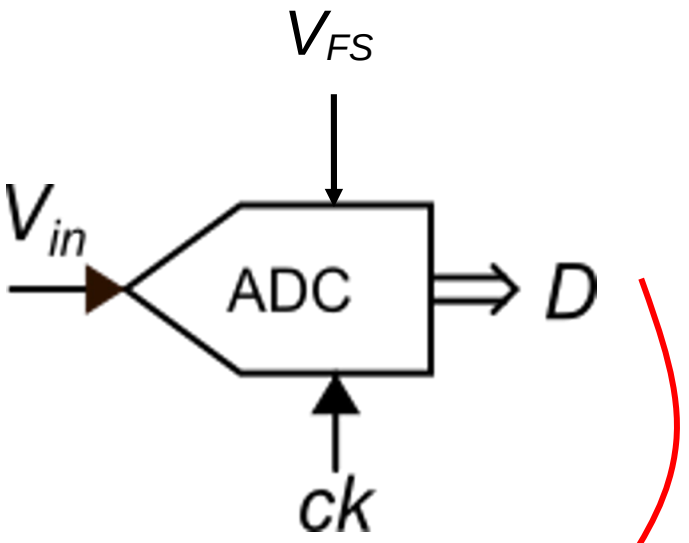
ADC applications

The ADC mirrors the DAC operation, hence, usually the same applications requiring a DAC also require an ADC. This is strictly true when a feedback or a control is needed to monitor the DAC output

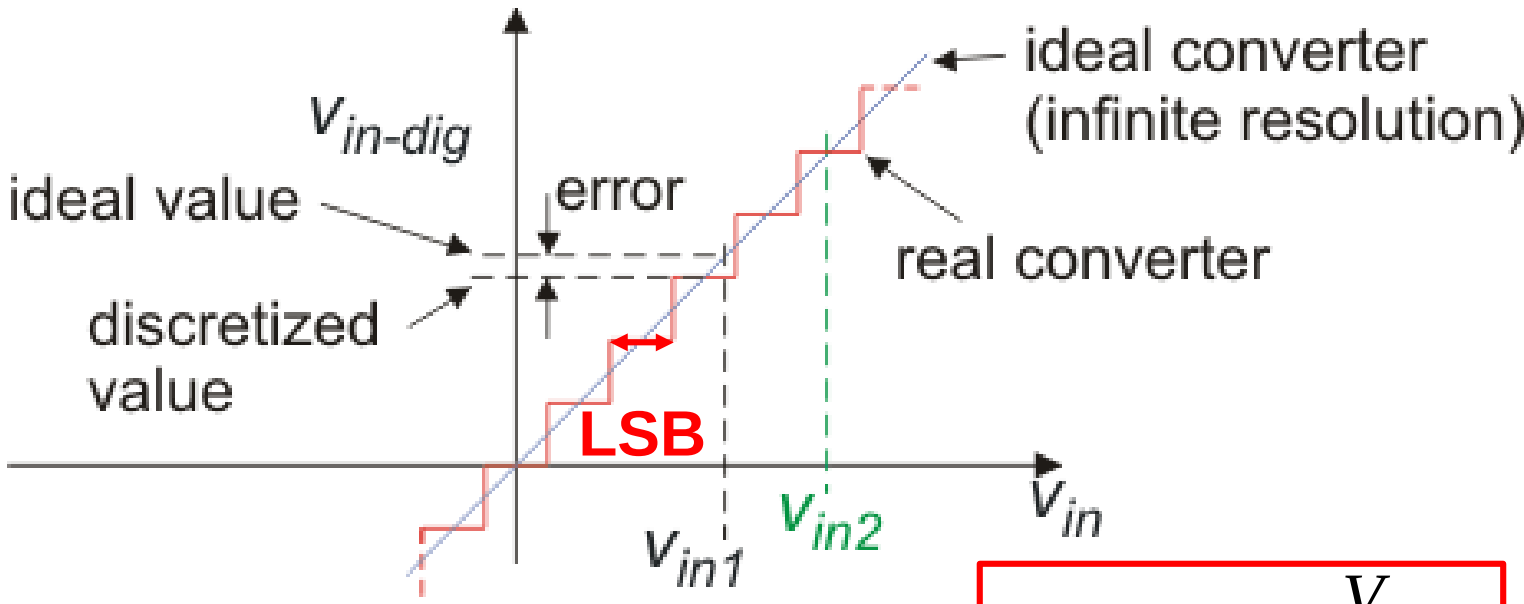
- **Measurements and data acquisition**, from low-frequency to high frequency applications (wearables, sensors, IoT, automotive, data-link communications)
- **Industrial applications** (robotics, control systems, PLCs, …)
- **Commercial electronics** (mobile phones, video and audio devices, microcontrollers …)

Analog to Digital Converters: ideal characteristics



$$v_{in\text{-}dig} = V_{MIN} + \frac{V_{FS}}{2^n} D$$

The digital output D can be referred to input by the action of an ideal DAC, whose full scale (V_{FS}) is matched with that of the ADC

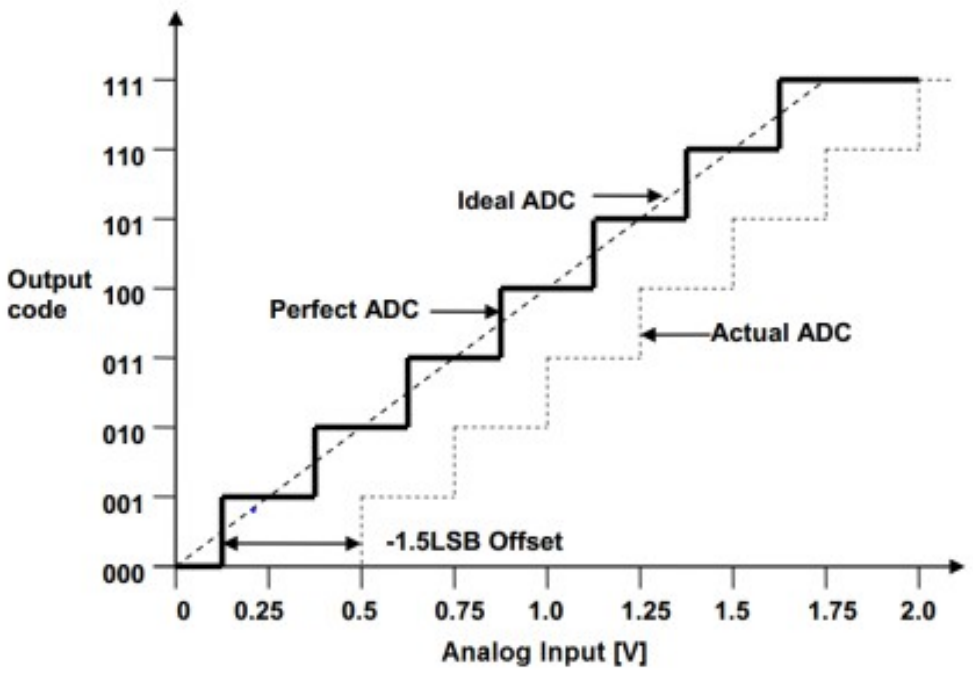


$$\Delta \equiv LSB = \frac{V_{FS}}{2^n}$$

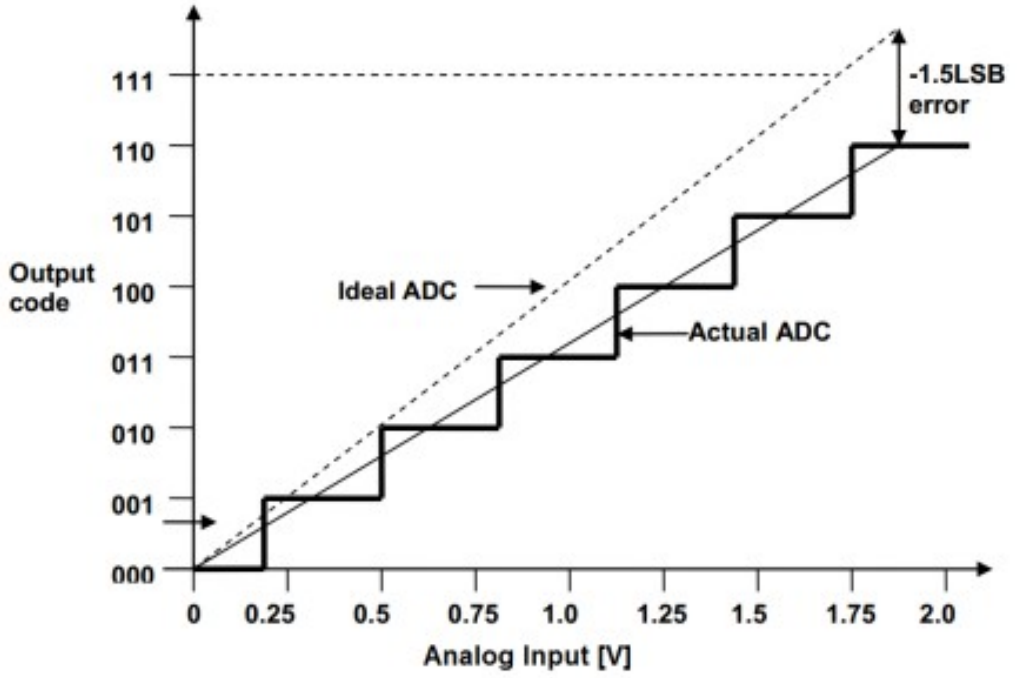
The characteristic of an n-bit ADC with no offset, gain, and non-linearity errors (only quantization errors): $v_{in\text{-}dig}$ is the best approximation of v_{in}, given n

ADCs Static Parameters: end-point errors

- **Offset error:** difference between the actual ADC characteristic and the perfect ADC characteristic, evaluated at the zero transition



- **Gain error:** difference between the last step midpoint of the actual ADC and the last step midpoint of the ideal ADC, after the compensation of the offset error



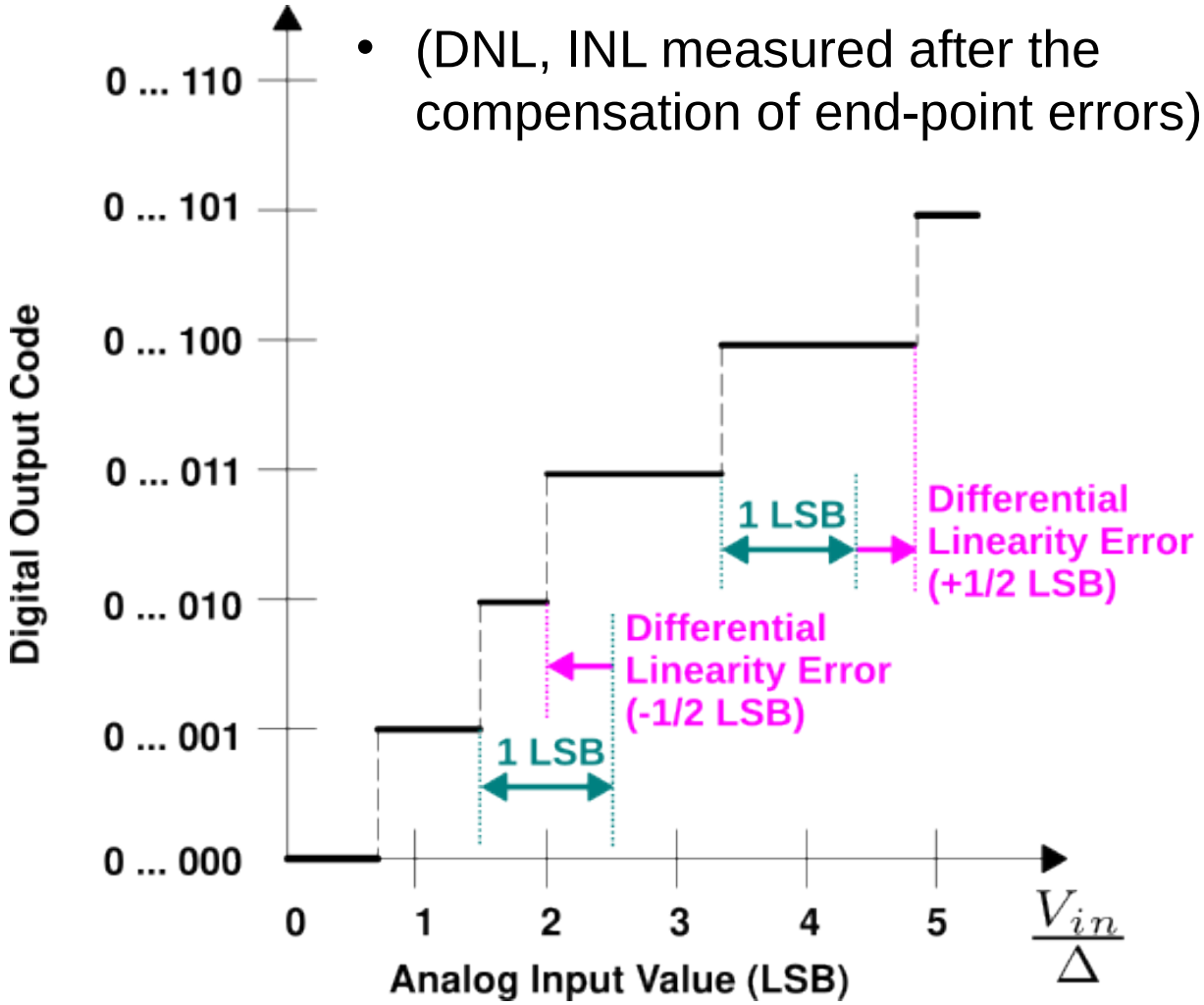
As in DACs, offset and gain are **end-points errors**, and are, generally easily corrected

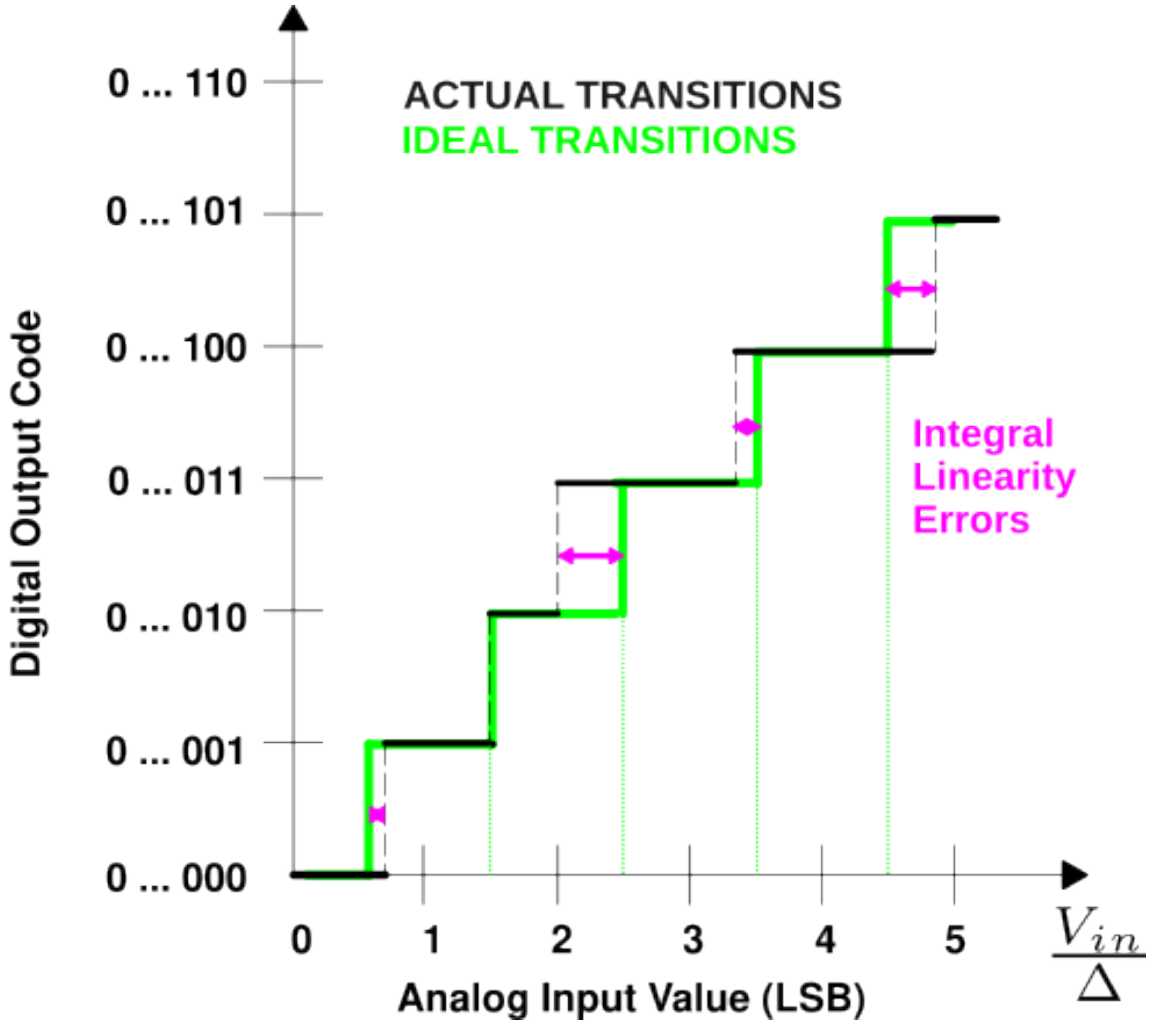
P. Bruschi – Design of Mixed Signal Circuits

http://ww1.microchip.com/downloads/en/appnotes/atmel-8456-8-and-32-bit-avr-microcontrollers-avr127-understanding-adc-parameters_application-note.pdf

ADCs Static Parameters: DNL, INL

- (DNL, INL measured after the compensation of end-point errors)





As in DACs, INL and DNL are of major concern, since they introduce distortion

ADCs – Static Parameters

AD9224

Typical Performance Characteristics (AVDD, DVDD = +5 V, F_S = 40 MHz [50% duty cycle] unless otherwise noted.)

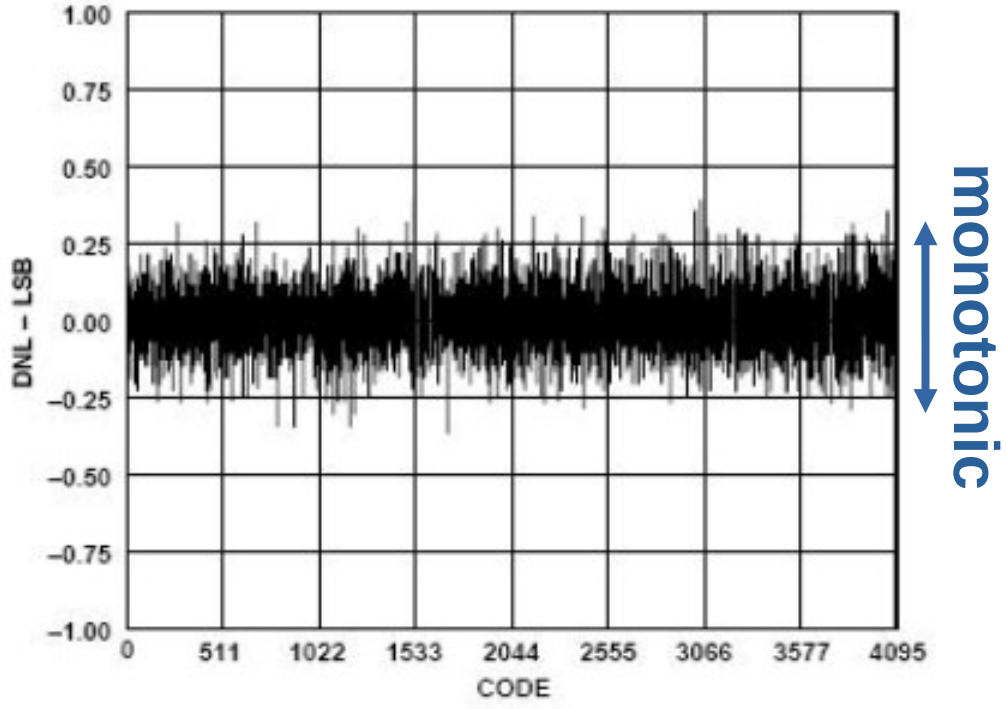


Figure 2. Typical DNL

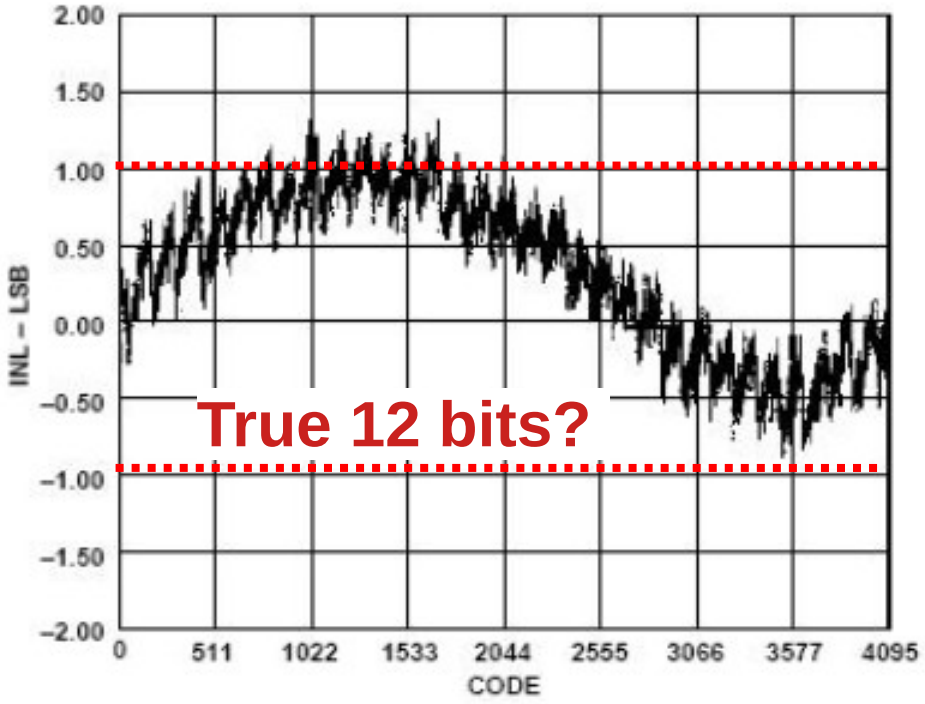
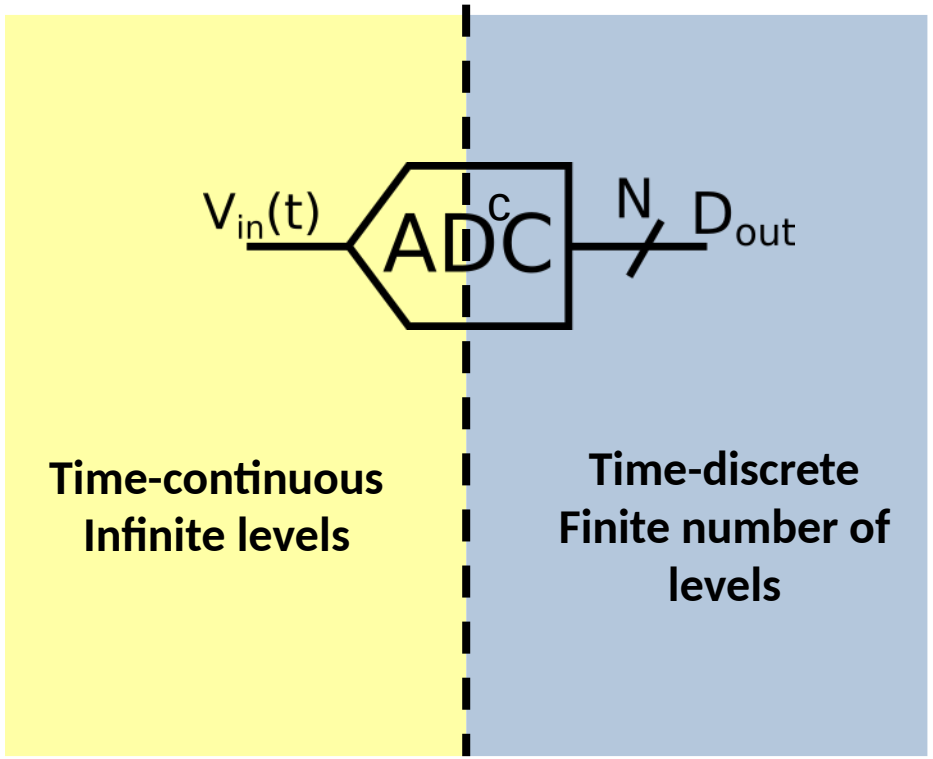


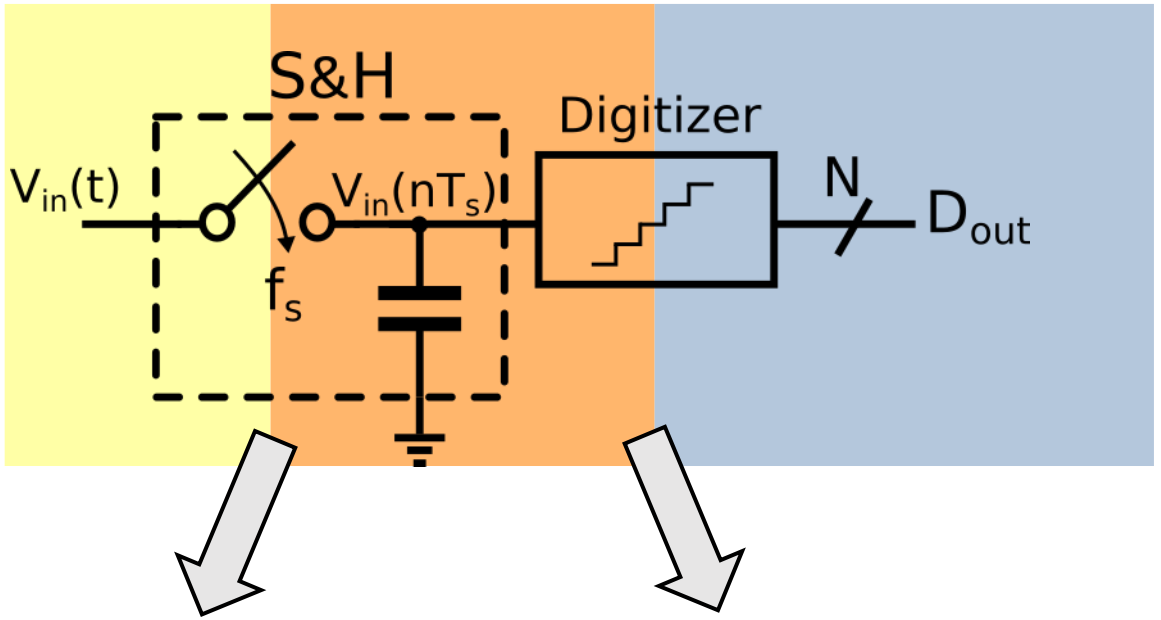
Figure 5. Typical INL

The ADC has 4096 distinct levels (a higher output code always implies a higher input), however the readout code is affected by an uncertainty of ~1 LSB = 5V/4096 = +/- 1.22 mV

Analog to Digital Converters: sampling process



Analog-to-Digital converter



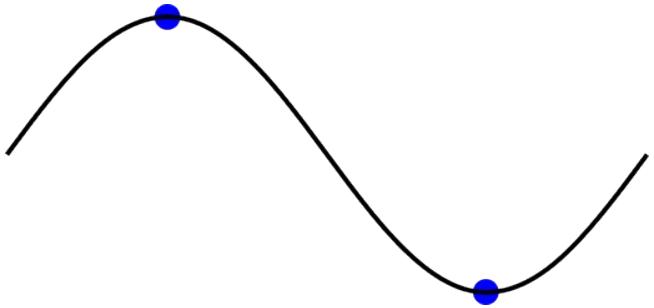
Sampling process:
Nyquist-Shannon sampling theorem (Aliasing): ideally, no information is lost

Quantization process:
Loss of information → Quantization noise

$V_{in}(t)$, comprising the intended input signal + any other unintended signal (couplings, noise) **must be band-limited** by a preceding CT anti-aliasing filter

Nyquist-Rate vs. Oversampling ADCs

Nyquist Rate ADC:

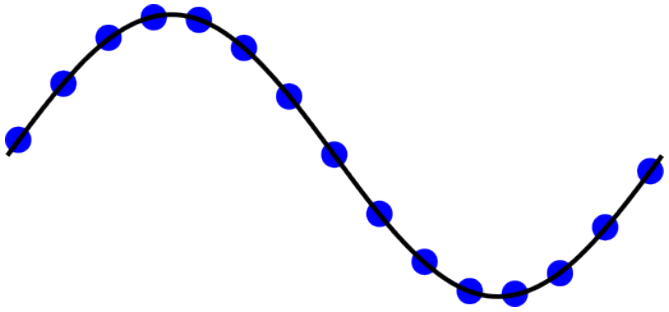


$$f_S \cong 2B_S$$

$$f_S \cong f_{s-Nyq}$$

No redundant information:
The output code depends only on the last conversion.
Previous conversions do not affect the present code

Oversampling ADC:

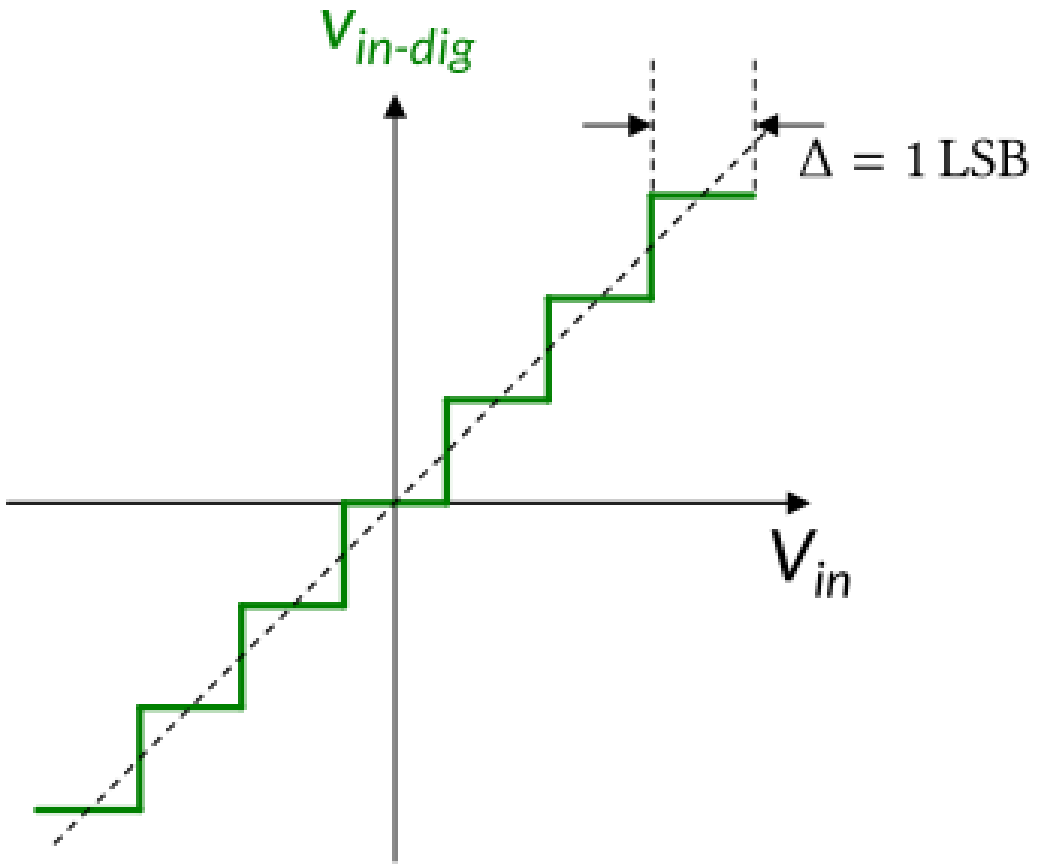


$$f_S >> 2B_S$$

$$f_S \gg f_{s-Nyq}$$

Information is redundant:
The output code at each sample time contains information also of the previous history of sampled data.

ADC quantization noise power

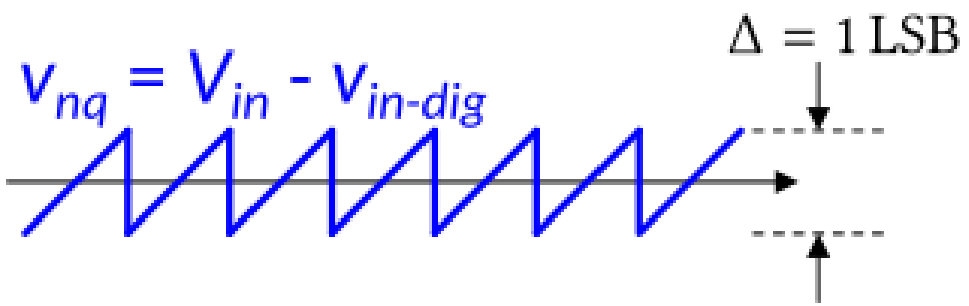


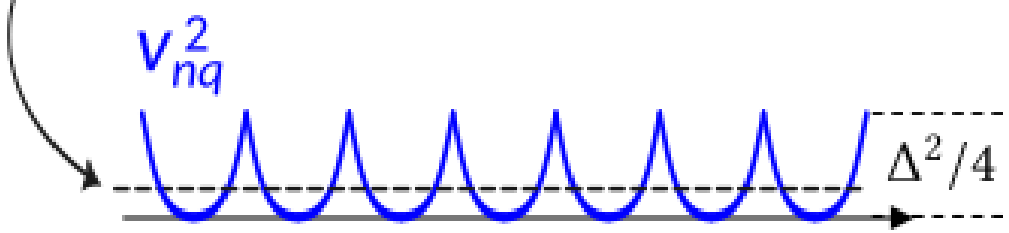
The expression of the quantization noise assumes that the input signal **uniformly "explores"** all the codes

Root-mean squared: Quantization noise power (V^2):

+1 bit → LSB halved → power/4

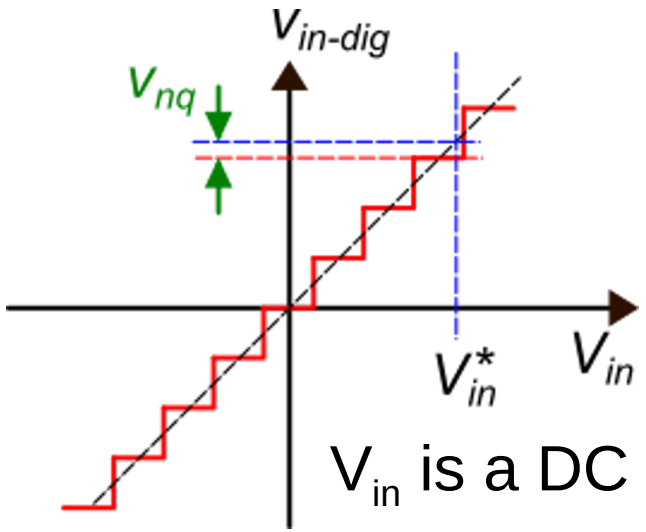
$$\langle v_{nq}^2 \rangle = \frac{\Delta^2}{12}$$





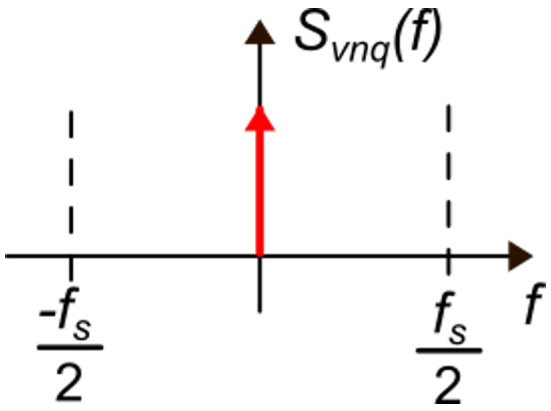
Quantization noise in the frequency domain

Since the ADC samples the input data, the output frequency domain is $[-f_s/2,+f_s/2]$



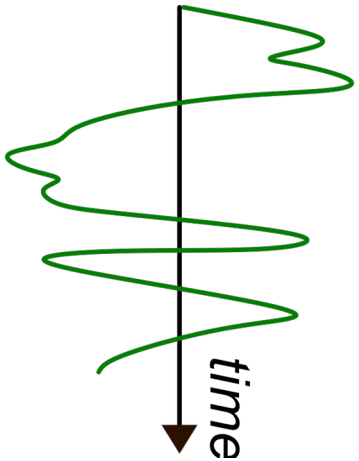
V_{in} is a DC signal

The v_{nq} spectrum is a Dirac delta

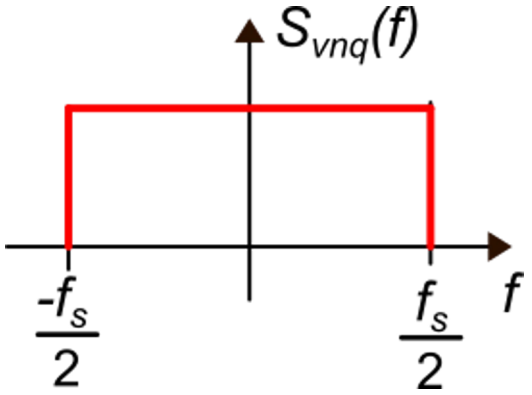


Two extreme cases:
In both cases, the power (area) is

$$\left\langle v_{nq}^2 \right\rangle = \frac{\Delta^2}{12}$$

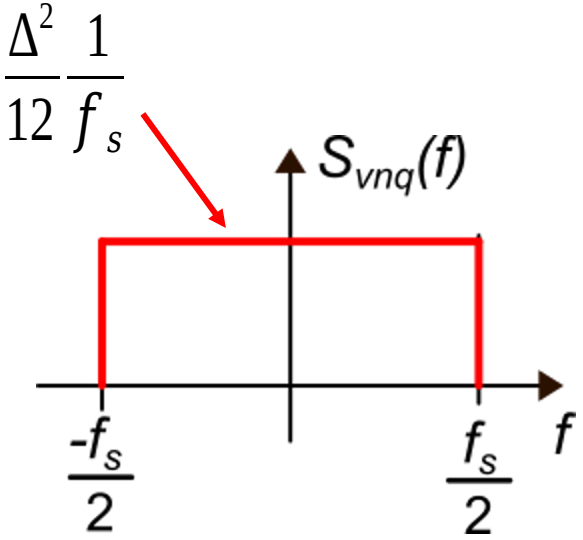


V_{in} is fast-varying signal of magnitude >> LSB



uniform distribution

The uniform power spectral density (PSD) model for the quantization noise



$$\Delta \equiv LSB = \frac{V_{FS}}{2^n}$$

This model is very useful and simple **but should be applied with much care.**

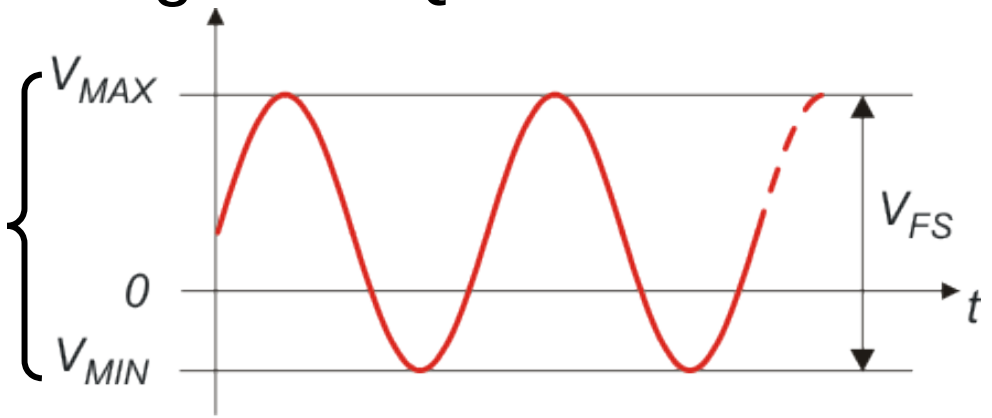
In real cases, the quantization noise depends on the input signal, and so does its spectrum.

The uniform spectral density model is acceptable when the input signal has **magnitude** and/or **frequency** such that the output levels are changed in a **fast** and almost **random** way.

This happens when the average time spent by the signal on a single level is short (of the order of the sampling time). **This condition is know as "busy" signal**

Signal to Quantization Noise Ratio (SQNR)

Input range of the ADC



Power of an input tone at maximum full scale

$$P_{MAX} = \frac{V_{FS}^2}{8}$$

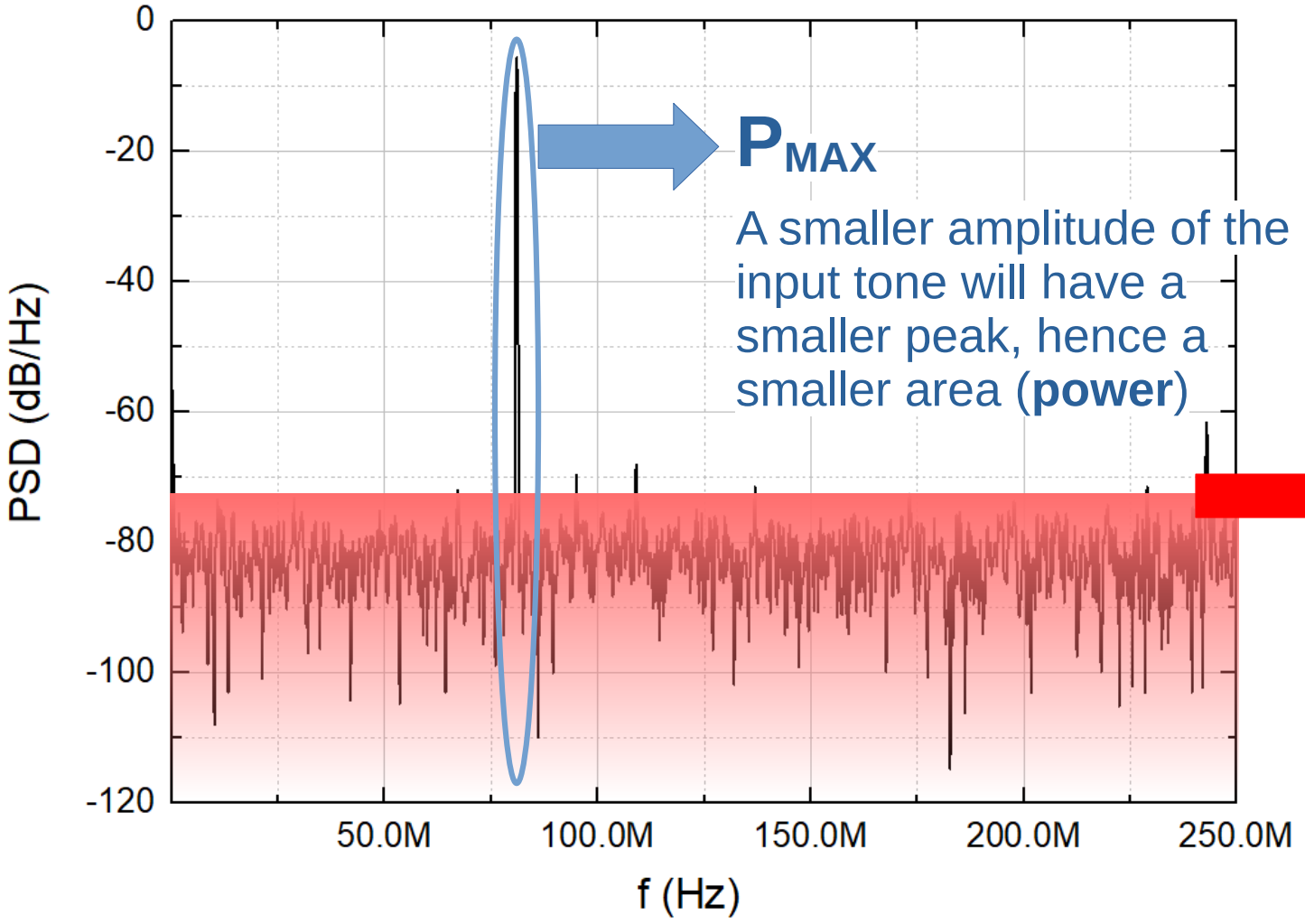
Quantization noise power:

$$\langle v_{nq}^2 \rangle = \frac{\Delta^2}{12}$$

$$\text{SQNR} = \frac{P_{max}}{\langle v_{nq}^2 \rangle} = \frac{V_{FS}^2}{8}\frac{12}{\Delta^2} = \frac{V_{FS}^2}{8}\frac{12 \cdot 2^{2n}}{V_{FS}^2} = \frac{3}{2} \cdot 2^{2n}$$

$$SQNR_{dB} = 10\log_{10}(SQNR) \cong 6.02n + 1.76$$

Signal to Quantization Noise Ratio (SQNR)



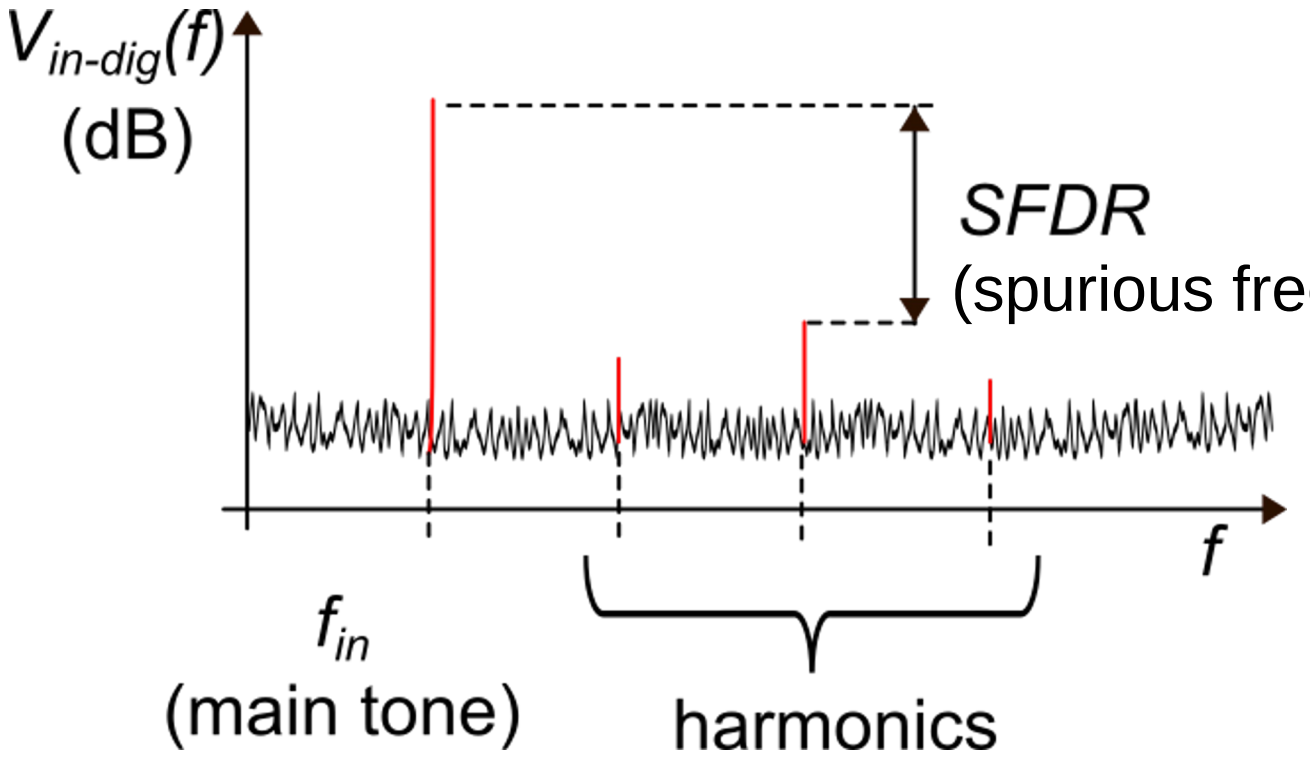
$$\mathrm{SQNR} = \frac{P_{max}}{\langle v_{nq}^2 \rangle}$$

Quantization noise power.

However in real ADCs, there is also **physical (electrical) noise** and **distortion.**

Each phenomenon has its own characteristic fingerprint in the PSD

Signal to Noise and Distortion Ratio (SINAD)



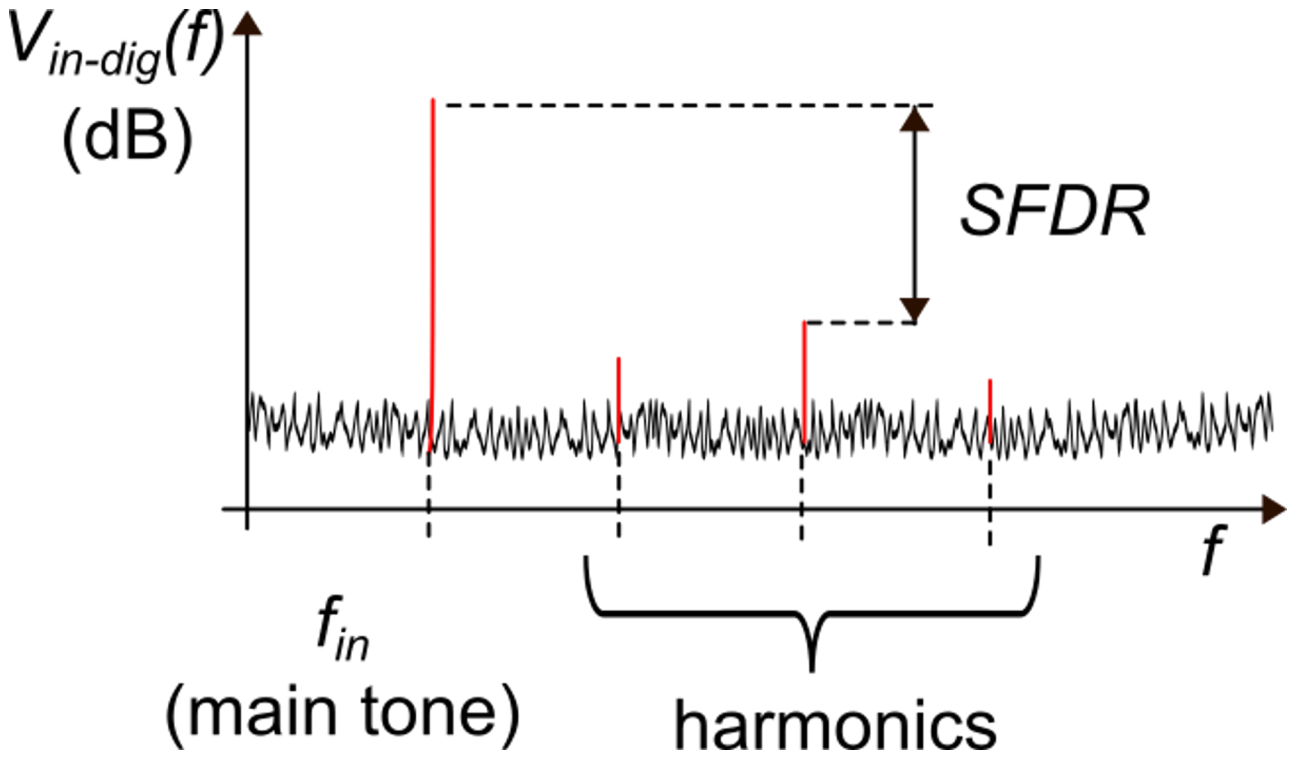
P_D=total power of the harmonics (except the main tone): clearly identified in the PSD

$$SINAD = \frac{P_{MAX}}{\langle v_n^2 \rangle + P_D}$$

Also indicated as SNDR

Quantization and electrical noise: they are both broadband, hence undistinguishable

Effective Number Of Bits (ENOB)



P_D=total power of the harmonics (except the main tone)

$$SINAD = \frac{P_{MAX}}{\langle v_n^2 \rangle + P_D}$$

$$SQNR_{dB} = 10\log_{10}(SQNR) \cong 6.02n + 1.76$$

$$SINAD_{dB} \cong 6.02 \cdot ENOB + 1.76$$

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02}$$

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Nyquist rate ADCs

For a N-bit ADC:

Direct conversion:
- Flash converters

1 cycle of comparison
fast but with low resolution

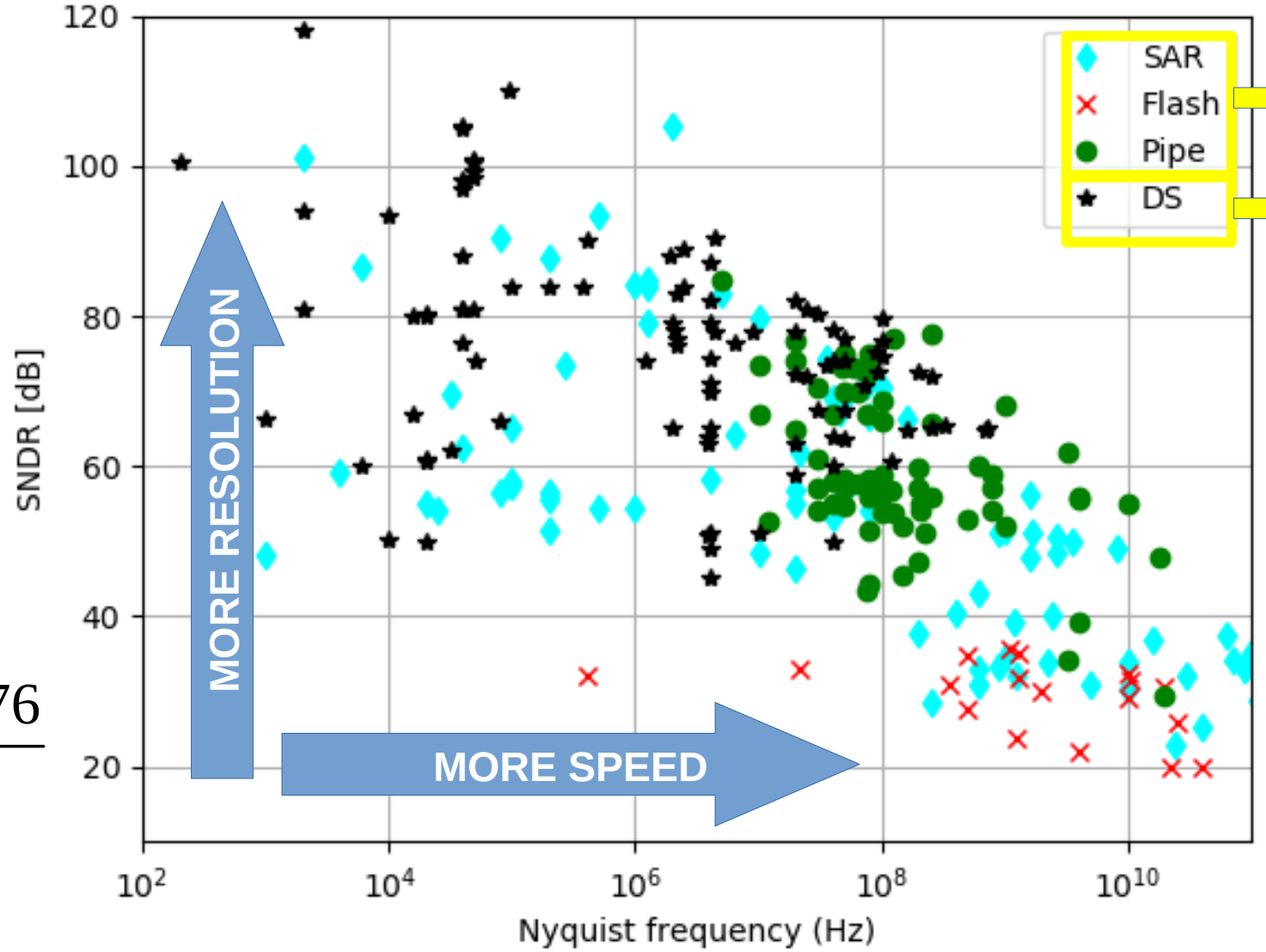
Counting and Integrating ADCs:
- Counting converters
- Dual-slope

2^N cycles of comparison
simple/accurate but slow

Binary-Search Algorithm based:
- Successive approximation converters (SAR)
- Cylic and Pipeline converters

N cycles of comparison
allows speed/resolution trade-off

State-of-the-art architectures versus resolution/speed trade off



Nyquist rate

Oversampled

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

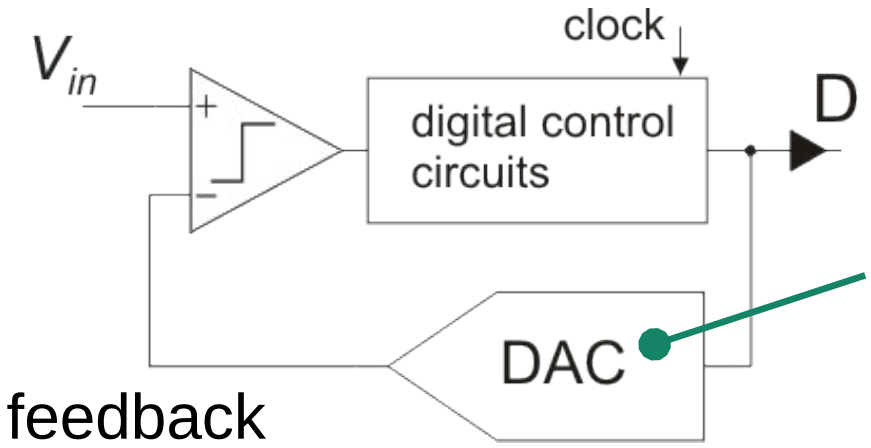
https://web.stanford.edu/~murmann/adcsurvey.html

Binary-Search based ADCs

For a N-bit ADC, the input signal (or part of it) is compared consecutively with N different levels:

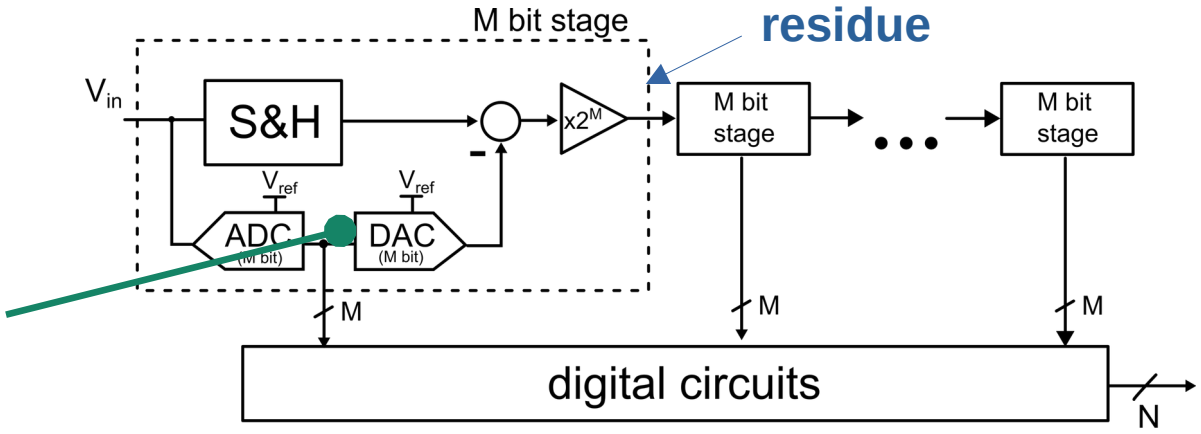
- **SAR ADC**: input voltage is compared with a feedback voltage, updated after each comparison cycle, the algorythm makes VDAC closer and closer to Vin after each comparison
- **Pipeline/cyclic ADC**: input voltage is compared with a coarse ADC, a matched DAC subtracts the result generating a **residue** which is the input of the next stage/cycle. (N cycles in case of cyclic, or N stage in the case of pipeline)

SAR ADC (digital control within the loop)



Typically, INL and DNL are mainly due to the DAC

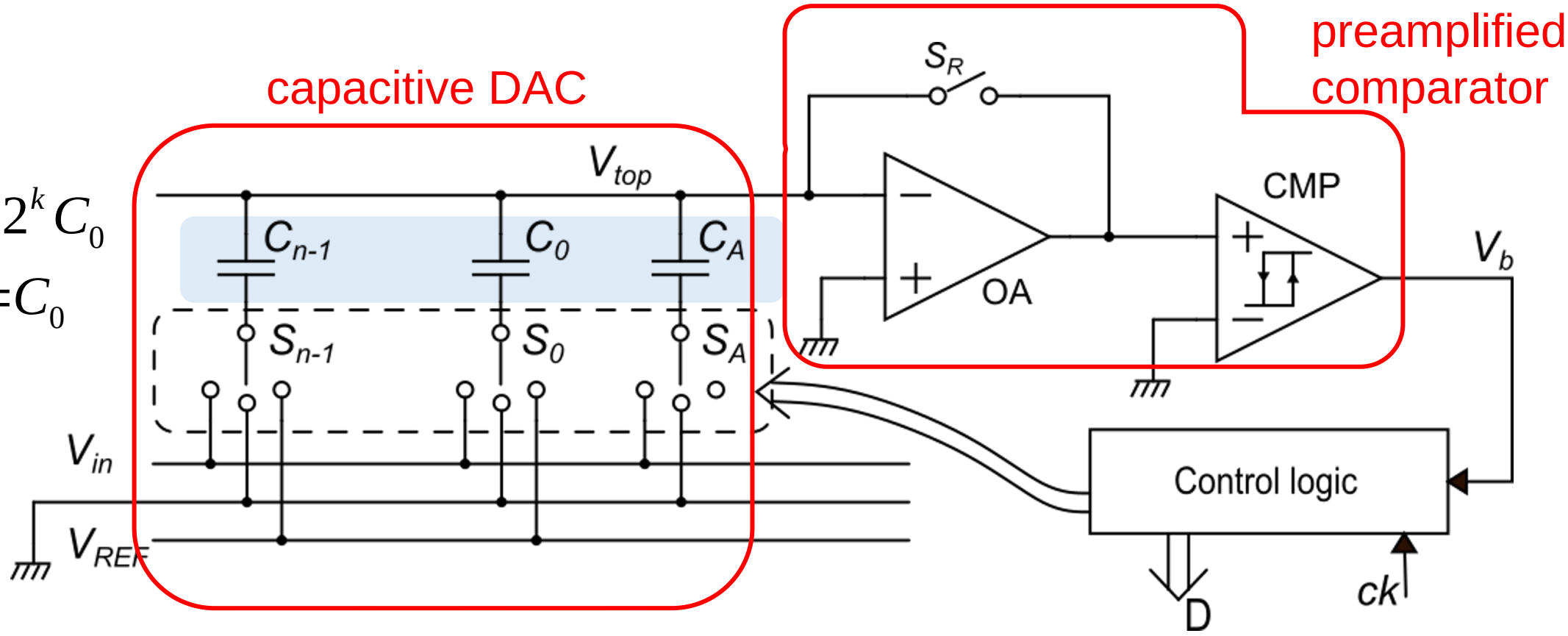
Pipeline ADC (digital outside the loop)



A very common SAR ADC: the charge-redistribution SAR with CDS

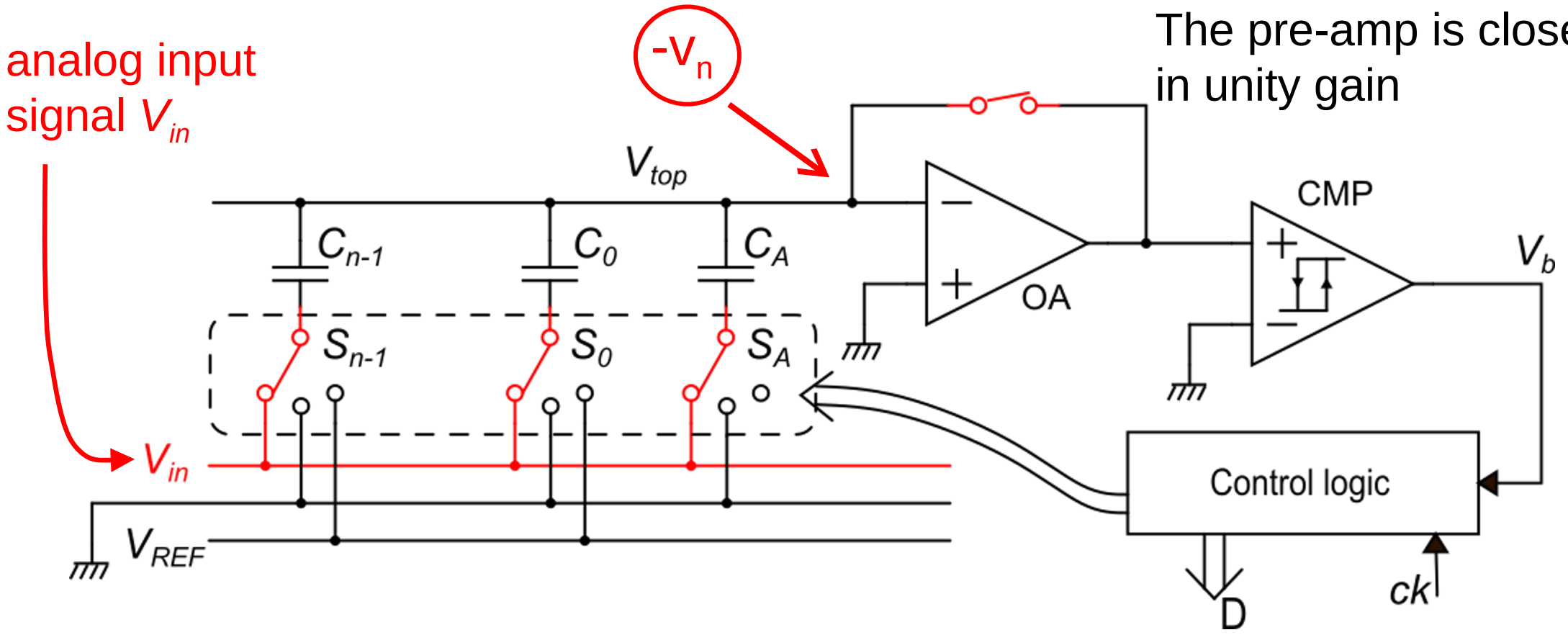
$$C_k = 2^k C_0$$

$$C_A = C_0$$



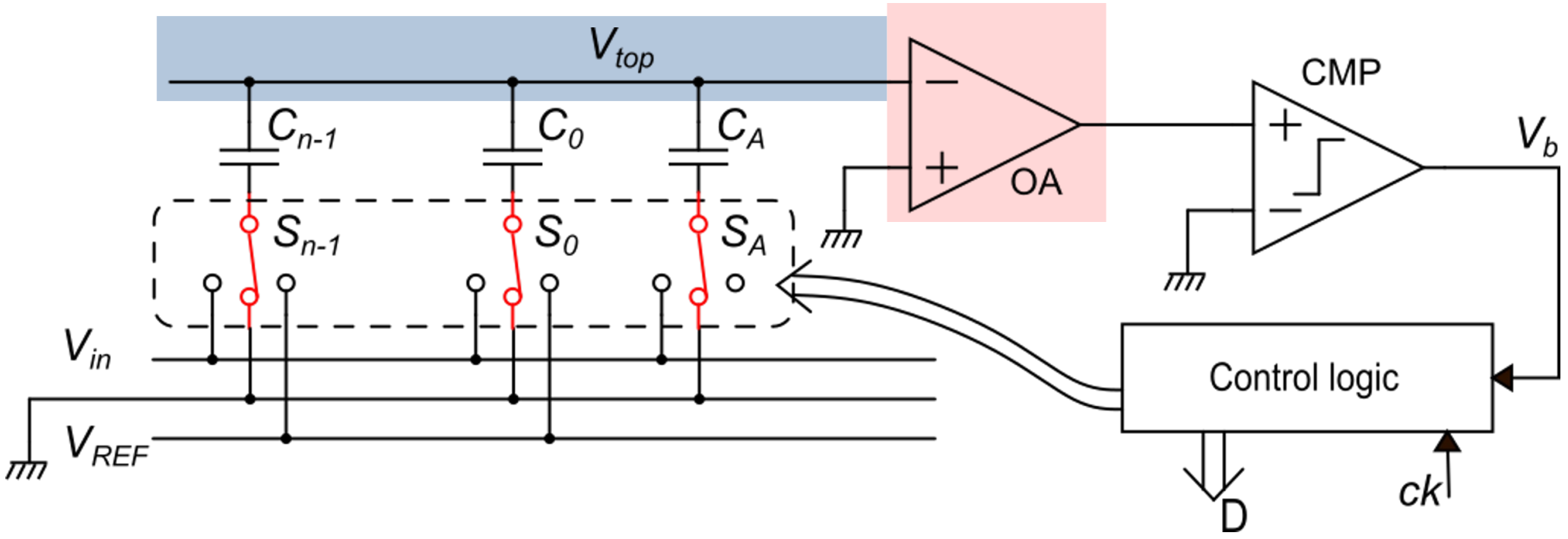
$$C_{tot} = C_A + \sum_{k=0}^{n-1} C_k = C_0 + C_0 \sum_{k=0}^{n-1} 2^k = C_0 + C_0 \left(2^n - 1\right) = 2^n C_0$$

Reset phase



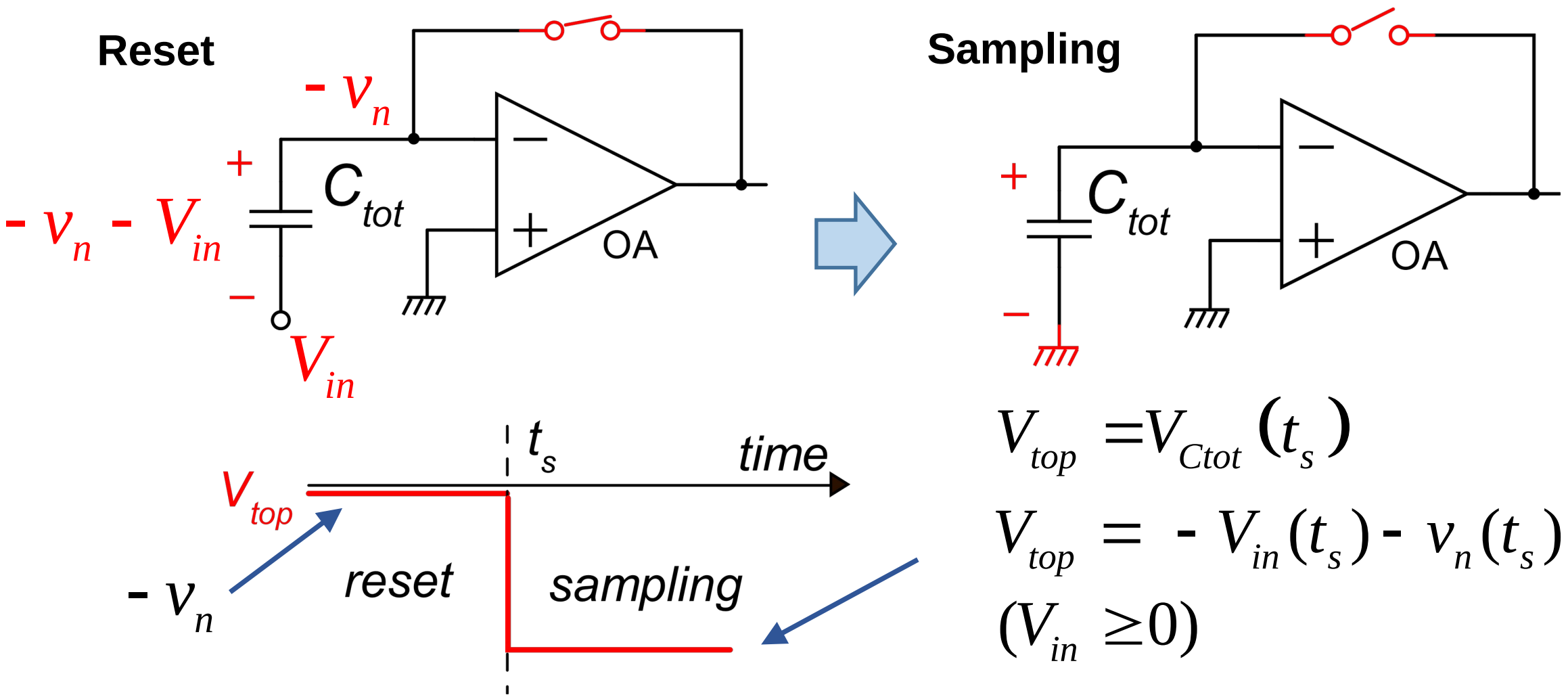
<u>All capacitors are in parallel,</u> with one terminal connected to the input voltage V_{in}.

Sampling phase



- The pre-amp is placed in **open loop configuration** and the bottom plates of all capacitors are connected to gnd.
- The voltage of the top plates (V_{top}) is **free to evolve** (it is floating, no current comes from the OA to V_{top})

Top voltage during the sampling phase



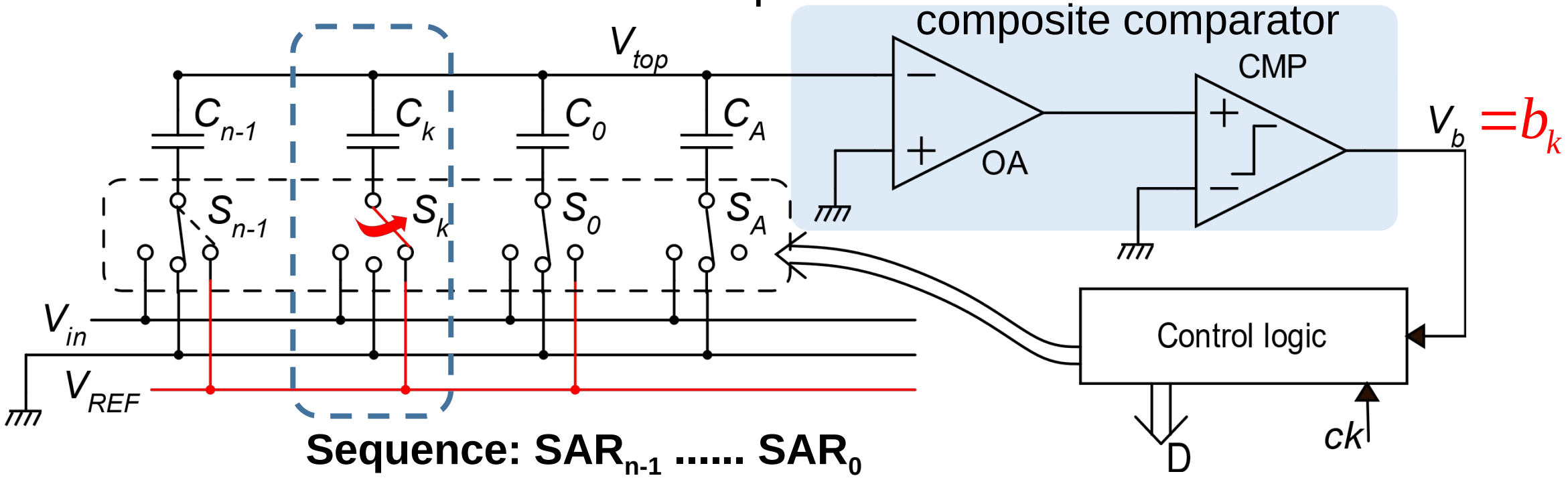
$$V_{top} = V_{Ctot}(t_s)$$

$$V_{top} = -V_{in}(t_s) - v_n(t_s)$$

$$(V_{in} \geq 0)$$

From now on, the SAR algorithm (phases) will try to succesively approach V_{top} to $-v_n$

SAR phases

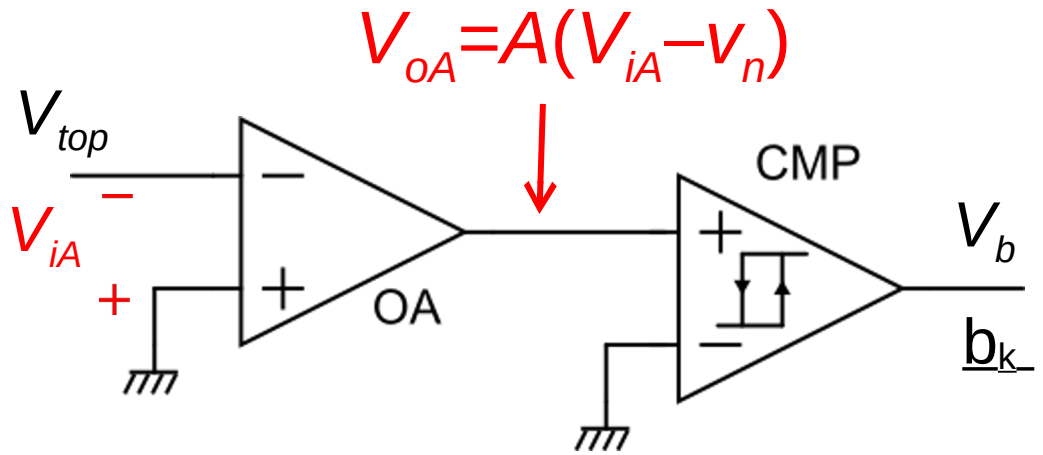


Sequence: SAR_{n-1} ..... SAR_0

Phase SAR_k

- Phase SAR_k begins by connecting the bottom plate of C_k to the reference voltage V_{REF} through switch S_k
- This causes a **positive jump** in voltage V_{top}.
- Bit k-th is the output of the composite comparator (V_b) at the end of phase SAR_k
- If b_k =0 S_k comes back to *gnd* (positive jump nulled), else it remains at V_{REF}

Composite comparator



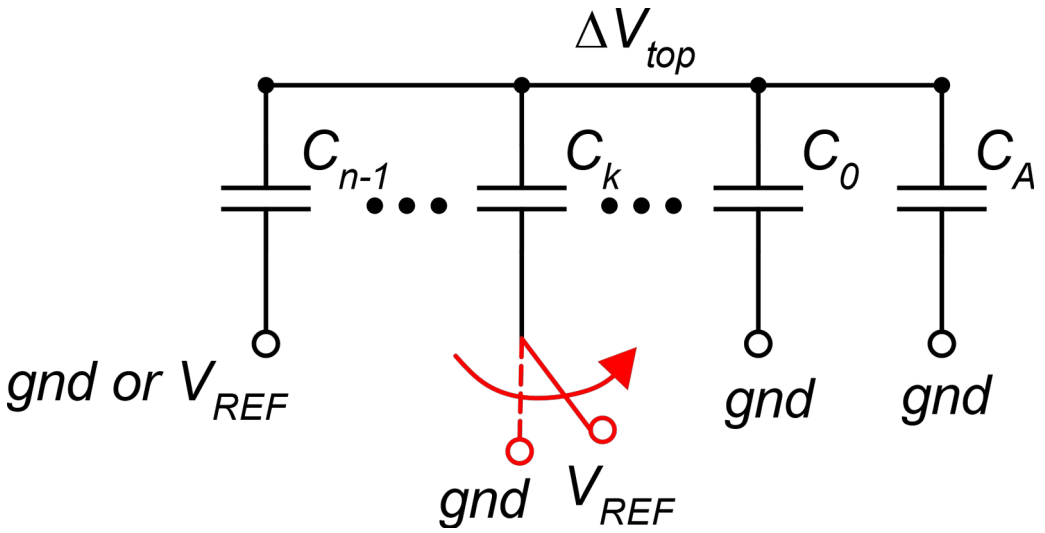
The gain of OA is so large that the offset and (eventual) hysteresis of CMP has negligible impact on the composite comparator characteristics.

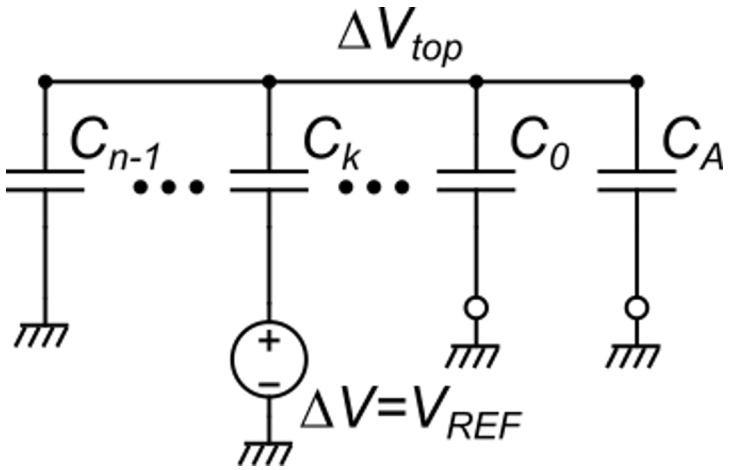
$$b_k = \begin{cases} \text{"1"} & \text{if: } V_{iA} > v_n \\ \text{"0"} & \text{if: } V_{iA} \le v_n \end{cases} \longrightarrow V_{iA} = - V_{top}$$

$$b_k = \begin{cases} \text{"1"} & \text{if: } -V_{top} > v_n \longrightarrow V_{top} < -v_n \\ \text{"0"} & \text{if: } -V_{top} \le v_n \longrightarrow V_{top} \ge -v_n \end{cases}$$

Hence, at each SAR phase, b_k is asserted if the positive jump does not cross the threshold ($-v_n$)

Phase **SAR$_k$**: calculation of the V_{top} jump





ΔV_{top} at phase SAR$_k$

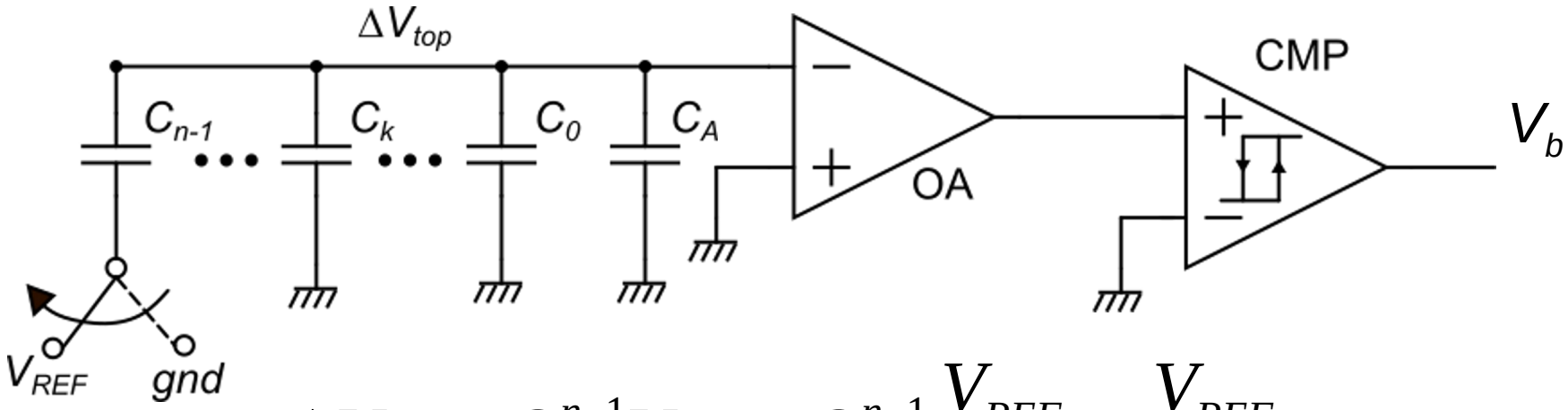
$$\Delta V_{top} = \Delta V_k = \Delta V \frac{C_k}{C_{tot}} = V_{REF} \frac{2^k C_0}{2^n C_0}$$

$$V_{LSB} = \frac{V_{REF}}{2^n} = \Delta$$

$$\Delta V_k = 2^k V_{LSB}$$

All-capacitor network: equivalent circuit for variations. Capacitors can be replaced by a resistors of value 1/C

Phase **SAR$_{n-1}$**



$$\Delta V_{n-1} = 2^{n-1} V_{LSB} = 2^{n-1} \frac{V_{REF}}{2^n} = \frac{V_{REF}}{2}$$

from sampling phase

$$V_{top} = \underbrace{-V_{in}(t_s) - v_n(t_s)} + \Delta V_{n-1} = -V_{in}(t_s) - v_n(t_s) + \frac{V_{REF}}{2}$$

Decision for bit b_{n-1} (taken at time t_{n-1} = end of phase SAR_{n-1}

$$V_b = 1 \text{ if } V_{top}(t_{n-1}) < -v_n(t_{n-1}) \Rightarrow -V_{in}(t_s) - v_n(t_s) + \frac{V_{REF}}{2} < -v_n(t_{n-1})$$

Phase SAR_{n-1}

$$b_{n-1}=1 \text{ if: } -V_{in}(t_s)-v_n(t_s)+\frac{V_{REF}}{2}<-v_n(t_{n-1})$$

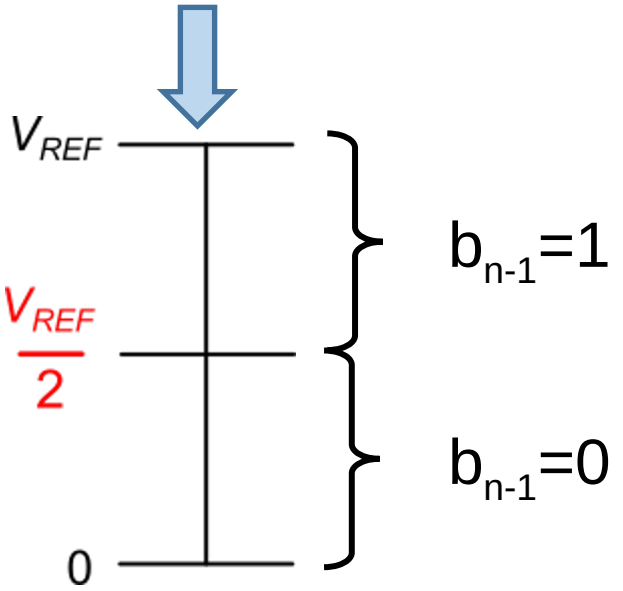
$$V_{in}(t_s)>\frac{V_{REF}}{2}-\underbrace{v_n(t_s)+v_n(t_{n-1})}$$

Subtraction of two noise samples taken at different times: constant and correlated components are rejected (CDS).

Neglecting noise / offset components, the condition becomes:

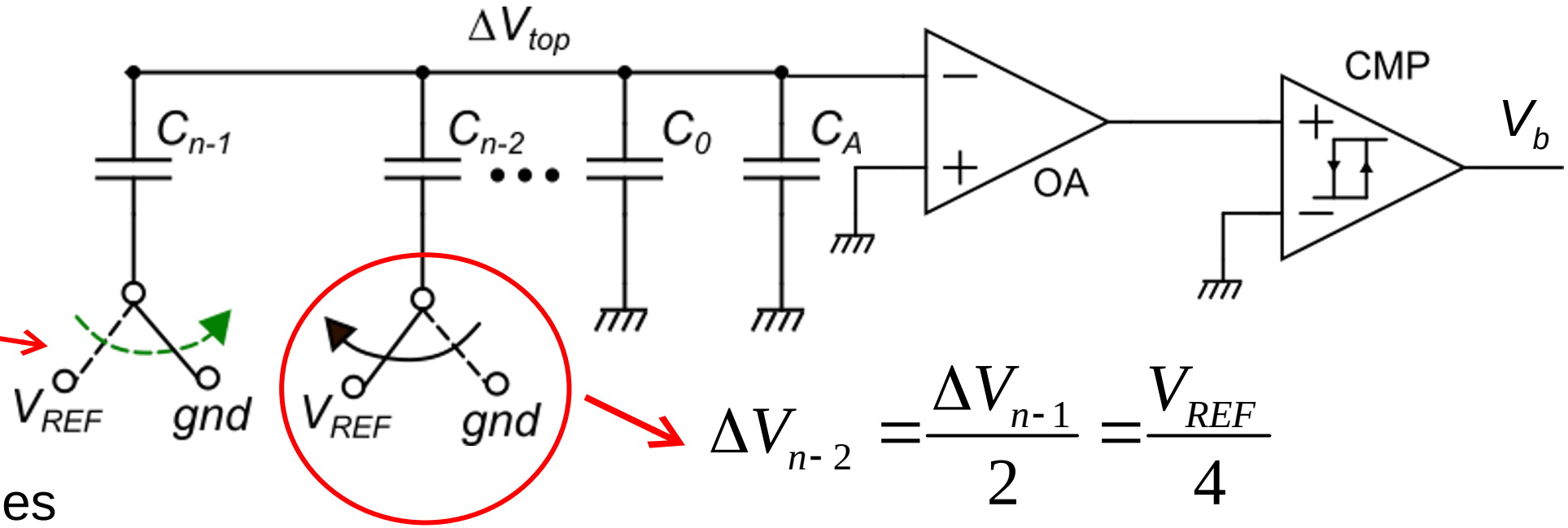
$$V_{in}(t_s)>\frac{V_{REF}}{2}$$

possible values of $V_{in}(t_s)$ and resulting value of b_{n-1}



This is in conformity with the successive approximation algorithm

Phase SAR$_{n-2}$



$$\Delta V_{n-2} = \frac{\Delta V_{n-1}}{2} = \frac{V_{REF}}{4}$$

Switch S_{n-1} goes back to *gnd* **if b_{n-1}=0**

Otherwise, it remains to V_{REF}

Decision : bit b_{n-2} =1 if:

$$V_{top} = -V_{in}(t_s) - v_n(t_s) + b_{n-1}\Delta V_{n-1} + \Delta V_{n-2} < -v_n(t_{n-2})$$

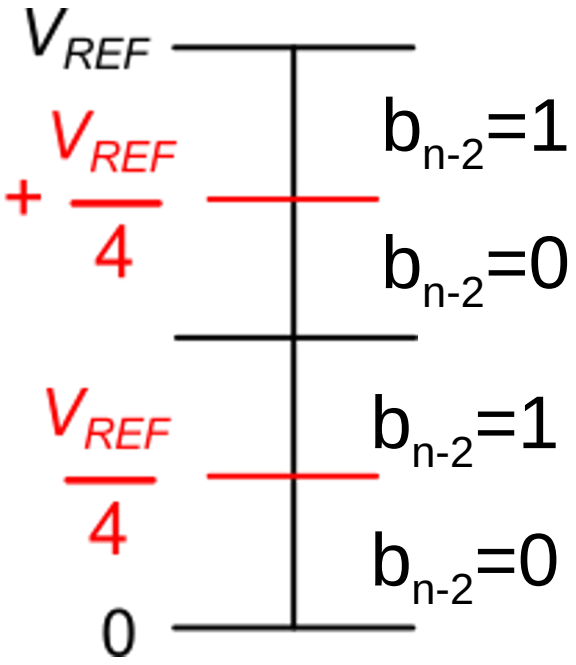
If S_{n-1} comes back to *gnd*, it subtracts ΔV_{n-1} from V_{top}

Decision for b_{n-2}

$$b_{n-2} = 1 \text{ if: } V_{in}(t_s) > \underbrace{b_{n-1}\Delta V_{n-1} + \Delta V_{n-2}}_{V_{tst}(n-2)}$$

if $b_{n-1}=1$ $V_{tst}(n-2) = \frac{V_{REF}}{2} + \frac{V_{REF}}{4}$

if $b_{n-1}=0$ $V_{tst}(n-2) = \frac{V_{REF}}{4}$



Generalization

At k-th step (phase SAR_k) , bit b_k is determined from the comparison of $V_{in}(t_s)$ with:

$$V_{tst}(k) = \underbrace{b_{n-1}\Delta V_{n-1} + b_{n-2}\Delta V_{n-2} + ... + b_{k+1}\Delta V_{k+1}} + \Delta V_k$$

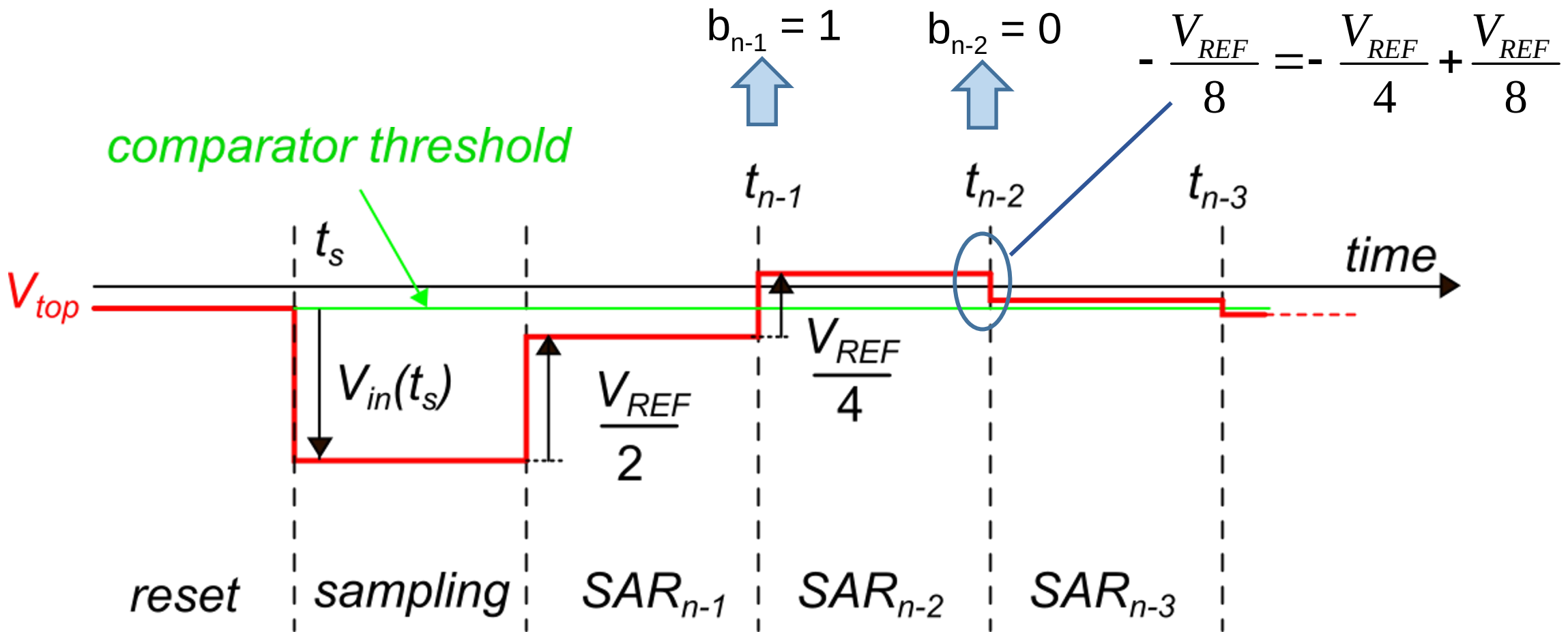
Increments applied in previous phases and maintained only if the corresponding bits are 1

At any step the increment is halved

$$\Delta V_k = \frac{\Delta V_{k+1}}{2}$$

At the last phase, SAR_0, the LSB (b_0) is determined and the conversion is complete. The bits determined in the successive phases are stored inside a register of the control logic and can be retrieved at the end of conversion.

Examples of conversion cycle



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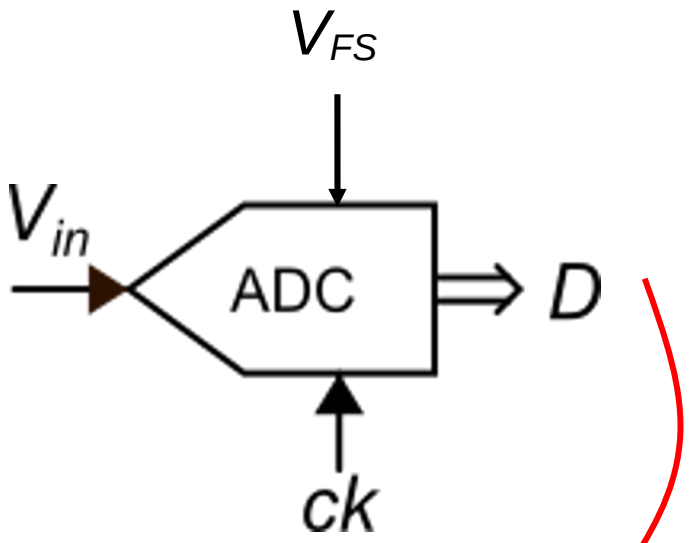
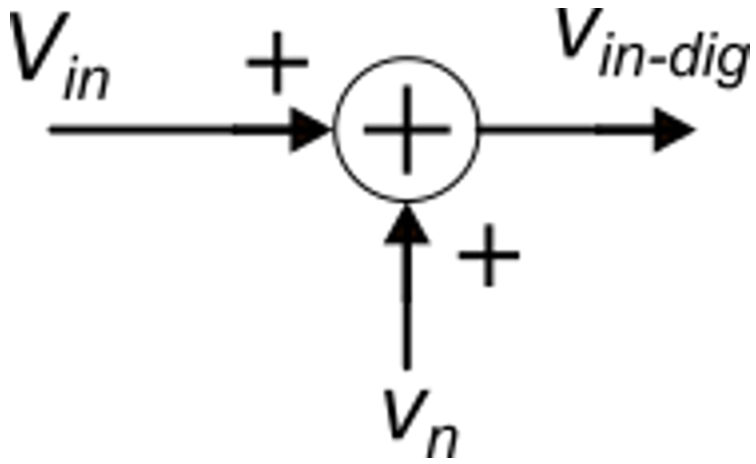
ADC linearized model



$$v_{in\text{-}dig} = V_{MIN} + \frac{V_{FS}}{2^n} D$$

Consequently, a **linearized model** of the ADC is:



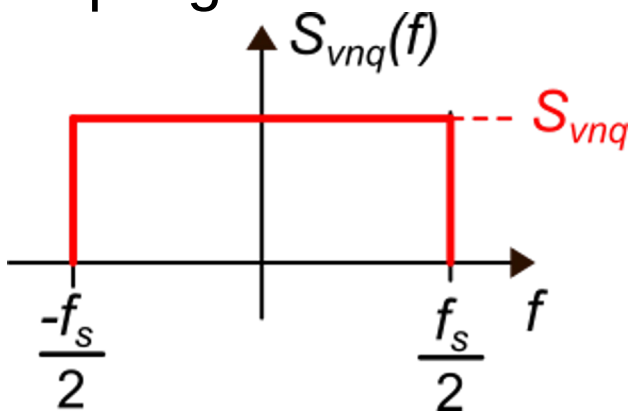
The converted value is affected by an error:

$$v_n = V_{in} - v_{in\text{-}dig}$$

This error accounts for all sources of non-ideality:
Quantization noise, physical noise and distortion

Uniform quantization noise PSD: properties

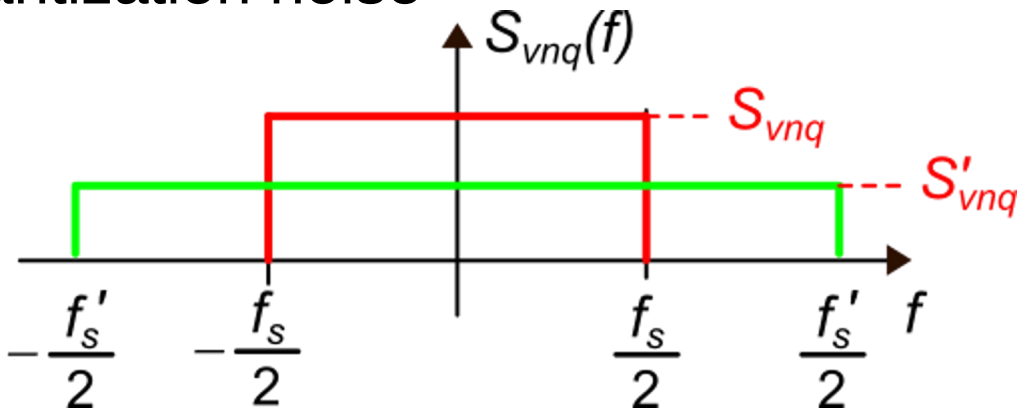
Effect of sampling:



Total v_{nq} power: $\left\langle v_{nq}^2 \right\rangle = \frac{\Delta^2}{12}$

$$S_{vnq} = \frac{\Delta^2}{12}\frac{1}{f_S}$$

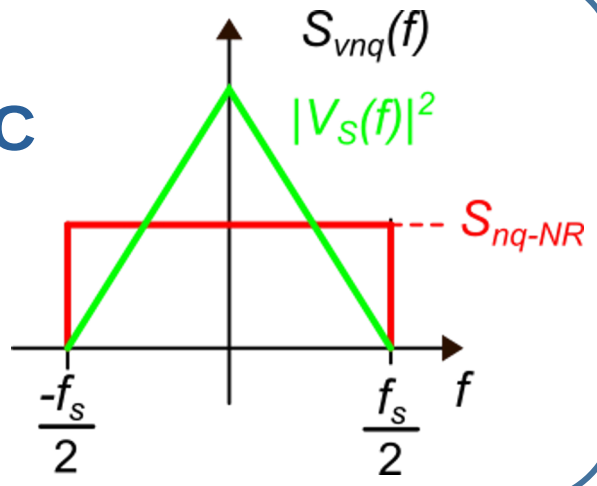
For the same ADC, increasing the sampling frequency reduces the PSD of the quantization noise



$$S'_{vnq} = \frac{\Delta^2}{12}\frac{1}{f_S'} = S_{vnq}\frac{f_s}{f_S'}$$

Oversampling ADCs

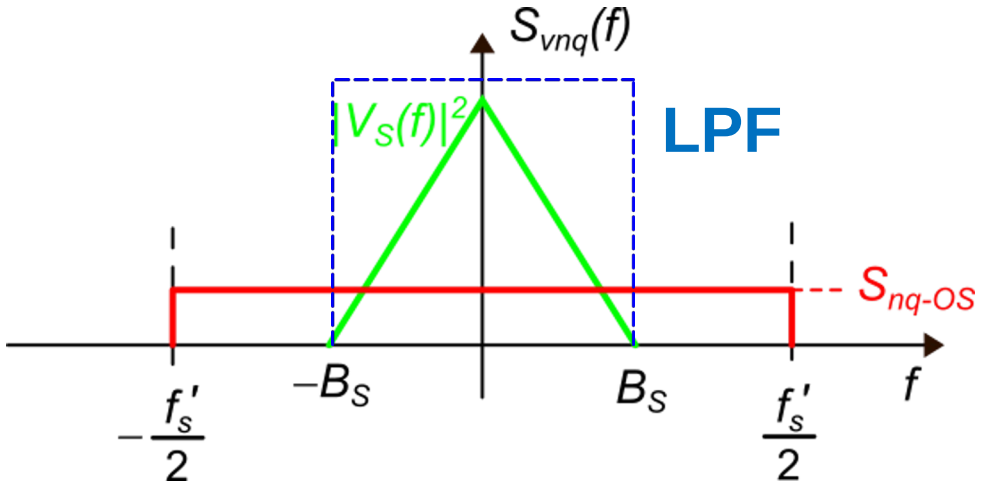
Nyquist rate ADC



$$\left\langle v^2_{nq\text{-}NR} \right\rangle = \frac{\Delta^2}{12} = f_S \cdot S_{nq\text{-}NR} = 2B_S \cdot S_{nq\text{-}NR}$$

B_S: signal bandwidth

$$f_S' = r_{OS} \cdot 2B_S \qquad r_{OS}\text{=Over-Sampling Ratio } (OSR)$$



Oversampling ADC

$$\left\langle v^2_{nq\text{-}OS} \right\rangle = 2B_S \cdot S_{nq\text{-}OS} \quad \text{(Ideal LPF)}$$

$$S_{nq\text{-}OS} = S_{nq\text{-}NR} \frac{2B_S}{f_S'} = \frac{S_{nq\text{-}NR}}{r_{OS}}$$

$$\left\langle v^2_{nq\text{-}OS} \right\rangle = \frac{2B_S \cdot S_{nq\text{-}NR}}{r_{OS}} = \frac{1}{r_{OS}} \left\langle v^2_{nq\text{-}NR} \right\rangle$$

Resolution increment in a pure oversampling ADC

$$SQNR = \frac{P_{MAX}}{\left\langle v_{nq}^2 \right\rangle} = \frac{3}{2} \cdot 2^{2n}$$

(The same can be applied considering broadband physical noise, bandwidth limited in +/- fs/2)

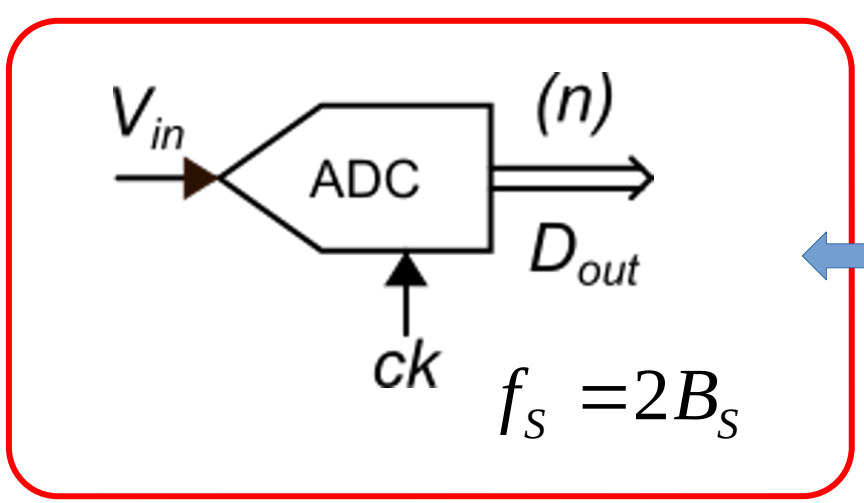
Considering two ADCs with same $\boldsymbol{V_{FS}}$

$\begin{cases} \text{ADC}_1\text{: SQNR}_1,\ n_1 \\ \text{ADC}_2\text{: SQNR}_2,\ n_2 \end{cases}$

$$\frac{SQNR_2}{SQNR_1} = 2^{2(n_2 - n_1)} = \frac{P_{MAX}}{\left\langle v_{nq2}^2 \right\rangle} \frac{\left\langle v_{nq1}^2 \right\rangle}{P_{MAX}} = \frac{\left\langle v_{nq1}^2 \right\rangle}{\left\langle v_{nq2}^2 \right\rangle}$$

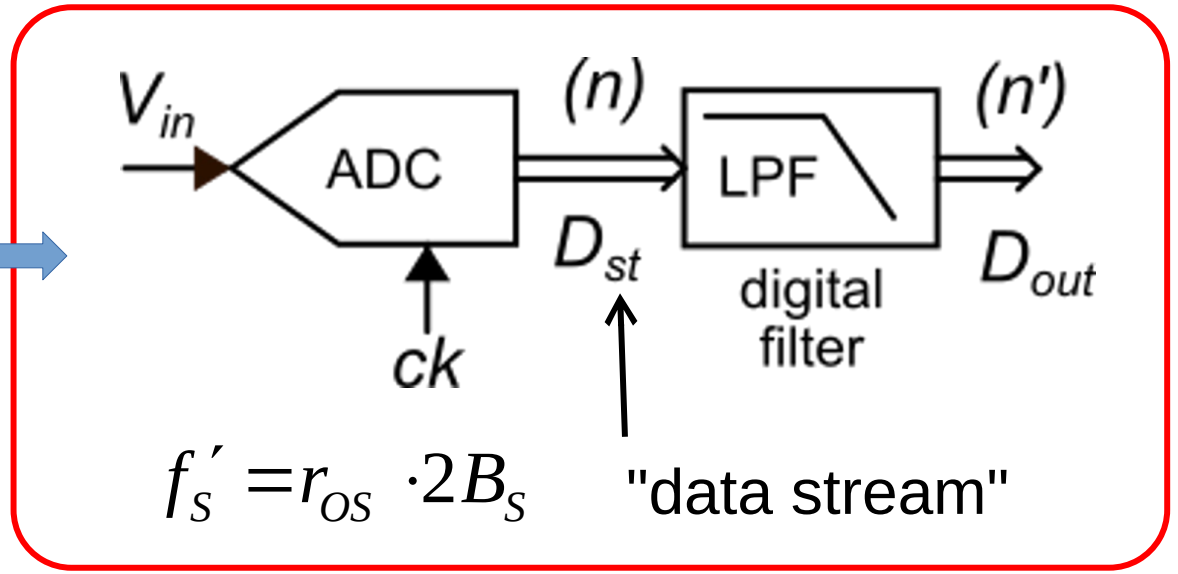
$$n_2 - n_1 = \frac{1}{2} \log_2 \left(\frac{\left\langle v_{n1}^2 \right\rangle}{\left\langle v_{n2}^2 \right\rangle} \right)$$

Resolution increment in a pure oversampling ADCc



ADC1, operated at Nyquist rate

Same core ADC



ADC2 = ADC1+LPF operated with oversampling

$$\left\langle v_{nq1}^2 \right\rangle = \left\langle v_{nq\text{-}NR}^2 \right\rangle$$

$$\left\langle v_{nq2}^2 \right\rangle = \left\langle v_{nq\text{-}OS}^2 \right\rangle = \frac{1}{r_{OS}} \left\langle v_{nq\text{-}NR}^2 \right\rangle$$

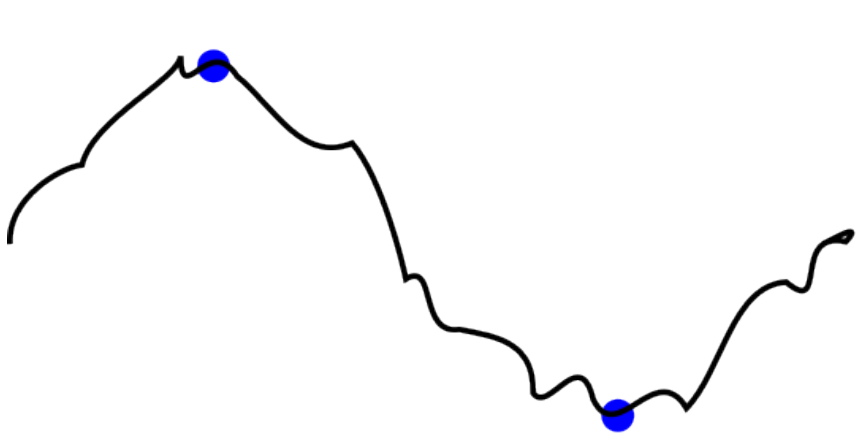
$$n_2 - n_1 = \frac{1}{2}\log_2\left(\frac{\left\langle v_{n1}^2 \right\rangle}{\left\langle v_{n2}^2 \right\rangle}\right) = \frac{1}{2}\log_2\left(\frac{\left\langle v_{nq\text{-}NR}^2 \right\rangle}{\left\langle v_{nq\text{-}OS}^2 \right\rangle}\right) = \frac{1}{2}\log_2\left(r_{OS}\right)$$

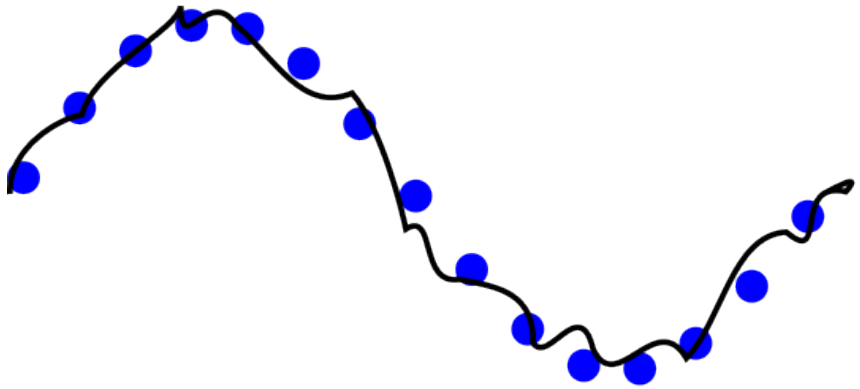
Resolution improvement

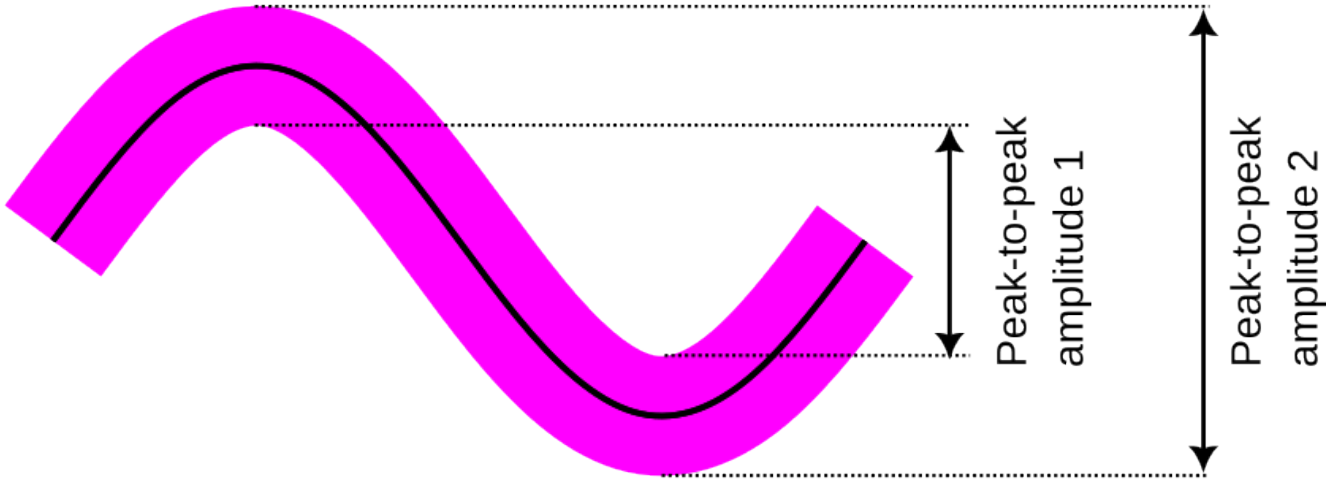
Resolution increment in a pure oversampling ADC

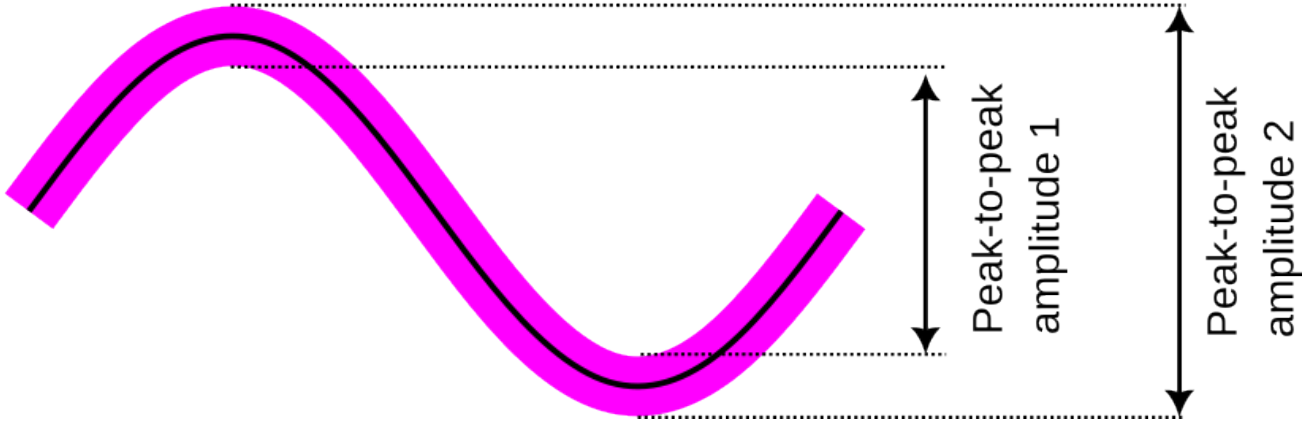
After filtering (reconstruction of the input tone)

Error on the reconstructed amplitude









Redundancy of information helps in reducing the uncertainty

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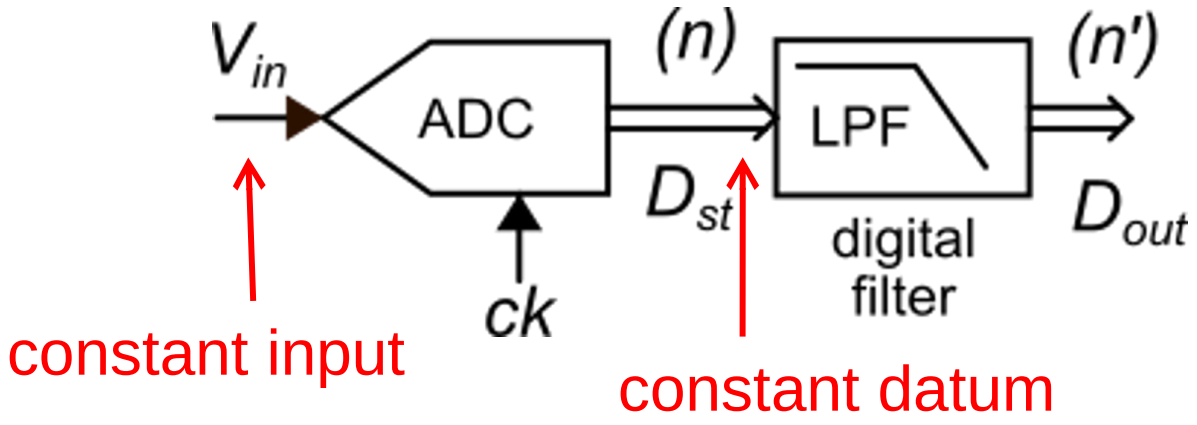
Pure oversampling ADCs: limits

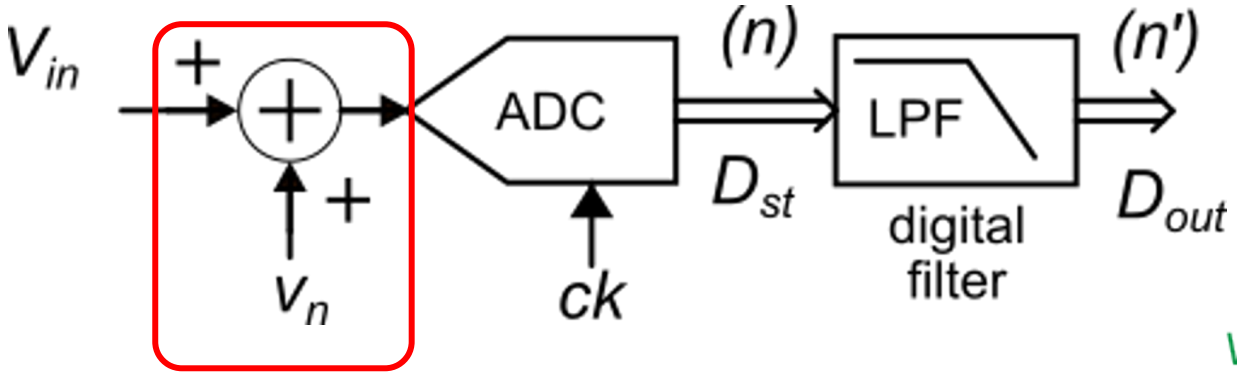
A minor limit:

The oversampling approach is based on the assumption that the quantization noise respects the uniform PSD model (quantizer input signal is "**busy**")

If the input signal is a **DC**, the quantization noise superimposed on the data stream will be constant and then will be unaffected by the LPF. A similar problem occurs with signals that are **slowly-varying** and/or have a **small magnitude** (below 1 LSB and with DC far from any decision level)

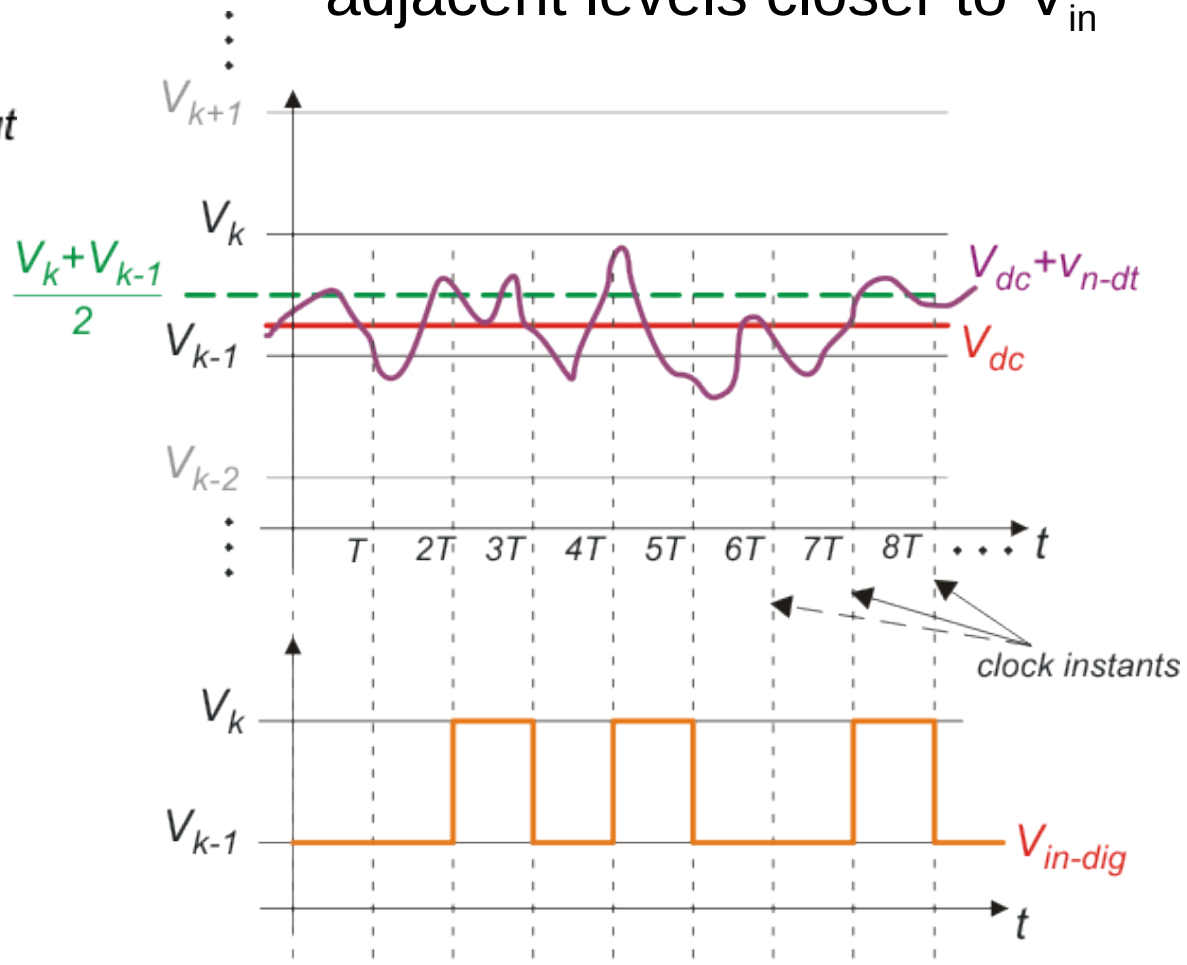


Increasing artificially the signal activity: the **dithering technique**



Dithering

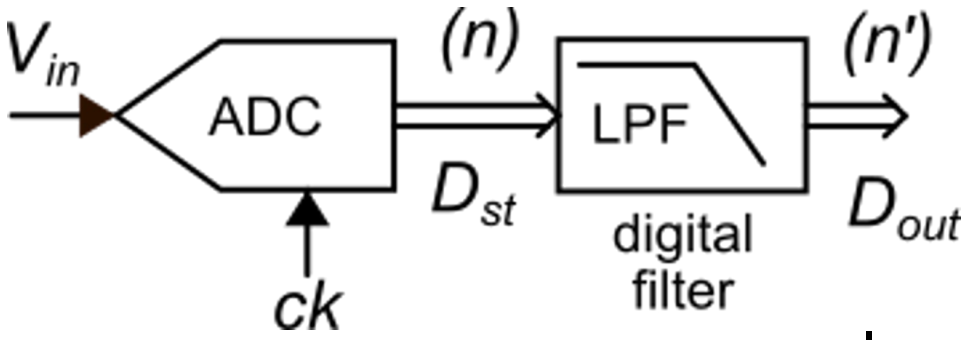
Noise makes the ADC switch across the two adjacent levels closer to V_{in}



Dithering consists in adding noise to the signal.

The added noise must have spectral components out of the signal band so that it is rejected by the LPF

The real limitation of the pure oversampling approach



$$n_{OS} - n_{NR} = \frac{1}{2}\log_2(r_{OS})$$

In order to obtain a resolution increment of a single bit, the sampling frequency must be **incremented by a factor of 4**

Example: oversamplig a 12-bit ADC to obtain 16 bits

$$n_{OS} - n_{NR} = 4 \ \text{(bits)} \Rightarrow r_{OS} = \frac{f_S}{2B_S} = 4^4 = 256$$

The pure oversampling approach is highly inefficient !

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The Delta-Sigma (Δ–Σ) ADC

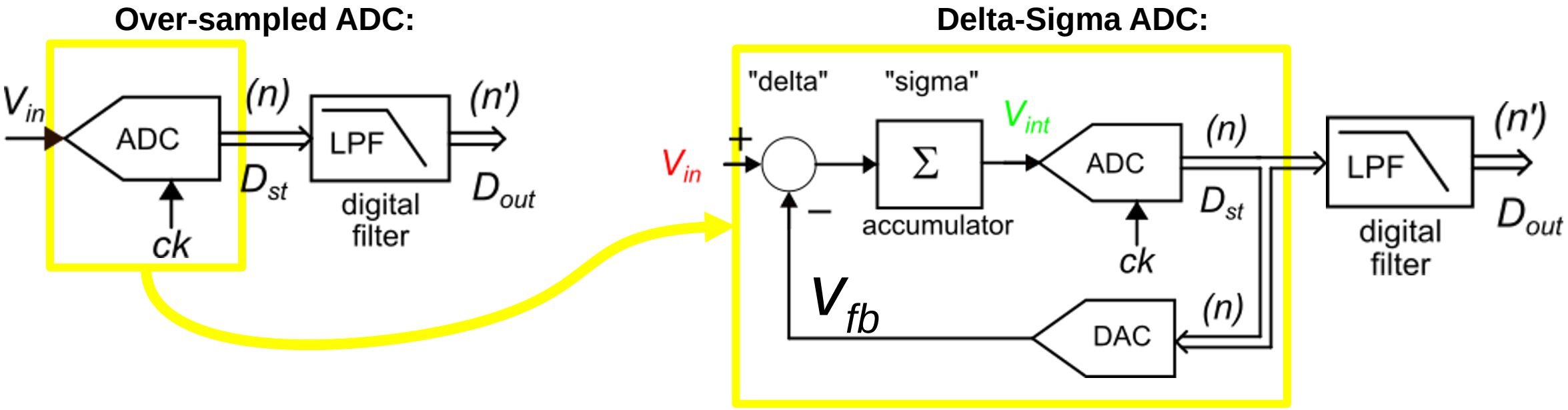
It was introduced in 1960
The term "Sigma-Delta (Σ–Δ)" ADC is simply synonym.

The Delta-Sigma converter combines two principles:

- **Oversampling**: $f_s >> 2B_s$
- **Noise shaping** (of quantization error)

The main target is to use more efficiently the oversampling in order to increase resolution with less oversampling ratio (r_{OS})

The Delta-Sigma (Δ–Σ) ADC

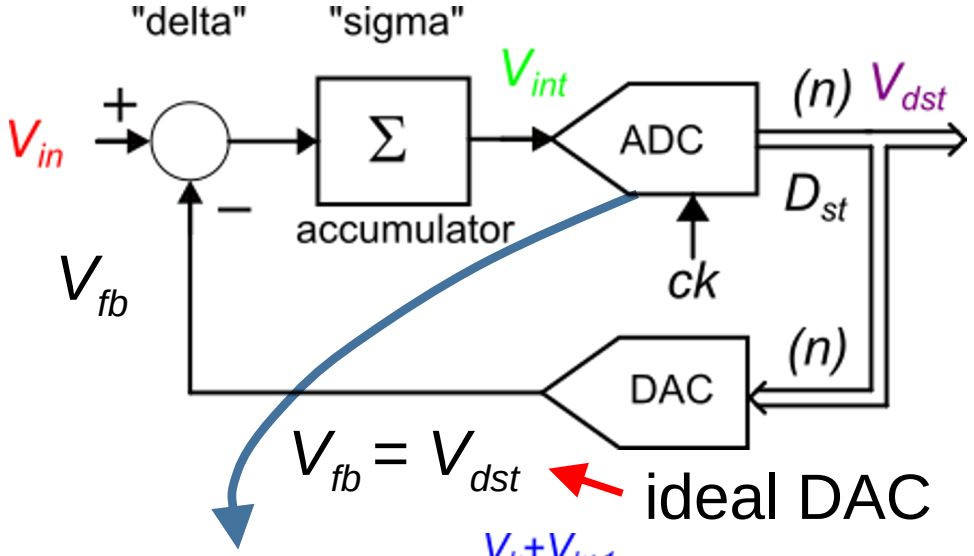


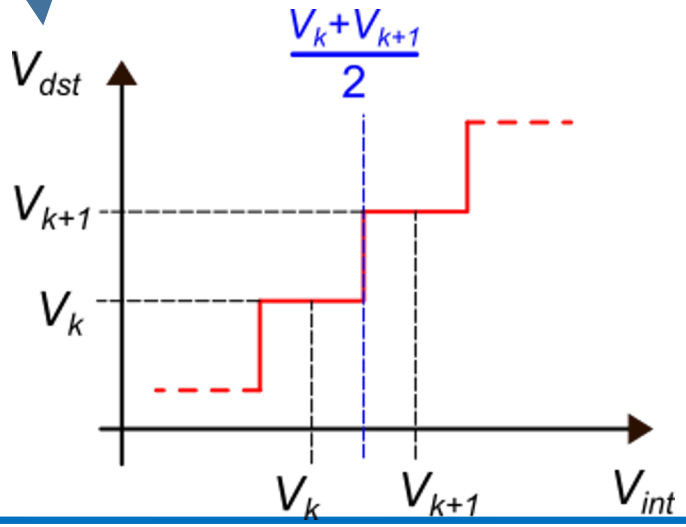
The ADC is substituted by a **Delta-Sigma modulator**:
The modulator is a fedback system composed by the following elements:

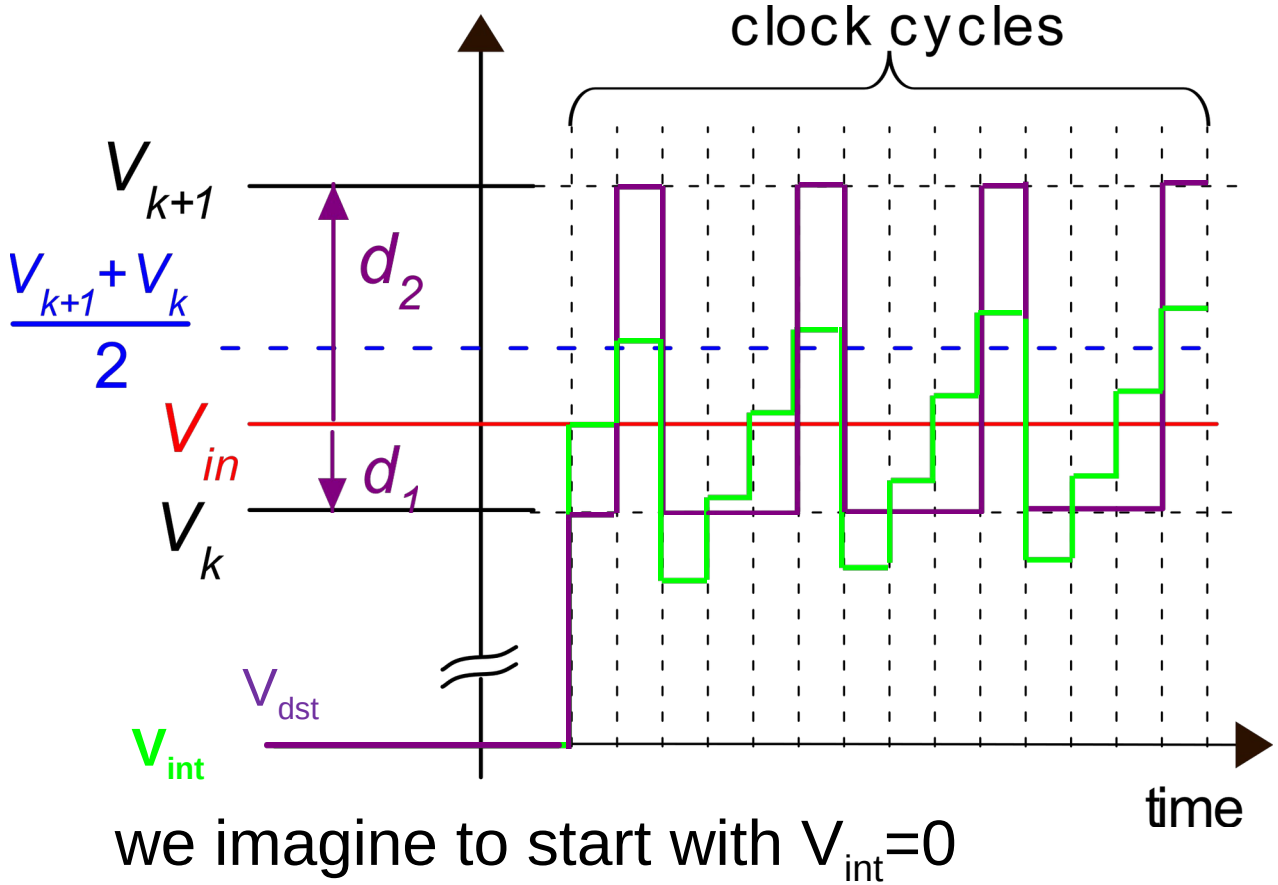
- A loop filter (accumulator in figure)
- A low-resolution ADC
- A low-resolution DAC

Delta-Sigma principle

The Delta-Sigma modulator (1st order)

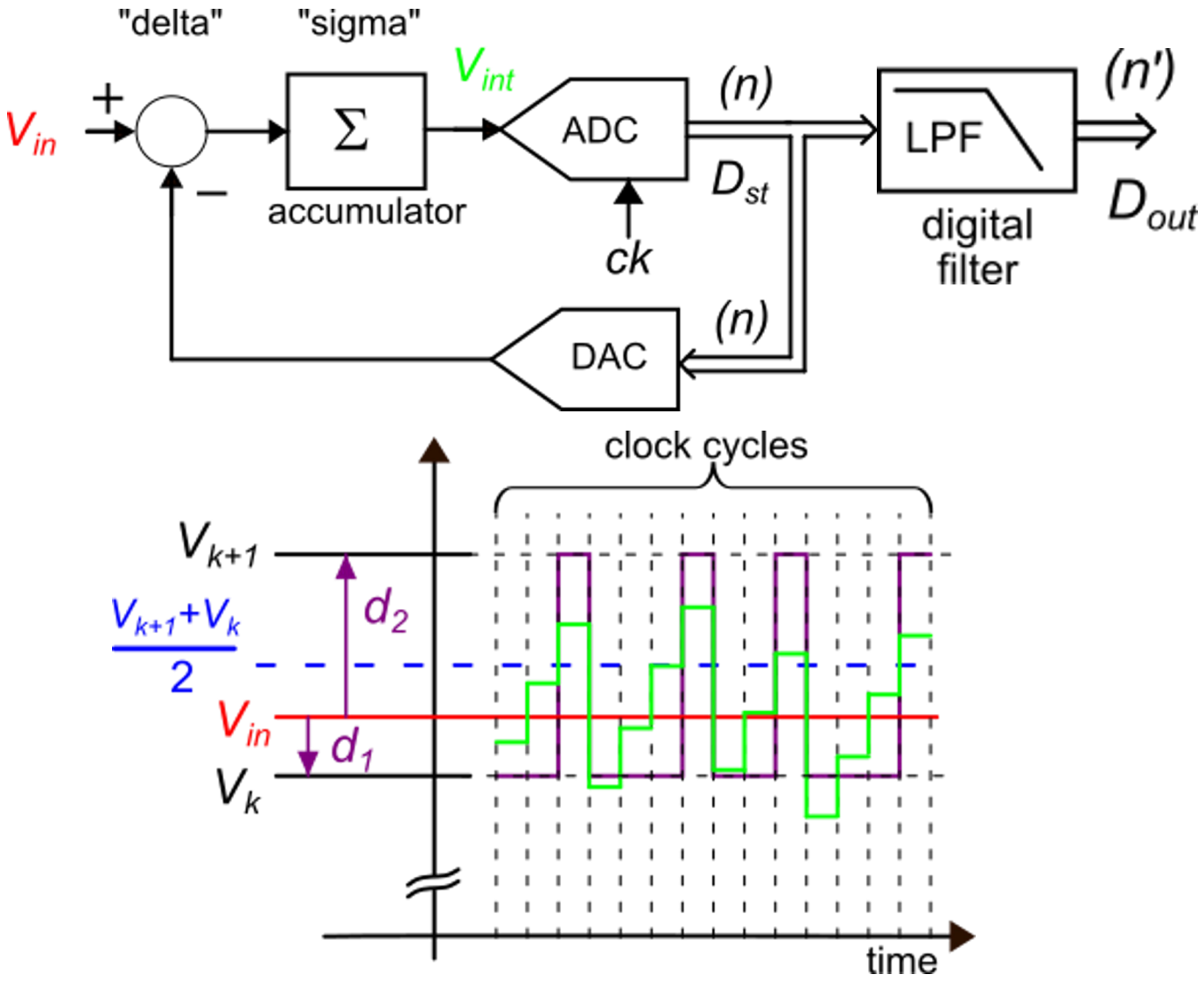






we imagine to start with $V_{int}=0$

Delta-Sigma principle

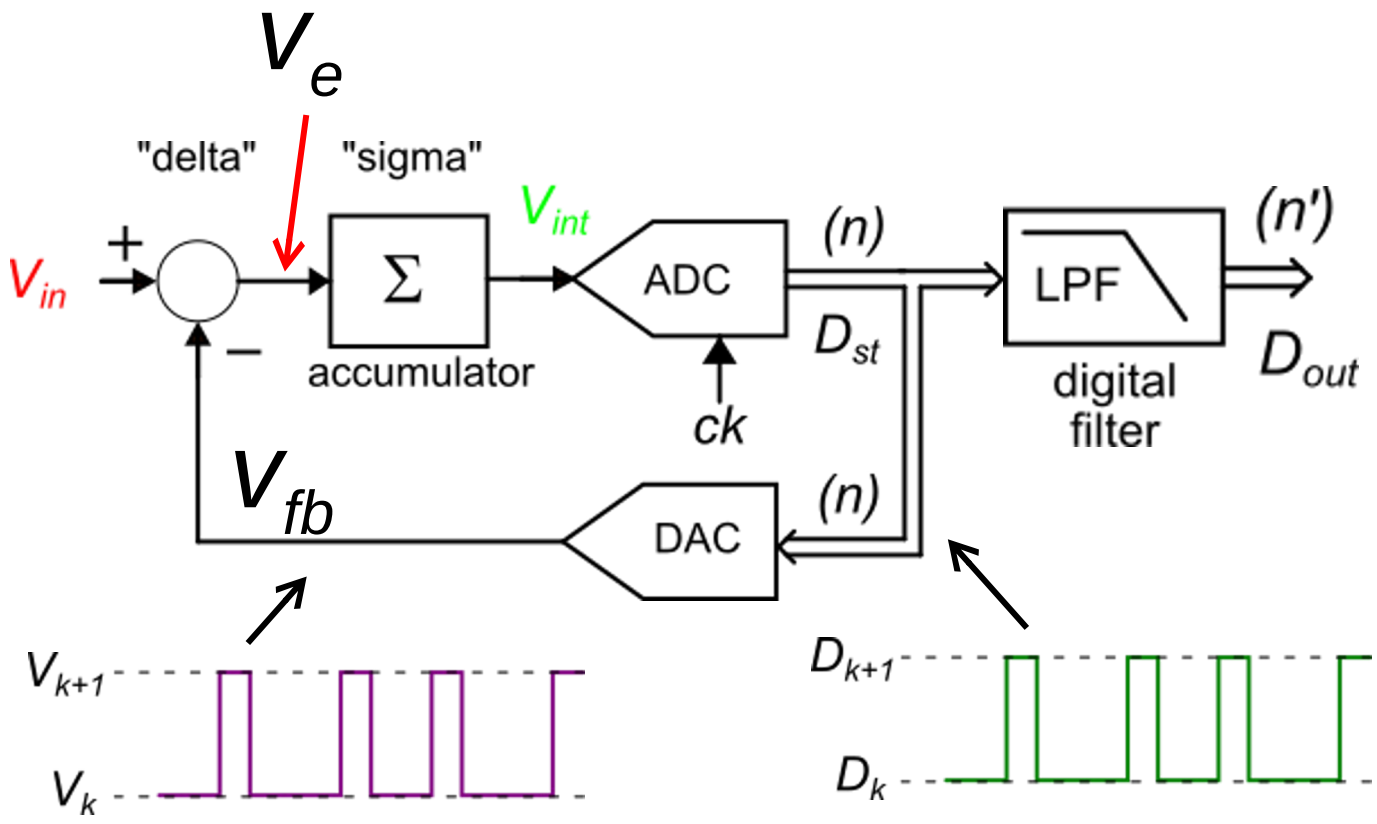


The digital filter averages the data stream that, in the example, contains only V_k and V_{k+1} levels.

The average will be a value between the two levels and will be closer to V_{in} than both V_k and V_{k+1}

In this example, value V_k appears more frequently than V_{k+1}. Then the average will be closer to V_k, as actually V_{in} is.

Delta-Sigma principle



The average of V_e, performed over a very long time, must be zero, otherwise the output of the accumulator would diverge.

$$\langle V_e \rangle = \langle V_{in} - V_{fb} \rangle = 0$$

$$\langle V_{fb} \rangle = \langle V_{in} \rangle$$

If the LPF filter has a bandwidth small enough, it can extract the average of the data stream D_k with arbitrary accuracy. If the DAC is ideal (no distortion), then the average of D_k gives V_{in} with an arbitrary resolution.

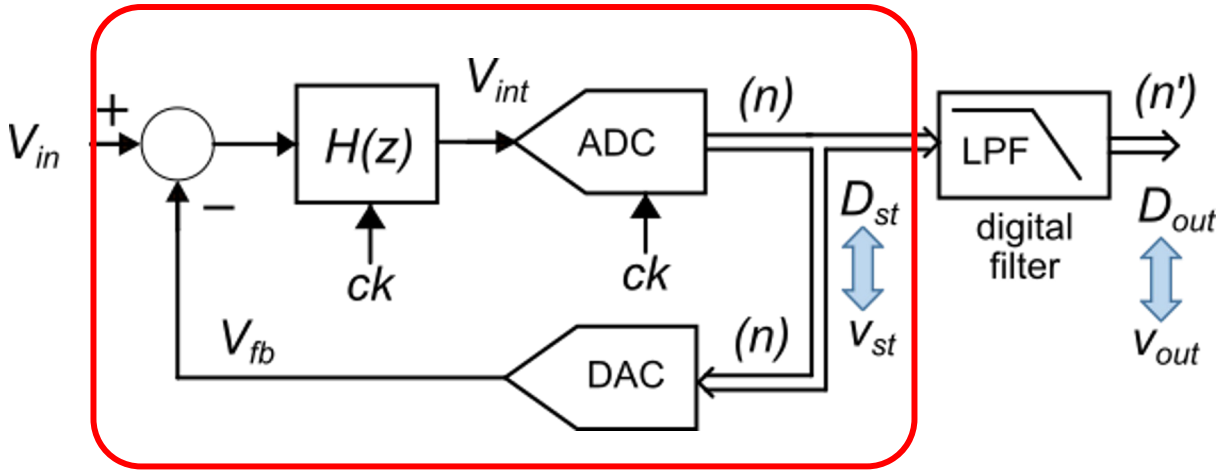
Delta-Sigma principle

What we have seen so far suggests that the delta-sigma modulator can produce an output data stream that, once properly filtered, can yield V_{in} with a higher resolution than the original ADC.

Differently from the pure oversampling ADC, the delta-sigma is capable of producing the alternation of two adjacent codes ($V_{k,}$ V_{k+1}) even with a DC signal without dithering. In the case of an input DC signal, the constant error v_n is modulated (this is the origin of the name) and can be filtered out.

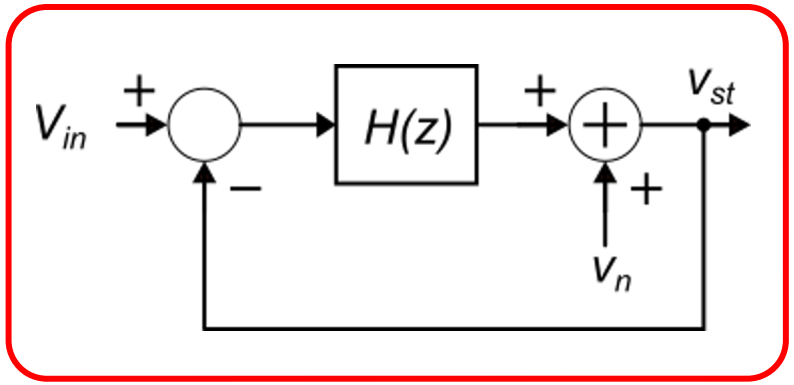
As in the oversampling approach, it is necessary to filter the output data stream, reducing the bandwidth to the minimum required by the signal spectrum. We will show that high resolution increments can be obtained with moderate oversampling ratios.

Analysis of a first order delta-sigma modulator



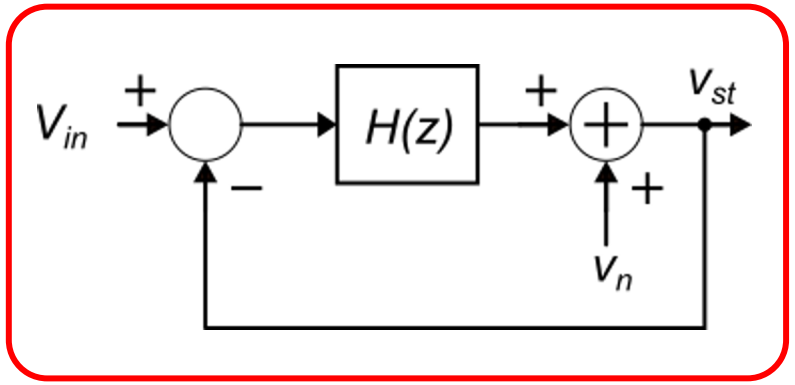
Δ–Σ modulator

H(*z*) is a discrete time transfer function, properly represented with its *z*-transform.



Linearized model of the modulator. The DAC is considered ideal; thus, it simply translates the voltage representation of D_{st} (v_{st}) in an exactly corresponding analog voltage (v_{fb}=v_{st})

Analysis of a first order delta-sigma modulator



$$v_{st} = (v_{in} - v_{st})H(z) + v_n$$

$$v_{st}\left[1 + H(z)\right] = v_{in}H(z) + v_n$$

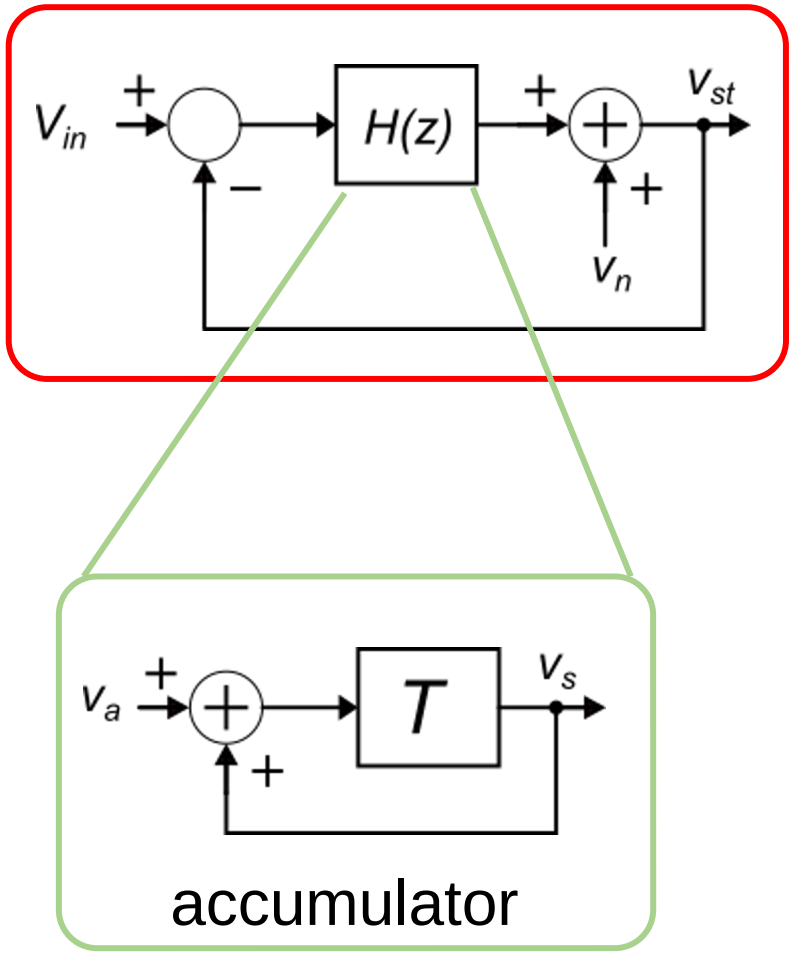
$$v_{st} = v_{in}\frac{H(z)}{1 + H(z)} + v_n\frac{1}{1 + H(z)}$$

$$v_{st} = v_{in} \cdot STF(z) + v_n \cdot NTF(z)$$

$$STF(z) = \text{Signal Transfer Function} = \frac{H(z)}{1 + H(z)}$$

$$NTF(z) = \text{Noise Transfer Function} = \frac{1}{1 + H(z)}$$

Analysis of a first order delta-sigma modulator



$$v_{st} = v_{in} \cdot STF(z) + v_n \cdot NTF(z)$$

$$STF(z) = \frac{H(z)}{1 + H(z)} \qquad NTF(z) = \frac{1}{1 + H(z)}$$

$$v_s(nT) = v_a(nT - T) + v_s(nT - T)$$

$$v_s(z) = v_a(z)z^{-1} + v_s(z)z^{-1}$$

$$v_s(z) = v_a(z)\frac{z^{-1}}{1 - z^{-1}}$$

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

Analysis of a first order delta-sigma modulator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

$$STF(z) = \frac{H(z)}{1 + H(z)} = \frac{\dfrac{z^{-1}}{1 - z^{-1}}}{1 + \dfrac{z^{-1}}{1 - z^{-1}}} = \frac{\dfrac{z^{-1}}{1 - z^{-1}}}{\dfrac{1}{1 - z^{-1}}} = z^{-1}$$

A simple delay of one clock cycle

$$NTF(z) = \frac{1}{1 + H(z)} = \frac{1}{1 + \dfrac{z^{-1}}{1 - z^{-1}}} = \frac{1}{\dfrac{1}{1 - z^{-1}}} = 1 - z^{-1}$$

This is the equivalent of the derivative in the DT domain

NTF in the frequency domain

$$STF(z) = z^{-1}$$

$$NTF(z) = 1 - z^{-1} \qquad z \Leftarrow e^{j\omega T} \qquad \text{where: } T = \frac{1}{f_s}$$

$$NTF(j\omega) = 1 - e^{-j\omega T} = e^{-\frac{j\omega T}{2}} \left(e^{\frac{j\omega T}{2}} - e^{-\frac{j\omega T}{2}} \right)$$

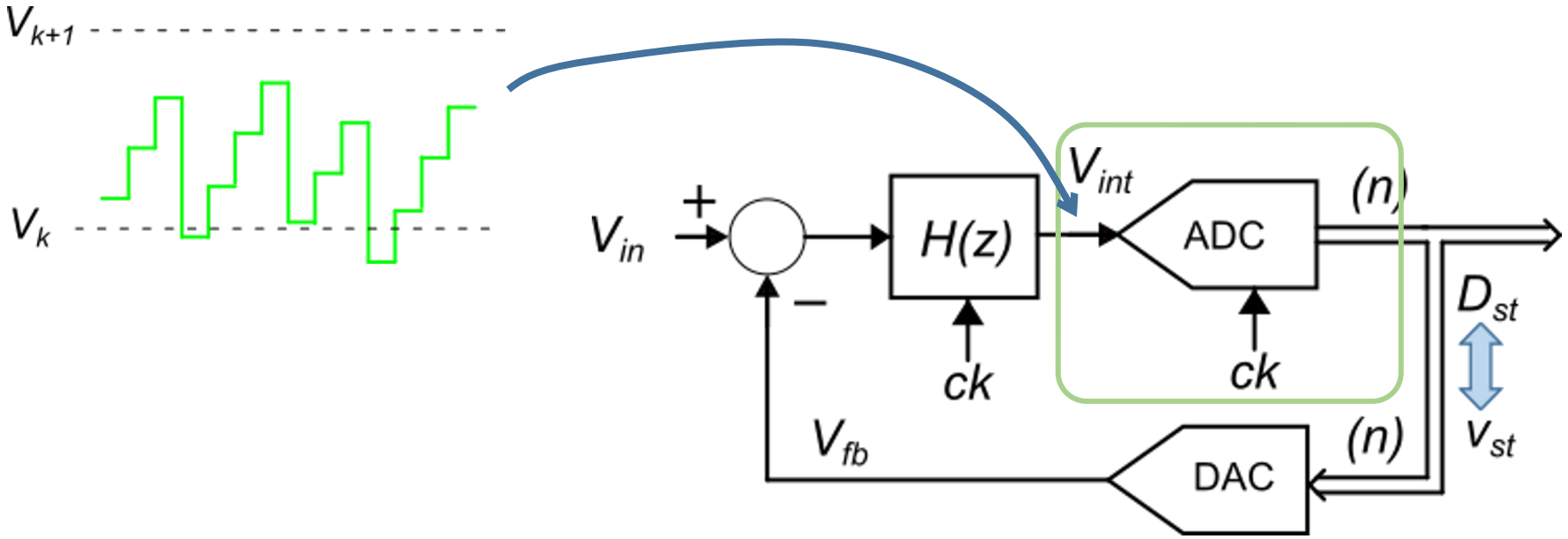
$$NTF(j\omega) = e^{-\frac{j\omega T}{2}} \cdot 2j \sin\left(\frac{\omega T}{2} \right) \qquad \omega = 2\pi f$$

$$NTF(j\omega) = e^{-j\pi fT} \cdot 2j \sin(\pi fT)$$

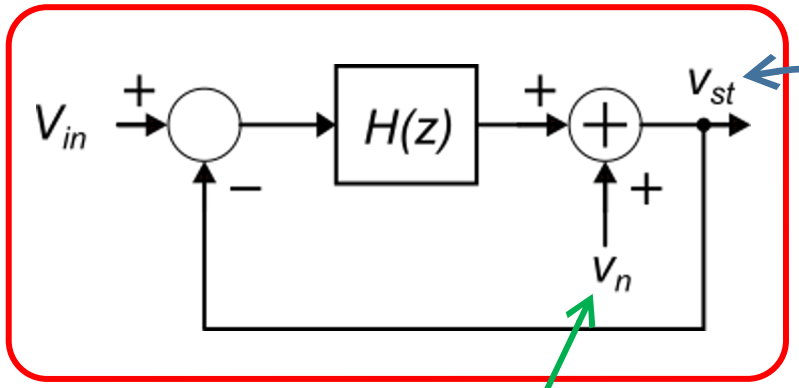
Output spectral density of the quantization noise

The uniform PSD model of the quantization noise is acceptable because the modulator continuously changes the input of the original ADC, sweeping across the whole range [-Δ/2, +Δ/2] of the quantization noise.

For more accurate analysis of second order effects, the limits of the uniform PSD model should be taken into account.



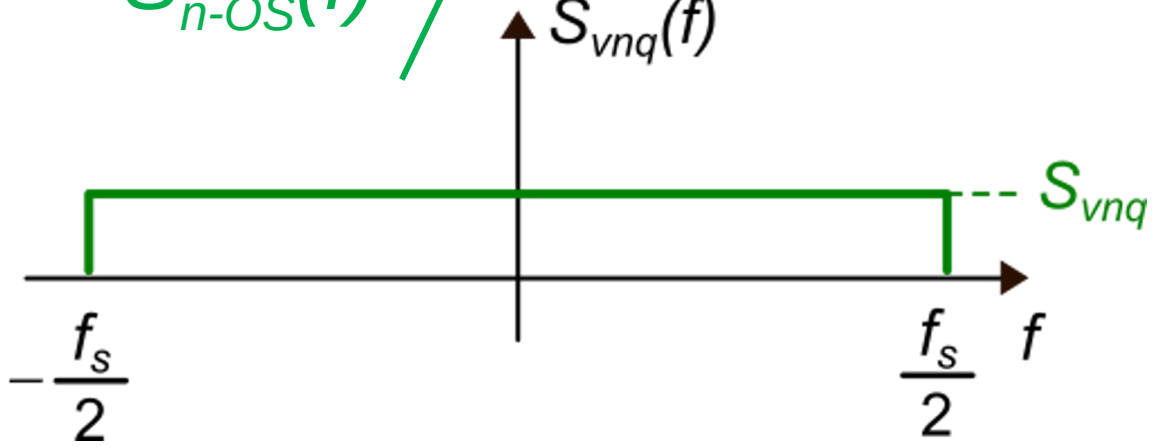
Quantization noise PSD at the output of the Δ–Σ modulator



$$NTF(j\omega) = e^{-j\pi fT} \cdot 2j\sin(\pi fT)$$

$$S_{n\text{-}DS}(f) = S_{n\text{-}OS}\left|NTF(f)\right|^2$$

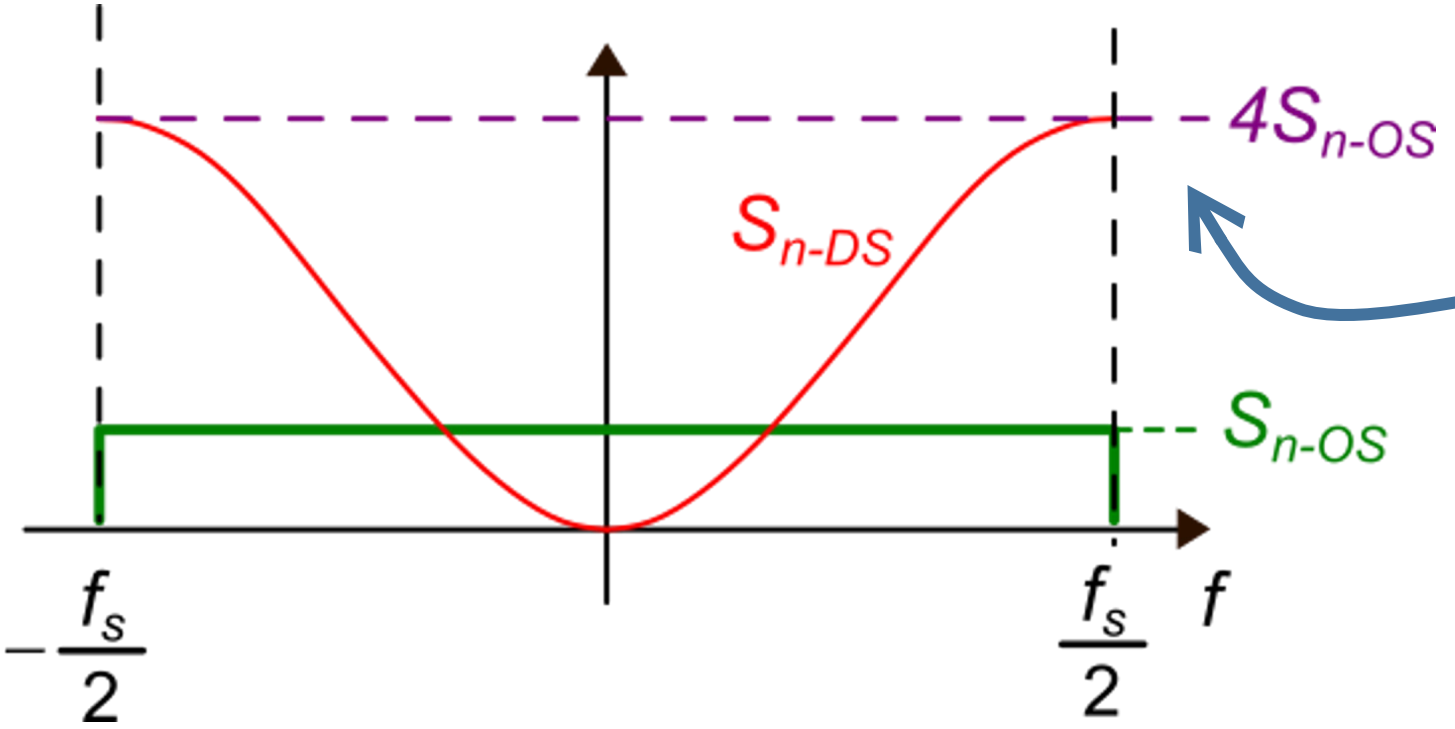
$S_{n\text{-}OS}(f)$



$$S_{n\text{-}DS}(f) = S_{n\text{-}OS} \cdot 4\sin^2\left(\pi\frac{f}{f_S}\right)$$

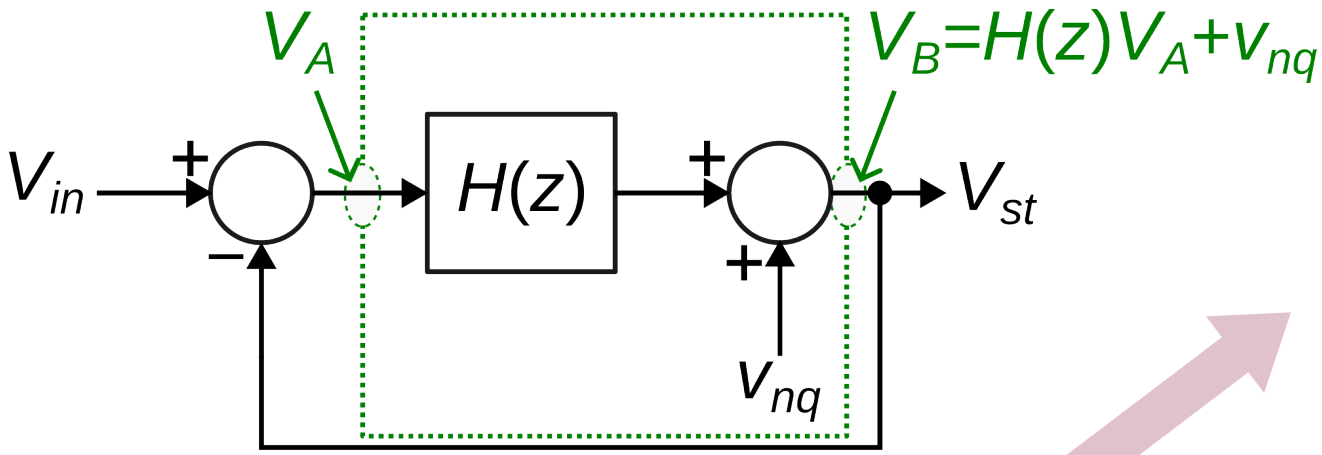
Quantization noise PSD at the output of the Δ–Σ modulator

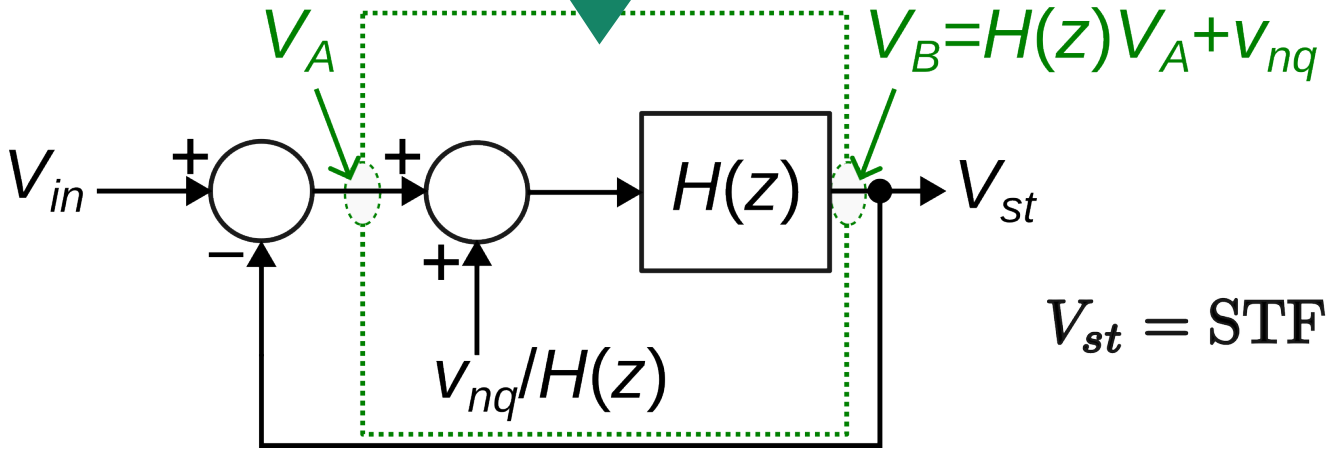
$$S_{n\text{-}DS}(f) = S_{n\text{-}OS} \cdot 4\sin^2\left(\pi \frac{f}{f_S}\right)$$

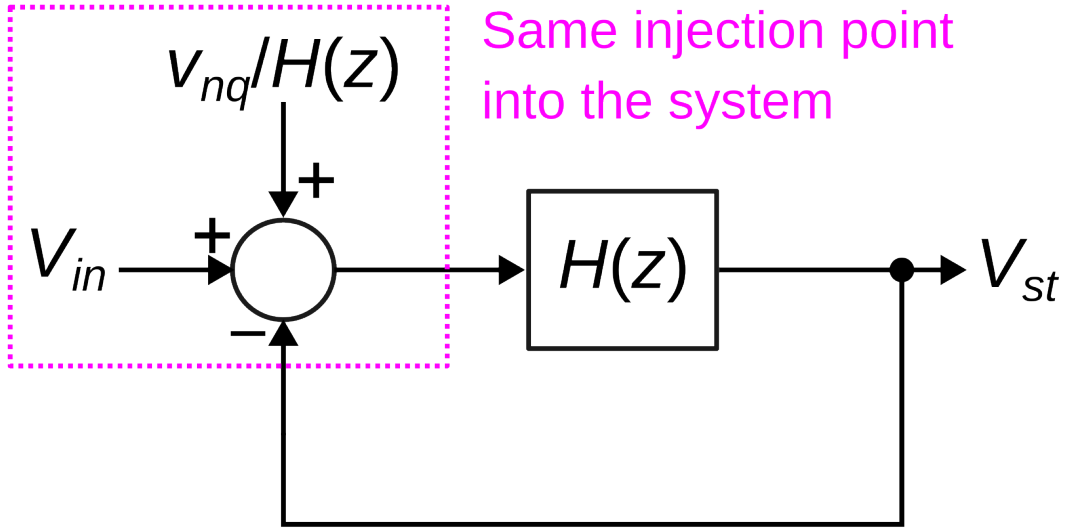


for $f=f_S/2$, the argument of $\sin^2$ is $\pi/2$

NTF: derivation from system perspective



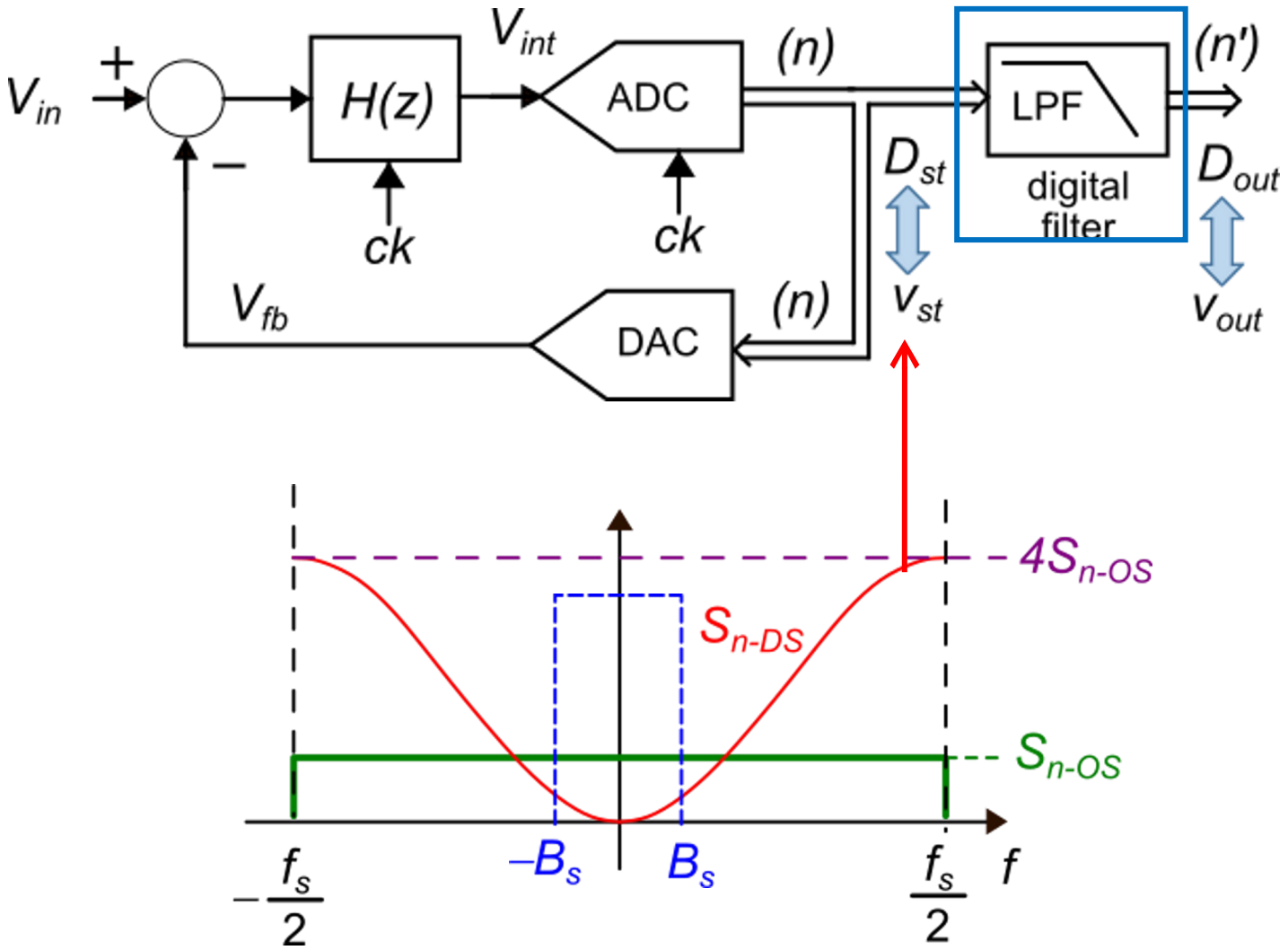




$$V_{st} = \mathrm{STF} \cdot \left(V_{in} + \frac{v_{nq}}{H(z)} \right) = \mathrm{STF} \cdot V_{in} + \frac{\mathrm{STF}}{H(z)} \cdot v_{nq}$$

NTF

Output noise power in the Delta-Sigma ADC



$$\left\langle v^2_{n\text{-}out} \right\rangle = \int_{B_S}^{B_S} S_{n\text{-}DS}(f)\,df$$

$$\left\langle v^2_{n\text{-}out} \right\rangle = S_{n\text{-}OS} \int_{B_S}^{B_S} 4\sin^2\left(\pi \frac{f}{f_S}\right) df$$

$$\sin\left(\pi \frac{f}{f_S}\right) \cong \pi \frac{f}{f_S}$$

$$\left\langle v^2_{n\text{-}out} \right\rangle \cong S_{n\text{-}OS} \int_{B_S}^{B_S} 4\left(\pi \frac{f}{f_S}\right)^2 df$$

Output noise power in the Delta-Sigma ADC

$$\left\langle v_{n\text{-}out}^2 \right\rangle \cong S_{n\text{-}OS} \int_{B_S}^{B_S} 4\left(\pi \frac{f}{f_S}\right)^2 df = S_{n\text{-}OS}\, 4\pi^2 \frac{1}{f_S^2} \int_{B_S}^{B_S} f^2 df$$

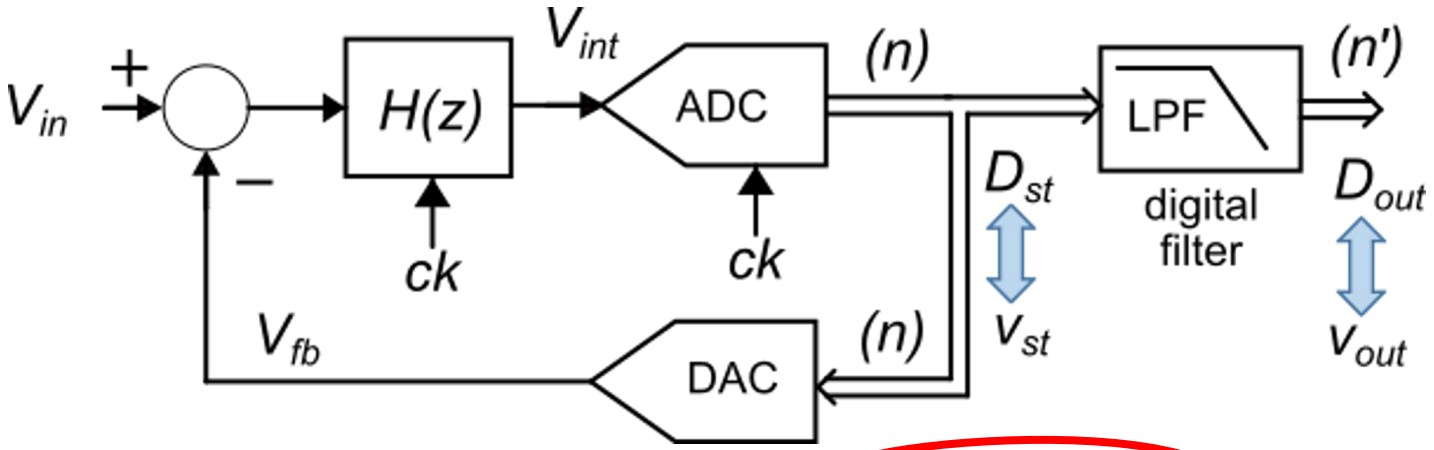
$$\left\langle v_{n\text{-}out}^2 \right\rangle \cong S_{n\text{-}OS}\, 4\pi^2 \frac{1}{f_S^2} \frac{2}{3} B_S^3 \qquad S_{n\text{-}OS} = \frac{S_{n\text{-}NR}}{r_{OS}} \qquad \left(r_{OS} = \frac{f_S}{2B_S} \right)$$

$$\left\langle v_{n\text{-}out}^2 \right\rangle \cong \frac{S_{n\text{-}NR}}{r_{OS}} 4\pi^2 \frac{1}{f_S^2} \frac{2}{3} B_S^3 \qquad 8B_S^3 = 2B_S \cdot (2B_S)^2$$

$$\left\langle v_{n\text{-}out}^2 \right\rangle \cong \frac{S_{n\text{-}NR} \cdot 2B_S}{r_{OS}} \frac{\pi^2}{3} \left(\frac{2B_S}{f_S}\right)^2 \frac{1}{r_{OS}^2} \qquad \left\langle v_{nq\text{-}NR}^2 \right\rangle$$

$$\left\langle v_{n\text{-}out}^2 \right\rangle \cong \left\langle v_{nq\text{-}NR}^2 \right\rangle \frac{\pi^2}{3} \frac{1}{r_{OS}^3}$$

Resolution increment in the first-order Δ–Σ ADC



$$n_2 - n_1 = \frac{1}{2}\log_2\left(\frac{\langle v_{n1}^2\rangle}{\langle v_{n2}^2\rangle}\right)$$

$$\langle v_{n-out}^2\rangle \cong \langle v_{nq-NR}^2\rangle \frac{\pi^2}{3}\frac{1}{r_{OS}^3}$$

$$\frac{1}{2}\log_2\left(\frac{3}{\pi^2}\right)$$

$$n' - n = \frac{1}{2}\log_2\left(r_{OS}^3\,\frac{3}{\pi^2}\right)$$

$$n' - n = \frac{3}{2}\log_2(r_{OS}) - 0.86$$

Resolution increment in the first order Δ–Σ ADC

$$n' - n = \frac{3}{2}\log_2(r_{OS}) - 0.86$$

Every increment of r_{OS} by a factor of 2 produces a resolution gain of 1 and 1/2 bit (1.5 bits).
This gain was only 1/2 bit in the pure oversampling ADC

Example

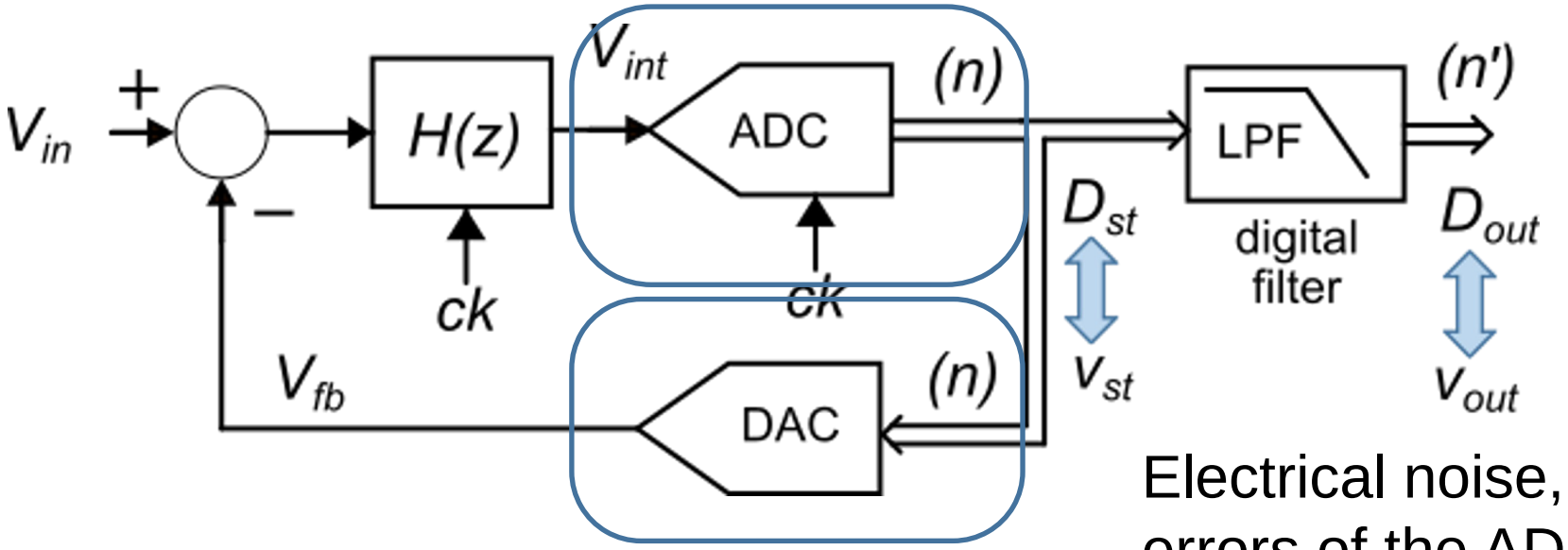
$$n' - n = 11 \text{ bits}$$

$$r_{OS} = 2^{\frac{2}{3}(n' - n + 0.86)} \cong 240$$

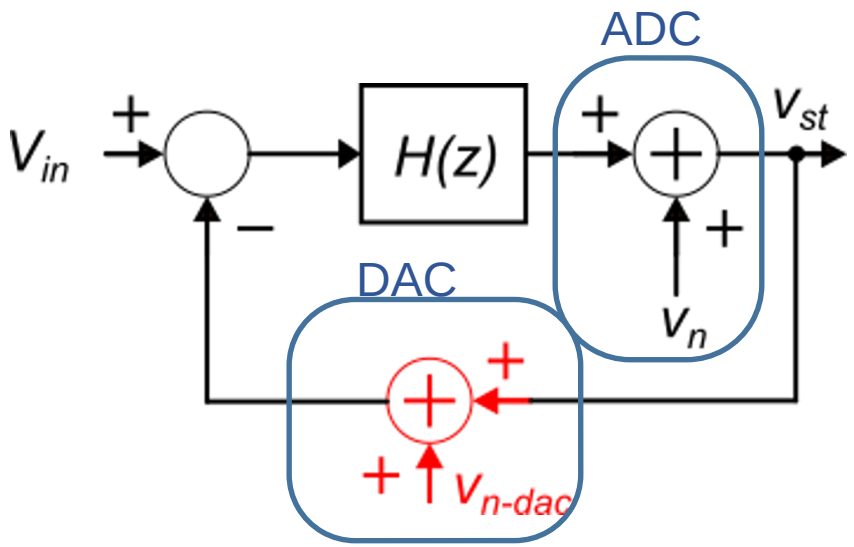
$$(n' - n + 0.86)\frac{2}{3} = \log_2(r_{OS})$$

This OSR value is rather large, but also the gain in resolution is very large
Starting with a comparator (single-bit quantizer), it is possible to obtain 12 bits

ADC and DAC non idealities in Δ–Σ ADC



Electrical noise, offset and non-linearity errors of the ADC are shaped by the high pass NTF of the modulator, then the effect on the signal BW is negligible.



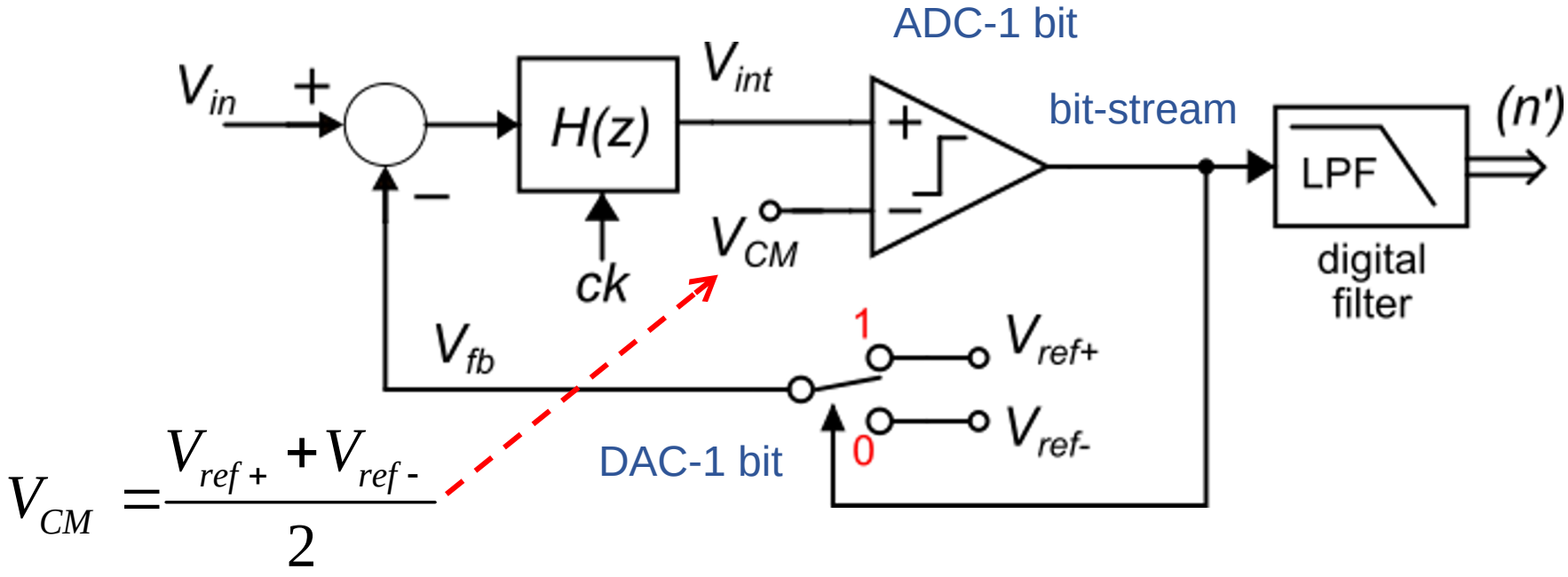
The **DAC** should be linear because it is in the feedback path. The DAC noise (that includes also non-linearity errors) are simply summed-up to the input signal.

Single-bit Δ–Σ ADC

As we have seen, the DAC linearity is a main issue of the Δ–Σ approach

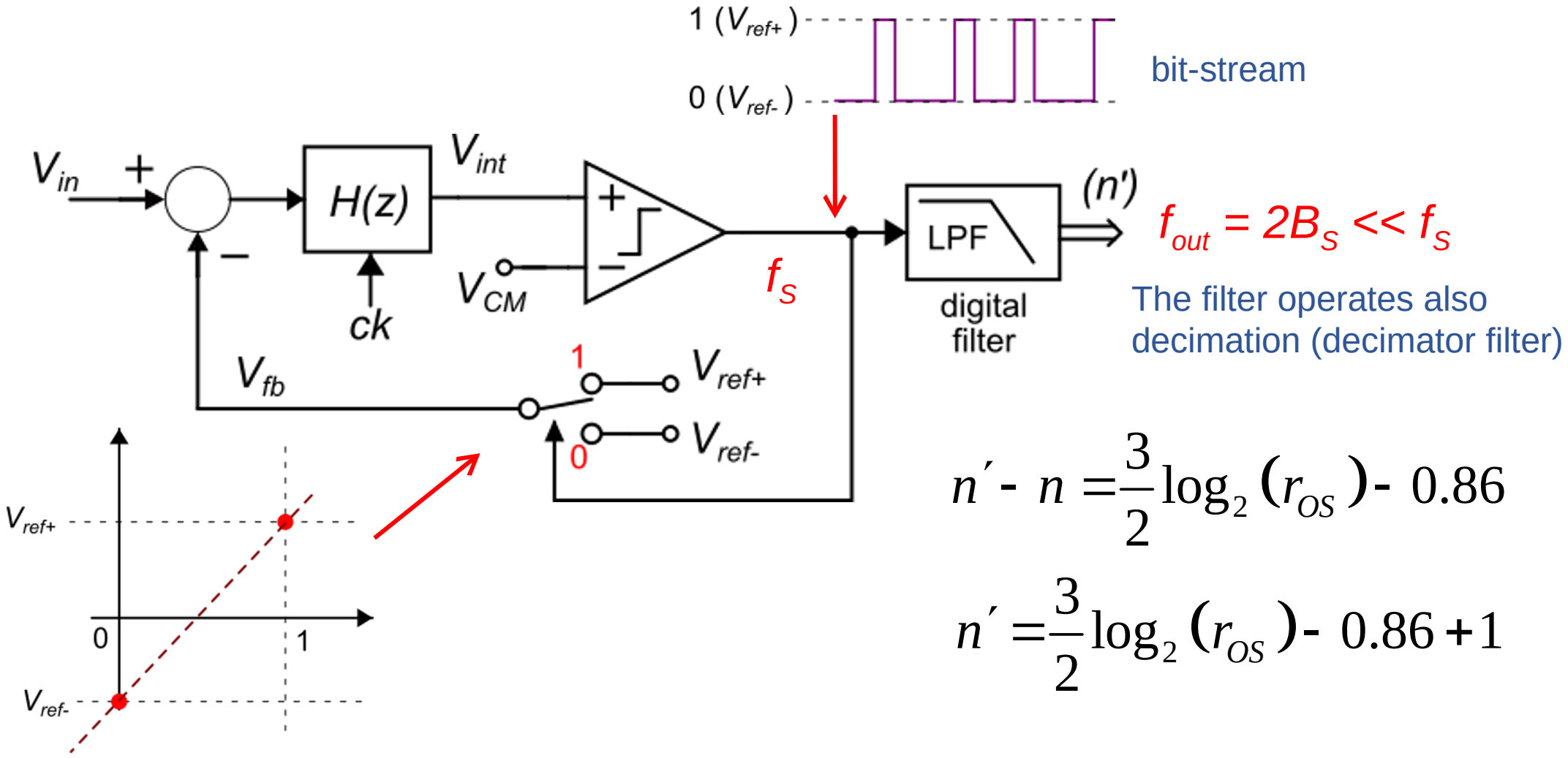
A widely used solution is the single bit Δ–Σ ADC

In the single bit D-S ADC the internal Nyquist-rate ADC is a single-bit quantizer, i.e., a comparator



Single-bit Δ–Σ ADC

[Tutorial Analog-Devices Delta-Sigma]



$$n' - n = \frac{3}{2}\log_2(r_{OS}) - 0.86$$

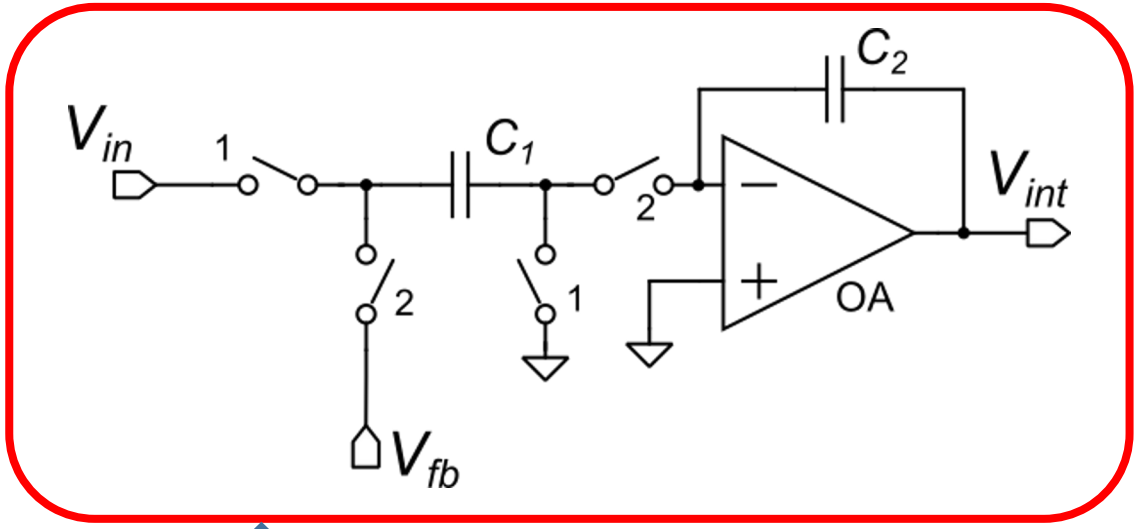
$$n' = \frac{3}{2}\log_2(r_{OS}) - 0.86 + 1$$

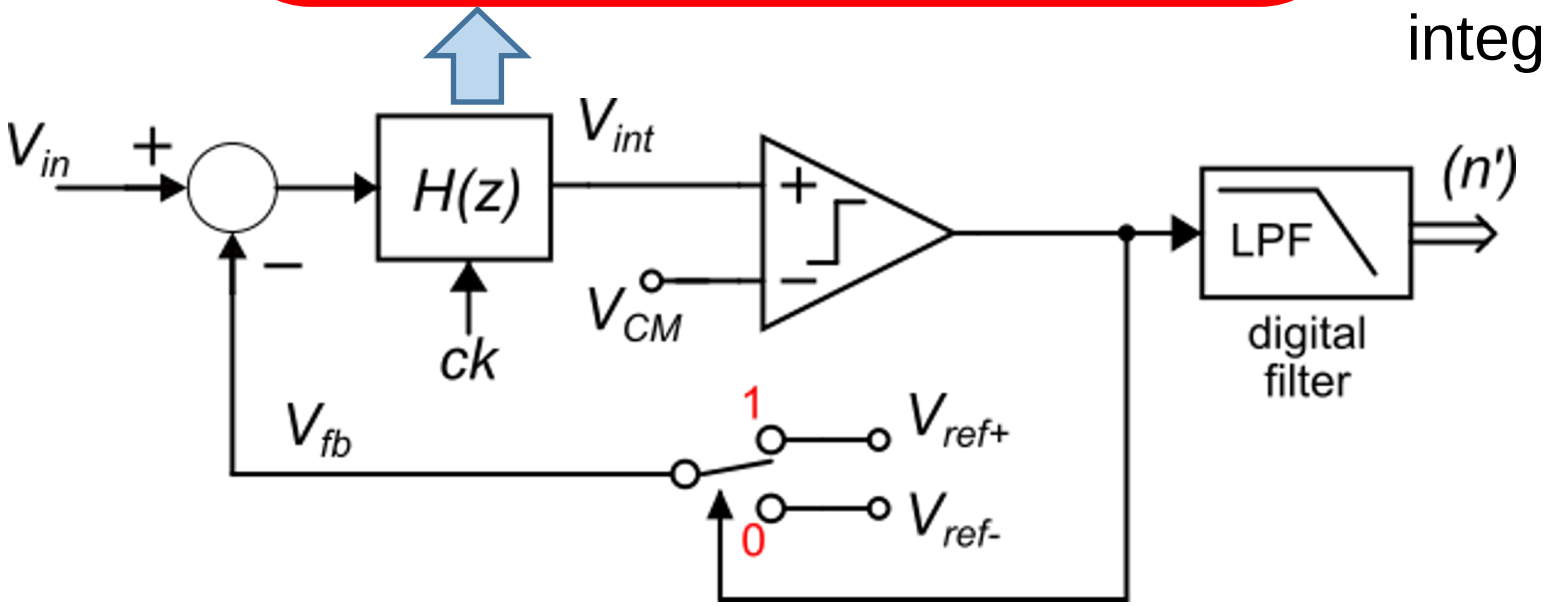
A 1-bit DAC is inherently linear: no distortion degradation of ENOB

H(z) implementation (Single ended)

Classical, "parasitic insensitive" Switched Capacitor Integrator

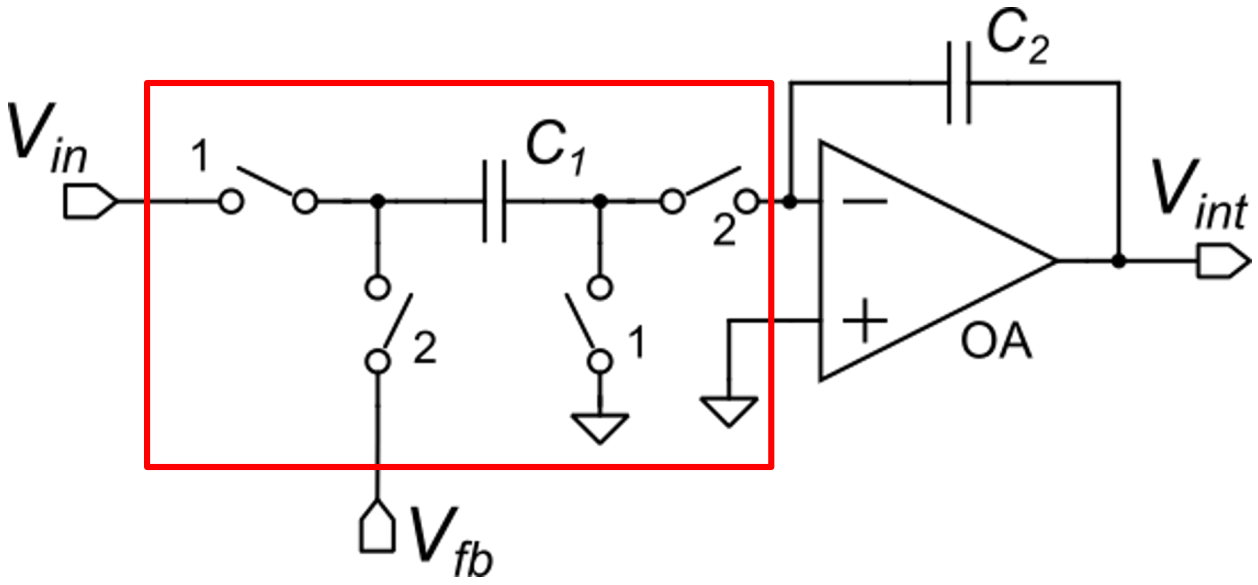
$$H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}}$$





Note: electrical noise and distortion of the DT integrator are not shaped by the NTF: careful design of the integrator is required.

Physical noise



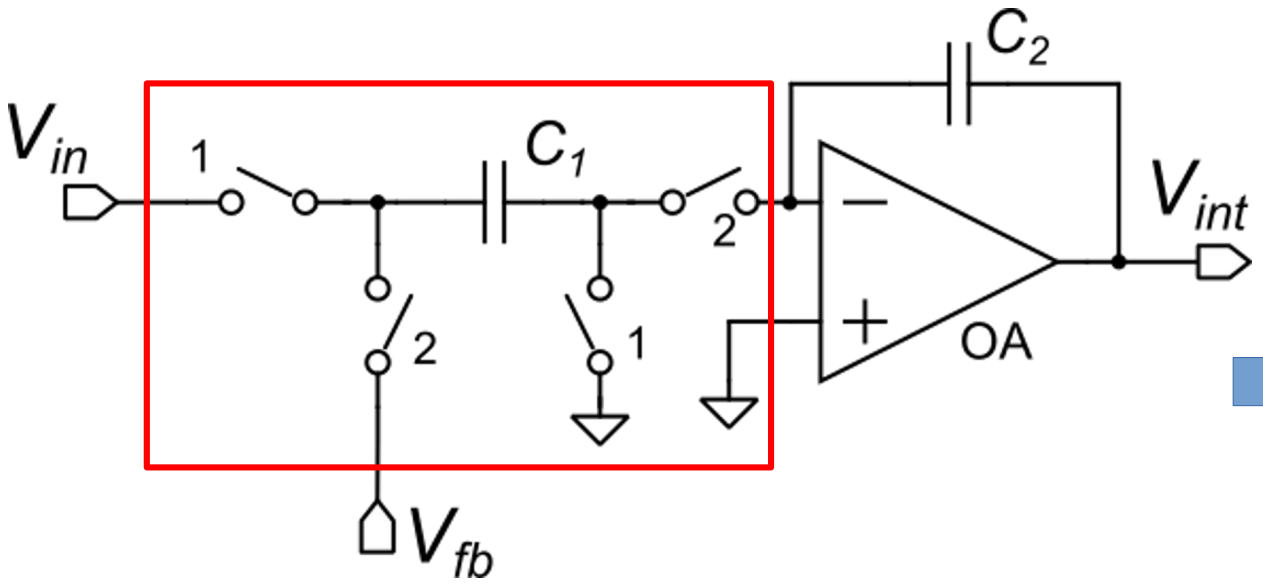
At each phase of the SC integrator, in addition to the charge transfer from C1 to C2, the sampling process produces noise as a consequence of a **thermal noise** generated due to finite ON resistance of the switch: KT/C noise.

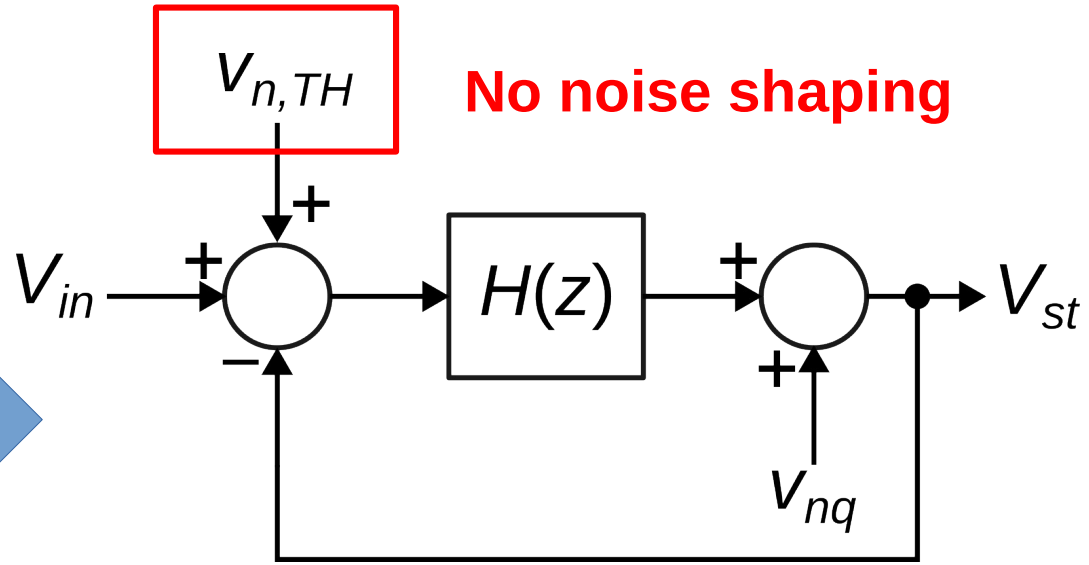
Power (V^2) of the KT/C process on C1:

$$\langle v_{n,TH}^2 \rangle = 2 \times \frac{KT}{C_1}$$

This error is added before the accumulation into C2: hence from the system-level point of view it is injected into the system at the system input

Physical noise

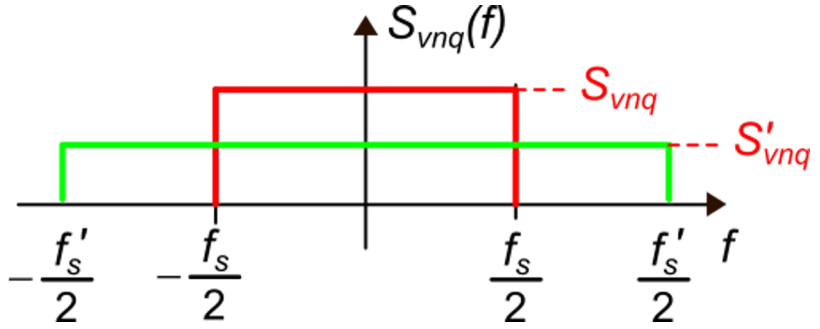




$$\langle v_{n,TH}^2 \rangle = 2 \times \frac{KT}{C_1}$$

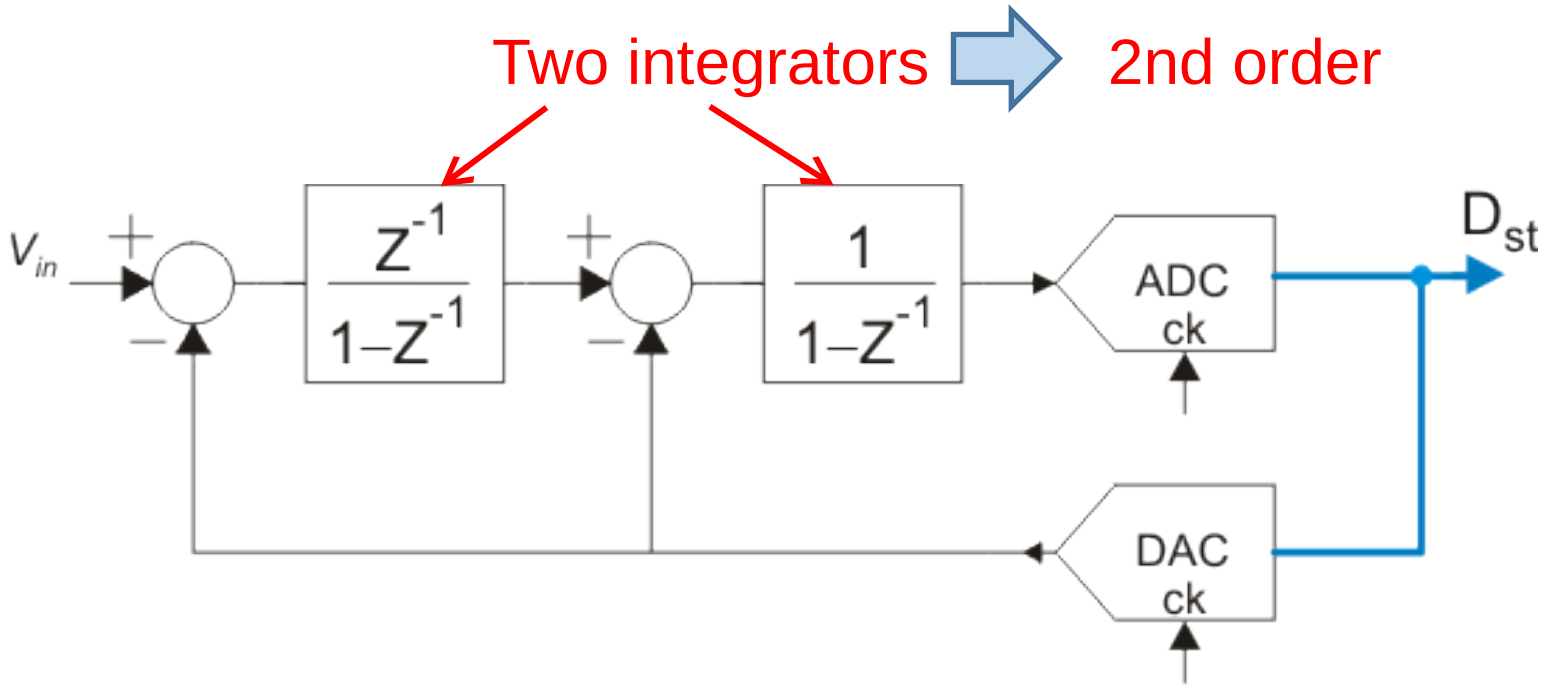
Produced as broadband (thermal) noise among +/-fs/2

Within the signal bandwidth, the power is divided by OSR (r_{OS})



Higher order Δ–Σ ADCs

Example: second-order ADC



Advantage: 2.5 bits are gained doubling the OSR (instead of 1.5 bits).
Same final resolution with a much smaller OSR
The 2nd order D-S ADC is a very popular converter for sensor interfaces.