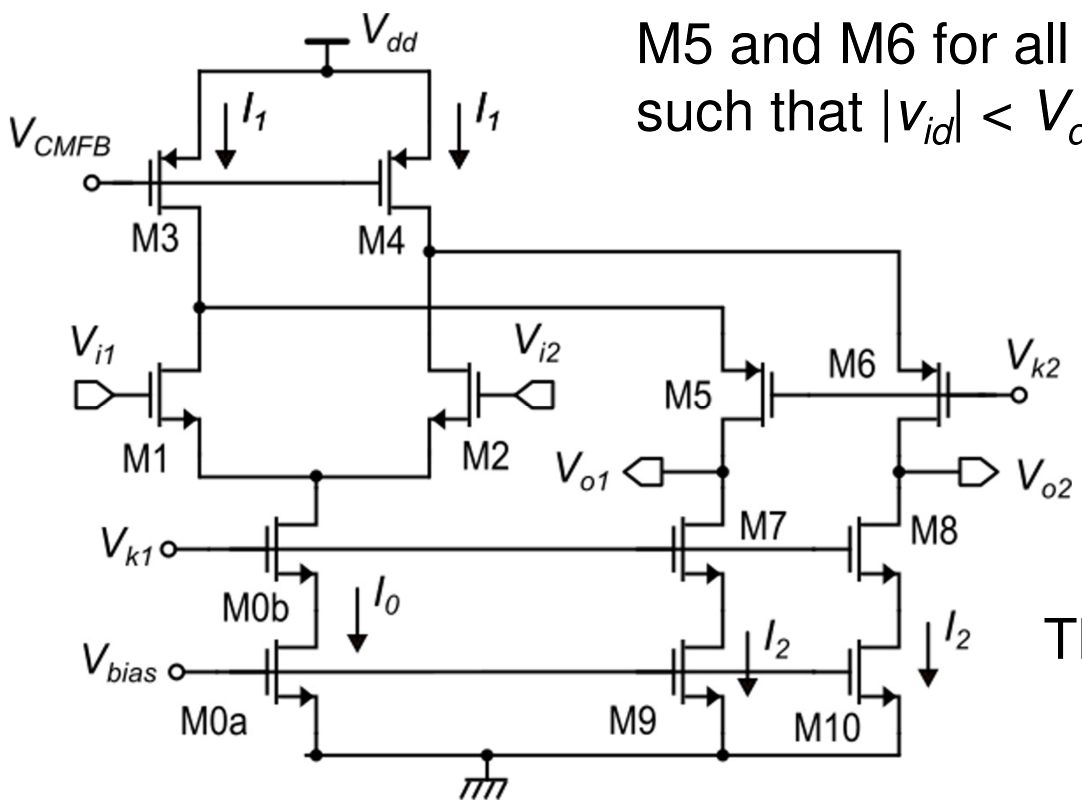
Folded cascode amplifier: quiescent current and total supply current



In order to avoid turning off M5 and M6 for all v_{id} values such that $|v_{id}| < V_{dmax}$ ⇨ $I_1 \geq \max\left(I_{D1}\right) = I_0$

We usually choose: $I_1 = I_0$

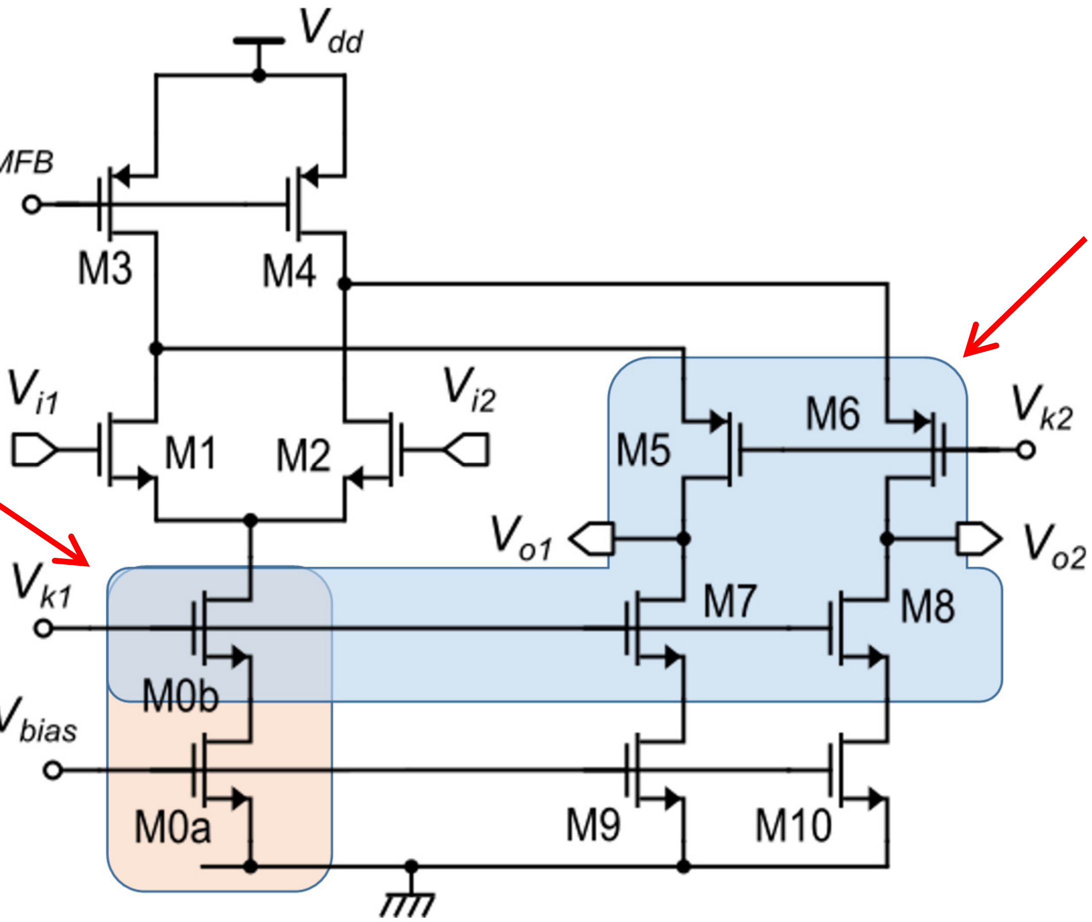
Since it must be: $I_1 - \dfrac{I_0}{2} - I_2 = 0$

then: $I_2 = \dfrac{I_0}{2}$

The supply current is: $I_{supply} = 2I_1 = 2I_0$

Folded cascode fully-differential amplifier: noise analysis

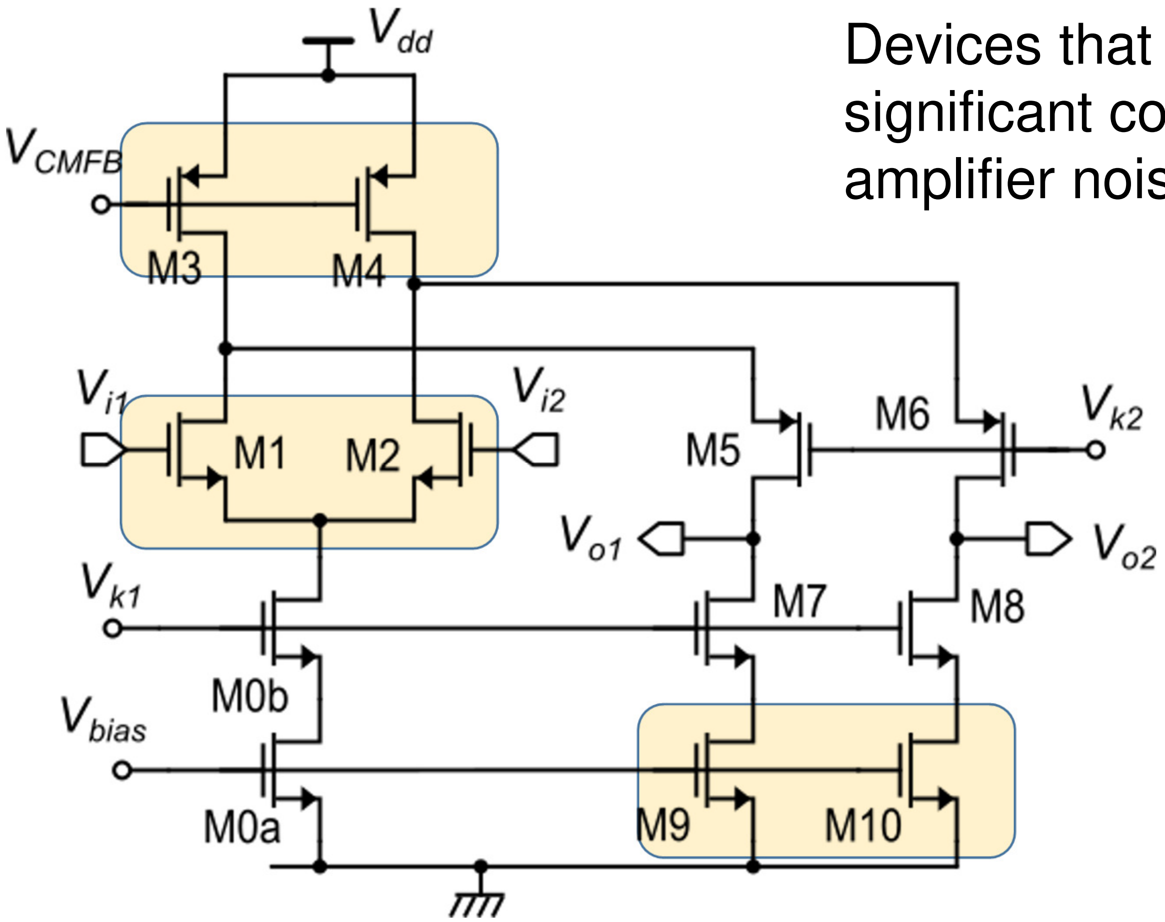
These devices give common mode contributions (except when the amplifier is unbalanced by a large differential input voltage)



All these MOSFET form common gate stages.

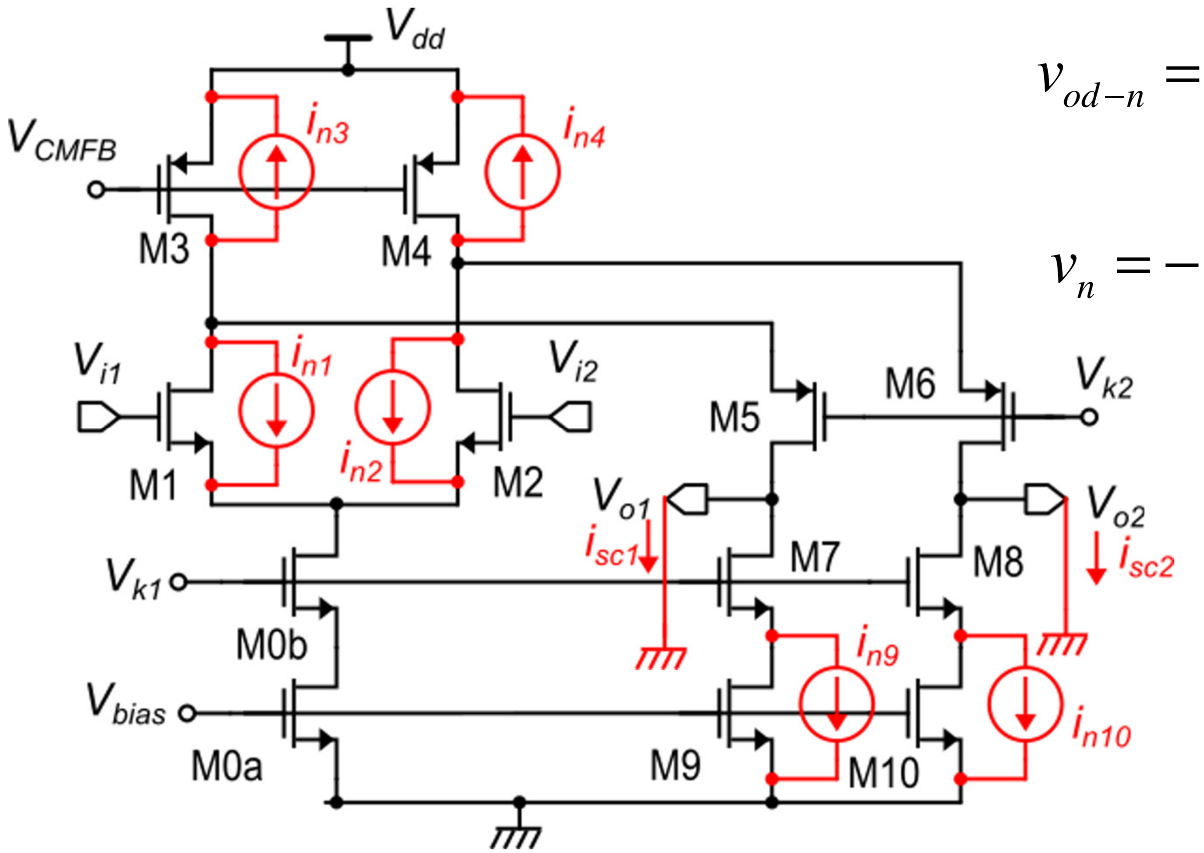
Their noise and offset contribution can be neglected up to relatively high frequencies

Fully-differential amplifier: noise analysis



Devices that gives a significant contribution to the amplifier noise and offset

Calculation of the input referred noise (and offset).



$$v_{od-n} = v_{o2-n} - v_{o1-n} = R_{out}\left(i_{sc2-n} - i_{sc1-n}\right)$$

$$v_n = -\frac{v_{od-n}}{A_{dd}} = -\frac{v_{od-n}}{g_{m1}R_{out}} = \frac{-\left(i_{sc2-n} - i_{sc1-n}\right)}{g_{m1}}$$

$$\begin{cases} i_{sc1-n} = -i_{n3} - i_{n1} - i_{n9} \\ i_{sc2-n} = -i_{n4} - i_{n2} - i_{n10} \end{cases}$$

Calculation of the input referred noise.

$$\begin{cases} i_{sc1-n} = -i_{n3} - i_{n1} - i_{n9} \\ i_{sc2-n} = -i_{n4} - i_{n2} - i_{n10} \end{cases}$$

$$v_n = \frac{-\left(i_{sc2-n} - i_{sc1-n}\right)}{g_{m1}} = \frac{\left(i_{sc1-n} - i_{sc2-n}\right)}{g_{m1}}$$

$$v_n = \frac{\left(i_{n2} - i_{n1}\right) + \left(i_{n4} - i_{n3}\right) + \left(i_{n10} - i_{n9}\right)}{g_{m1}}$$

This expression can be used for both the noise and offset analysis

Noise

$$v_n = \frac{(i_{n2} - i_{n1}) + (i_{n4} - i_{n3}) + (i_{n10} - i_{n9})}{g_{m1}}$$

$$S_{vn} = 2\frac{S_{I1} + S_{I3} + S_{I9}}{g_{m1}^2}$$

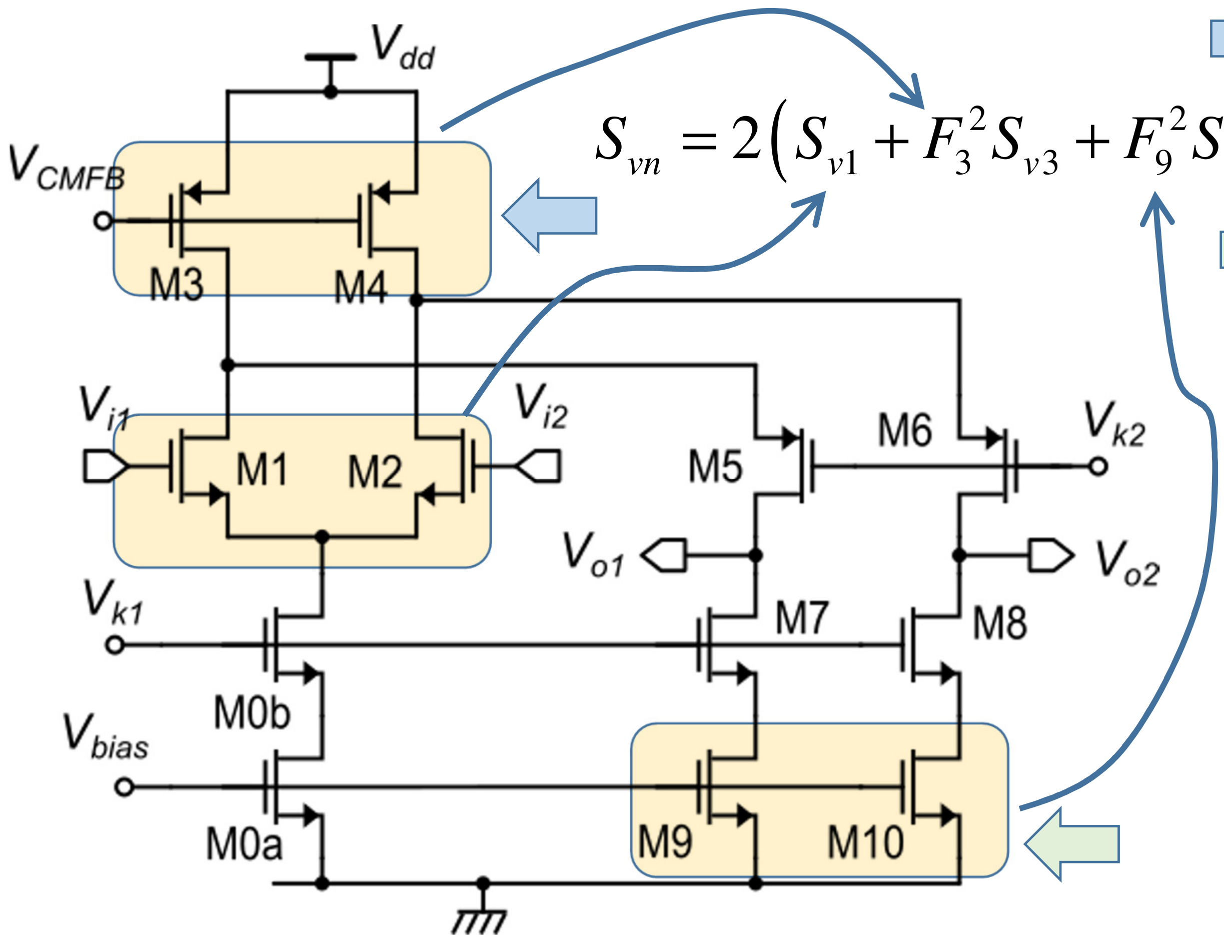
Expressing the S_I as a function of the PSDs of the gate referred voltage noise (S_V)

$$S_{vn} = 2\frac{g_{m1}^2 S_{v1} + g_{m3}^2 S_{v3} + g_{m9}^2 S_{v9}}{g_{m1}^2} = 2\left(S_{v1} + \frac{g_{m3}^2}{g_{m1}^2} S_{v3} + \frac{g_{m9}^2}{g_{m1}^2} S_{v9} \right)$$

$$S_{vn} = 2\left(S_{v1} + F_3^2 S_{v3} + F_9^2 S_{v9} \right)$$

$$\begin{cases} F_3 = \dfrac{g_{m3}}{g_{m1}} = \dfrac{I_{D3}}{I_{D1}} \dfrac{V_{TE1}}{V_{TE3}} \\ F_9 = \dfrac{g_{m9}}{g_{m1}} = \dfrac{I_{D9}}{I_{D1}} \dfrac{V_{TE1}}{V_{TE9}} \end{cases}$$

Fully-differential amplifier: noise analysis



$$S_{vn}=2\left(S_{v1}+F_3^2S_{v3}+F_9^2S_{v9}\right)$$

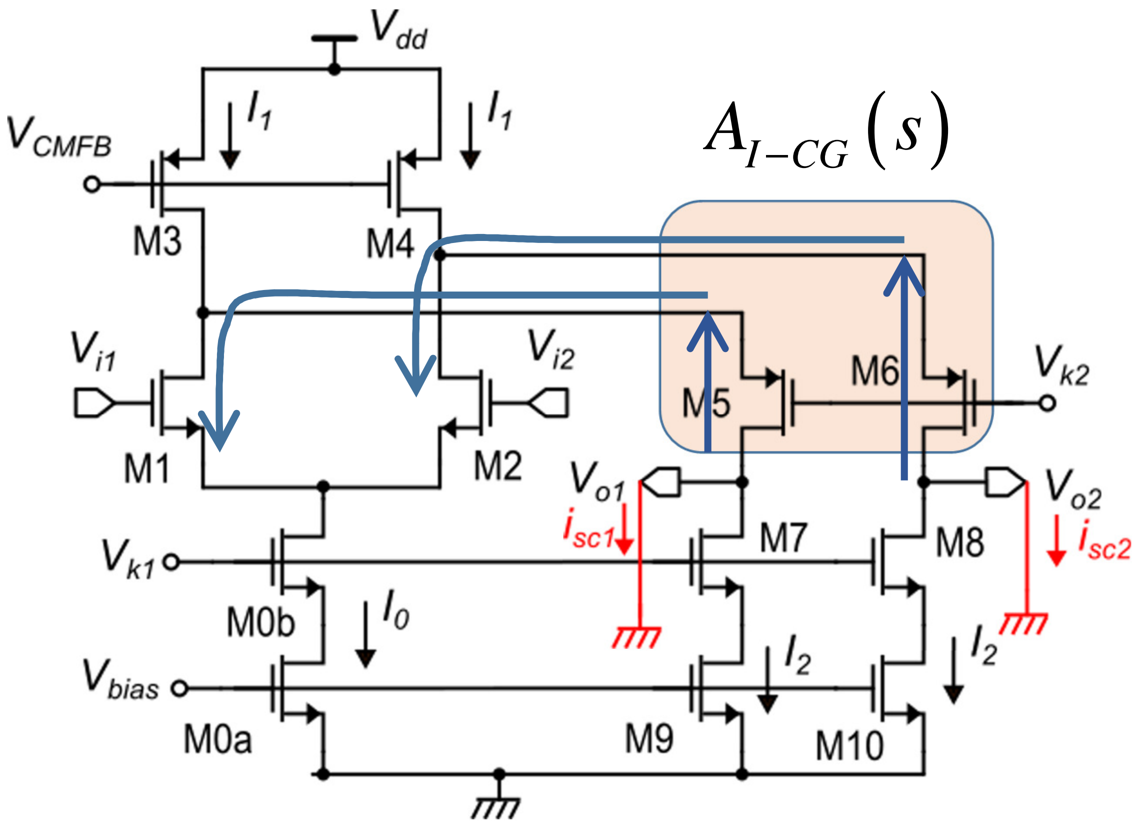
$$\begin{cases} F_3=\dfrac{g_{m3}}{g_{m1}}=\dfrac{I_{D3}}{I_{D1}}\dfrac{V_{TE1}}{V_{TE3}}=2\dfrac{V_{TE1}}{V_{TE3}} \\ F_9=\dfrac{g_{m9}}{g_{m1}}=\dfrac{I_{D9}}{I_{D1}}\dfrac{V_{TE1}}{V_{TE9}}=\dfrac{V_{TE1}}{V_{TE9}} \end{cases}$$

$$I_{D3}=I_1=I_0$$

$$I_{D1}=\frac{I_0}{2} \qquad I_{D9}=I_2=\frac{I_0}{2}$$

$\mathbf{F_3}$ is difficult to make <<1 since it includes a factor of 2 and making $V_{TE3} >> V_{TE1}$ would result in <u>reduced output swing</u>

Frequency response of the folded cascode op-amp

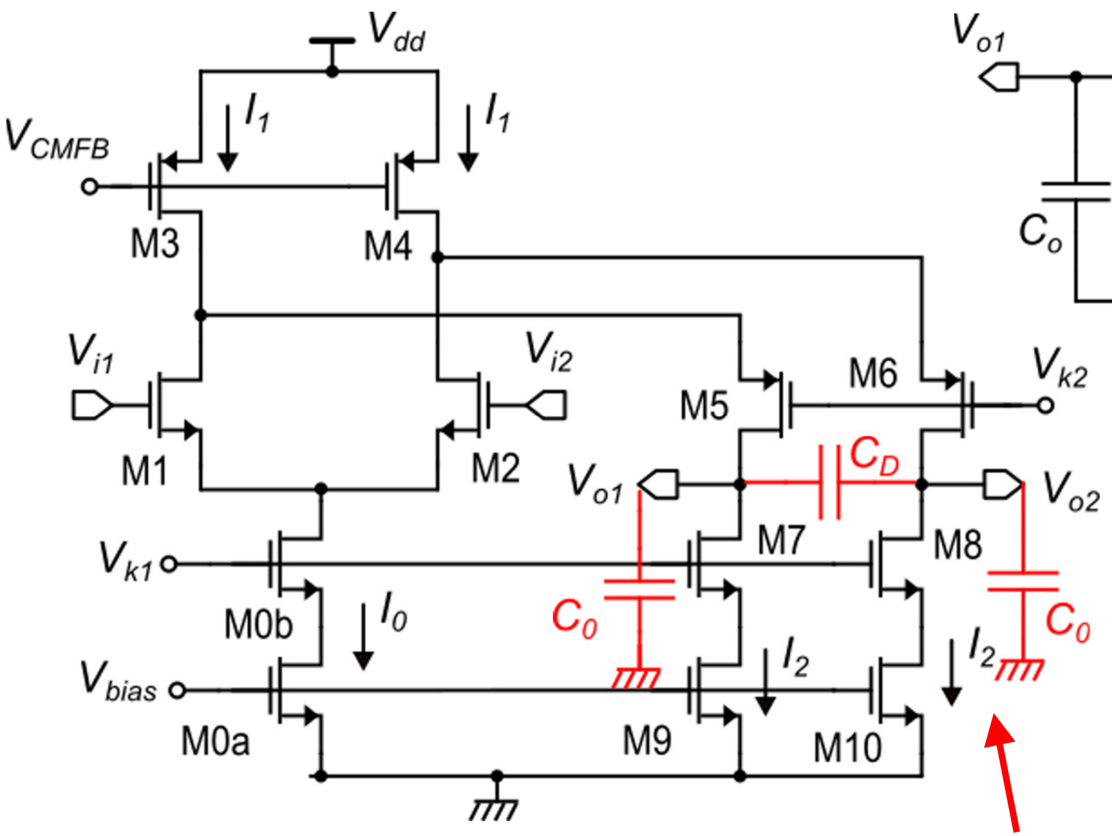


Let us analyze the frequency response of the output short circuit currents.

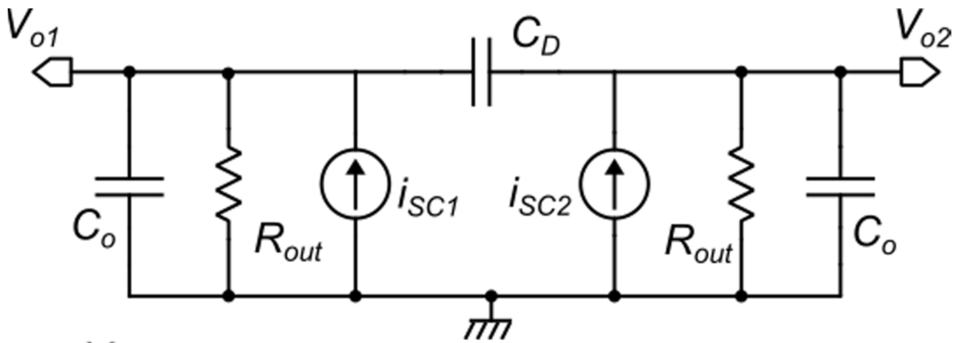
The drain current variations produced by the input pair reach the output port passing through the common gate stage

Let us indicate the transfer function of the common gate as $A_{I\text{-}CG}(s)$

Frequency response of the folded cascode op-amp



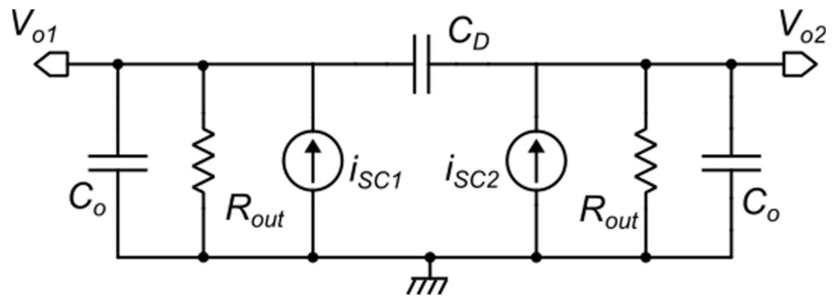
C_O,C_D: Load capacitances

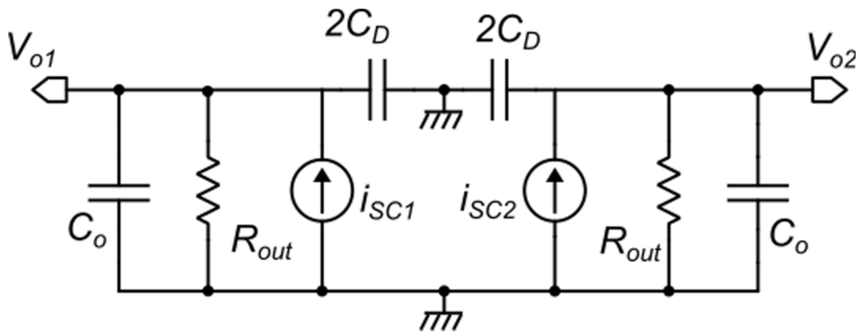


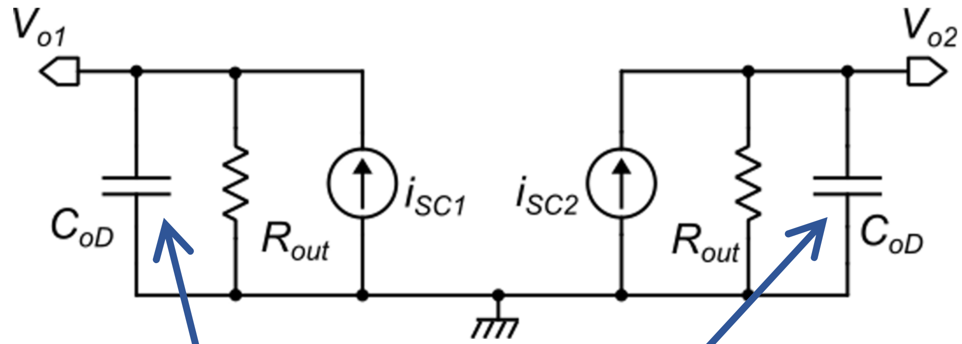
Small signal circuit of the output ports

$$
\begin{cases}
i_{sc1} = \left(-g_{m1}\dfrac{v_{id}}{2}\right) A_{I-CG}(s) \\
i_{sc2} = \left(g_{m1}\dfrac{v_{id}}{2}\right) A_{I-CG}(s)
\end{cases}
$$

Differential mode analysis

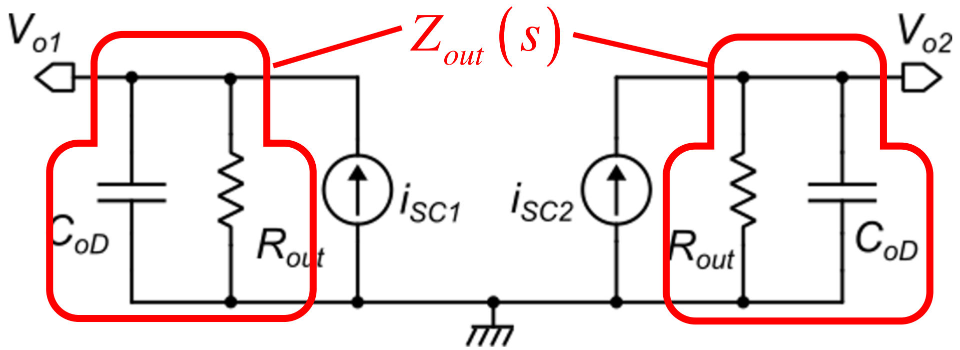






$$C_{oD} = C_o + 2C_D$$

Differential mode analysis



$$\begin{cases} i_{sc1} = \left(-g_{m1}\dfrac{v_{id}}{2}\right) A_{I-CG}(s) \\ i_{sc2} = \left(g_{m1}\dfrac{v_{id}}{2}\right) A_{I-CG}(s) \end{cases}$$

$$v_{od} = v_{o2} - v_{o1} = Z_{out}(s)\, i_{sc2} - Z_{out}(s)\, i_{sc1}$$

$$v_{od} = (i_{sc2} - i_{sc1}) Z_{out}(s)$$

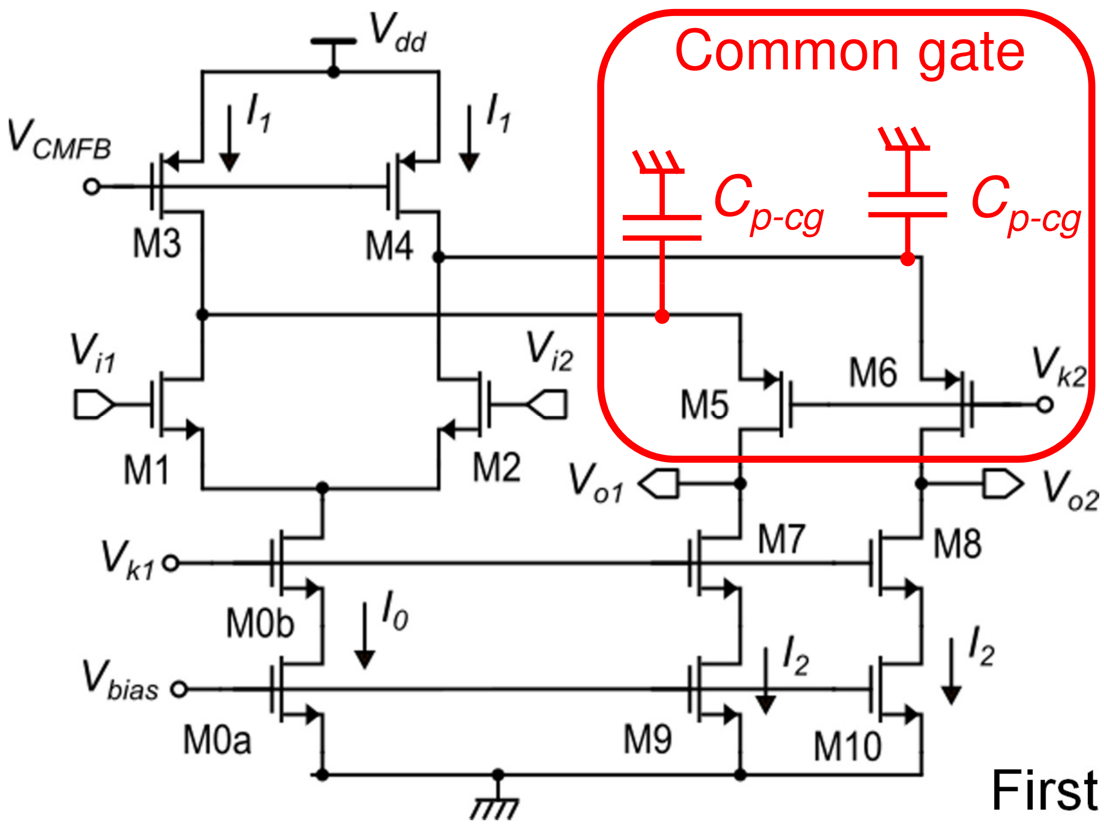
$$v_{od} = g_{m1} v_{id} A_{I-CG}(s) R_{out} \frac{1}{1 + sC_{oD}R_{out}}$$

$$Z_{out}(s) = \frac{1}{\dfrac{1}{R_{out}} + sC_{oD}} = \frac{R_{out}}{1 + sC_{oD}R_{out}}$$

$$A_{I-CG}(s) \cong \frac{1}{1 + \dfrac{s}{\omega_{pCG}}}$$

Response of the common gate

Differential mode analysis



$$v_{od} = g_{m1} v_{id} A_{I-CG}(s) R_{out} \frac{1}{1 + sC_{oD}R_{out}}$$

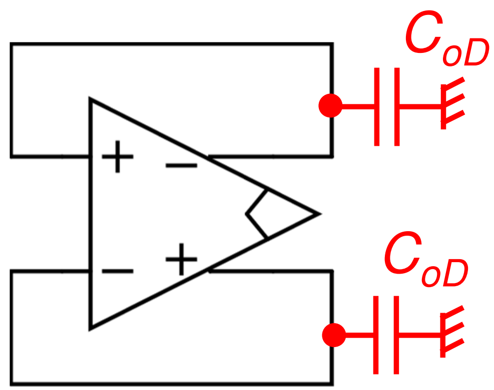
$$A_{dd}(s) = \underbrace{g_{m1} R_{out}}_{A_{dd}(0)} \frac{1}{\left(1 + \dfrac{s}{\omega_{pCG}}\right)} \cdot \frac{1}{\left(1 + \dfrac{s}{\omega_{pd}}\right)}$$

Dominant pole: $\omega_{pd} = \dfrac{1}{C_{oD} R_{out}}$

First non dominant pole: $\omega_{pCG} = \dfrac{g_{m5}}{C_{p-cg}} \cong \dfrac{g_{m5}}{C_{gs5}} \cong f_{T5}$

Differential mode analysis: stability in closed loop configurations

Unity gain angular-frequency:



$$\omega_{0d} = \omega_{pd} A_{dd}(0) = 2\pi GBW$$

$$\omega_{pd} = \frac{1}{C_{oD} R_{out}} \qquad \omega_{0d} = \frac{g_{m1} R_{out}}{C_{oD} R_{out}} = \frac{g_{m1}}{C_{oD}}$$

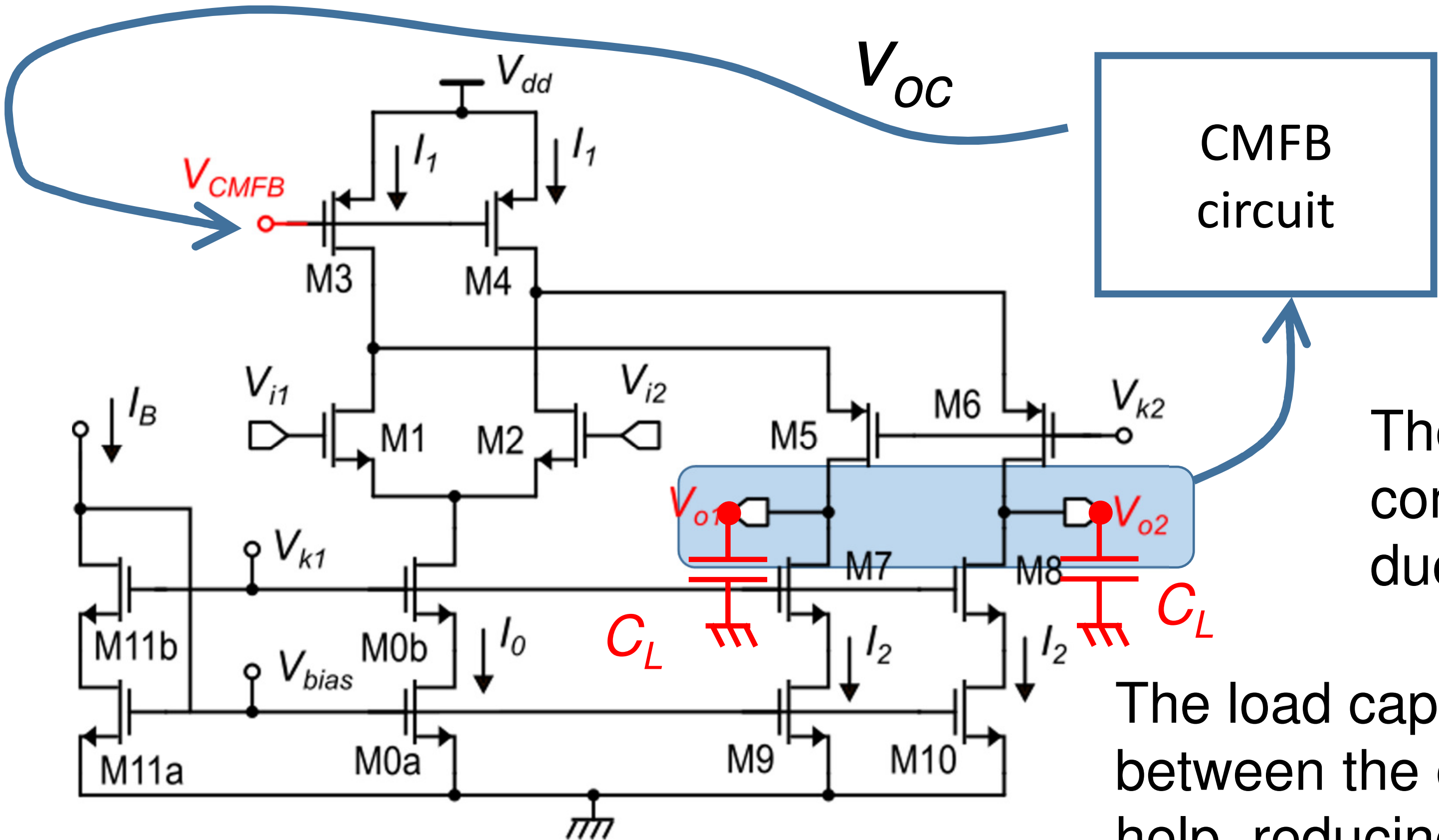
First non dominant pole: $\omega_2 = \omega_{pCG} \cong \dfrac{g_{m5}}{C_{gs5}}$

Worst case for stability: $|\beta|=1$

To have about 70° phase margin: $\omega_2 = 3\omega_{0d}$

Increasing the equivalent differential-mode load capacitances (C_{oD}) reduces the unity gain angular frequency (ω_{0d}), improving the phase margin but also reduces the GBW.

Mention to common mode stability



Considering small signal components, this is a feedback loop that can lead to instability

The dominant pole of the common mode loop is still due to the output capacitance

The load capacitances, if connected between the outputs and ground, help reducing the 0-dB frequency of the CMFB loop, improving stability

Example of commercial fully-differential op-amp: LTC6362

DC-Coupled Interface from a Ground-Referenced Single-Ended Input to an LTC2379-18 SAR ADC