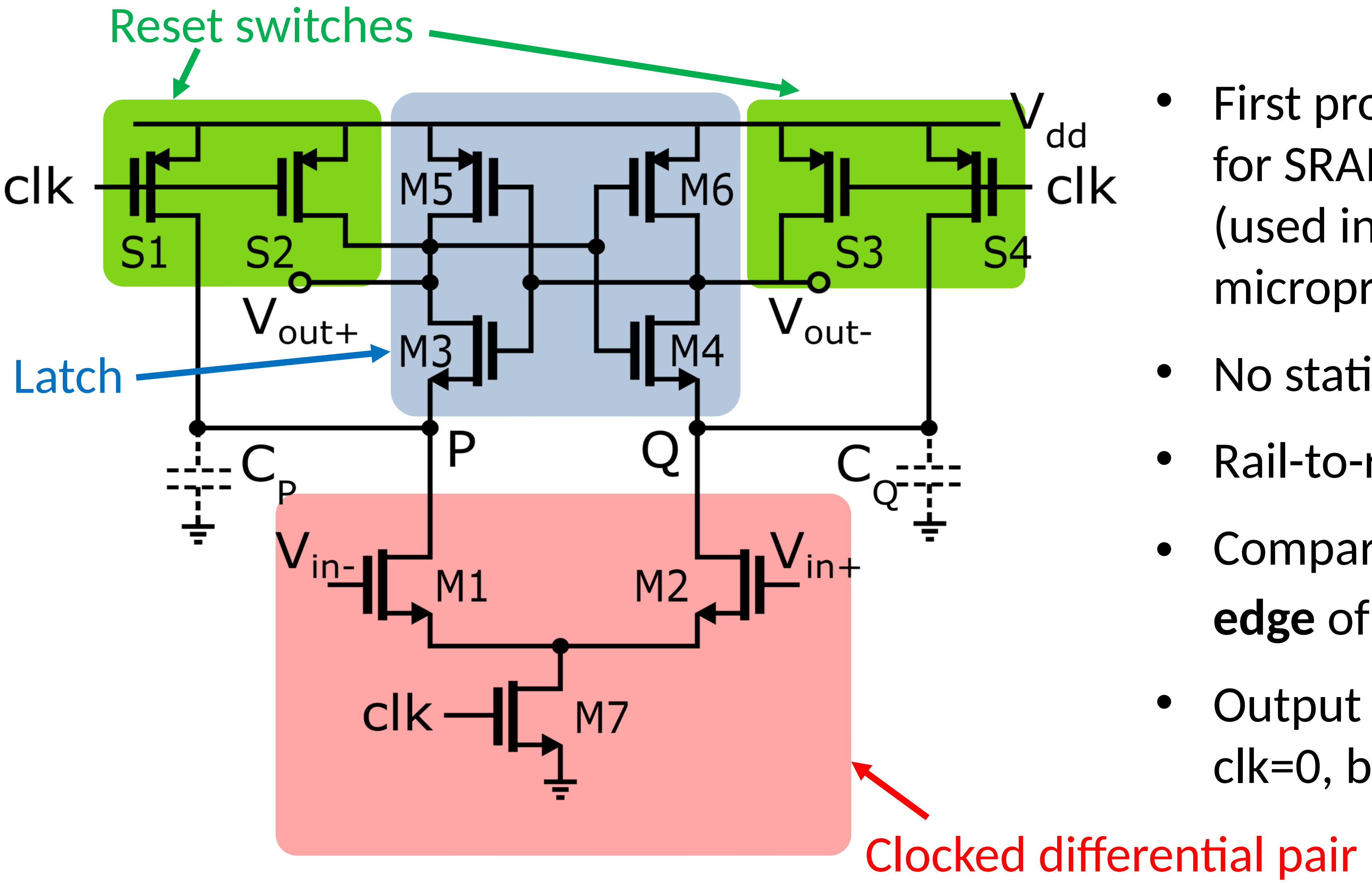
StrongARM: insights from literature

Analysis inspired by “The StrongARM Latch” paper from Prof. B. Razavi

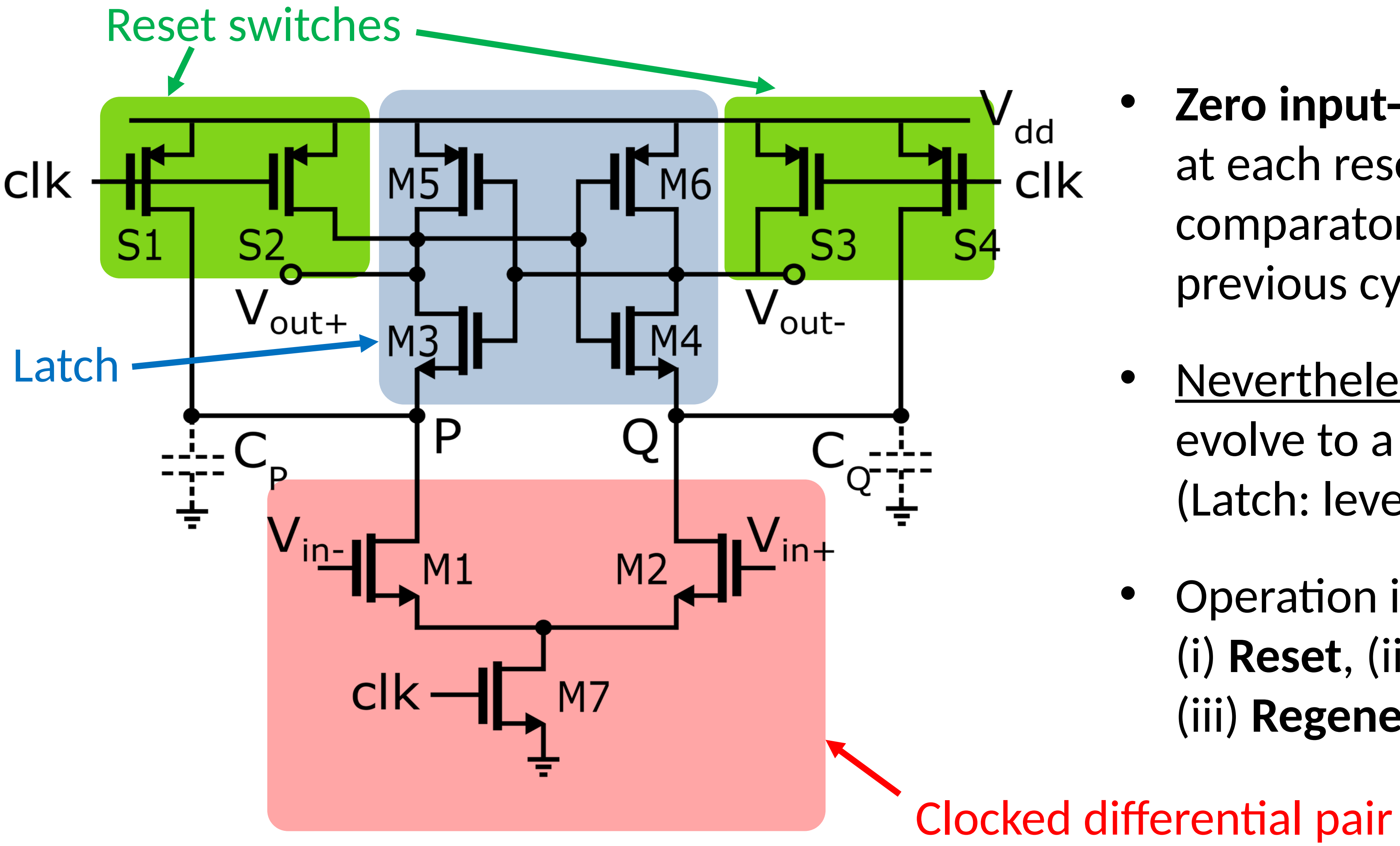
DOI: 10.1109/MSSC.2015.2418155

Dynamic comparator: StrongARM structure



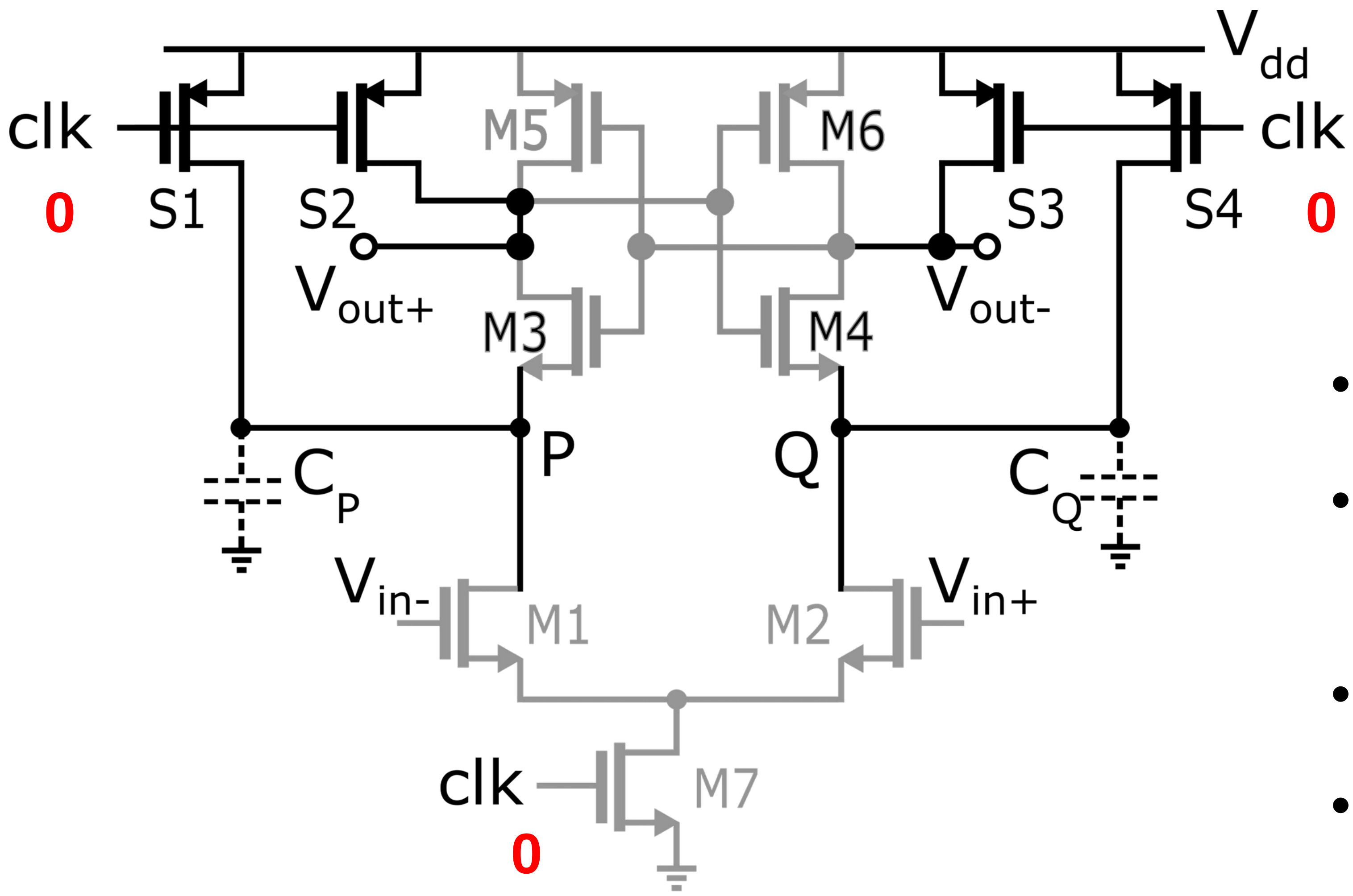
- First proposed as <u>Sense Amplifier</u> for SRAM (used in StrongARM microprocessor, in the '90s)
- No static-power consumption
- Rail-to-rail outputs
- Compares $V_{id} = V_{in}^{+} - V_{in}^{-}$ on the **rising edge** of the clock signal
- Output valid when clk=1. During clk=0, both Vout+, Vout- are at Vdd

Dynamic comparator: StrongARM structure



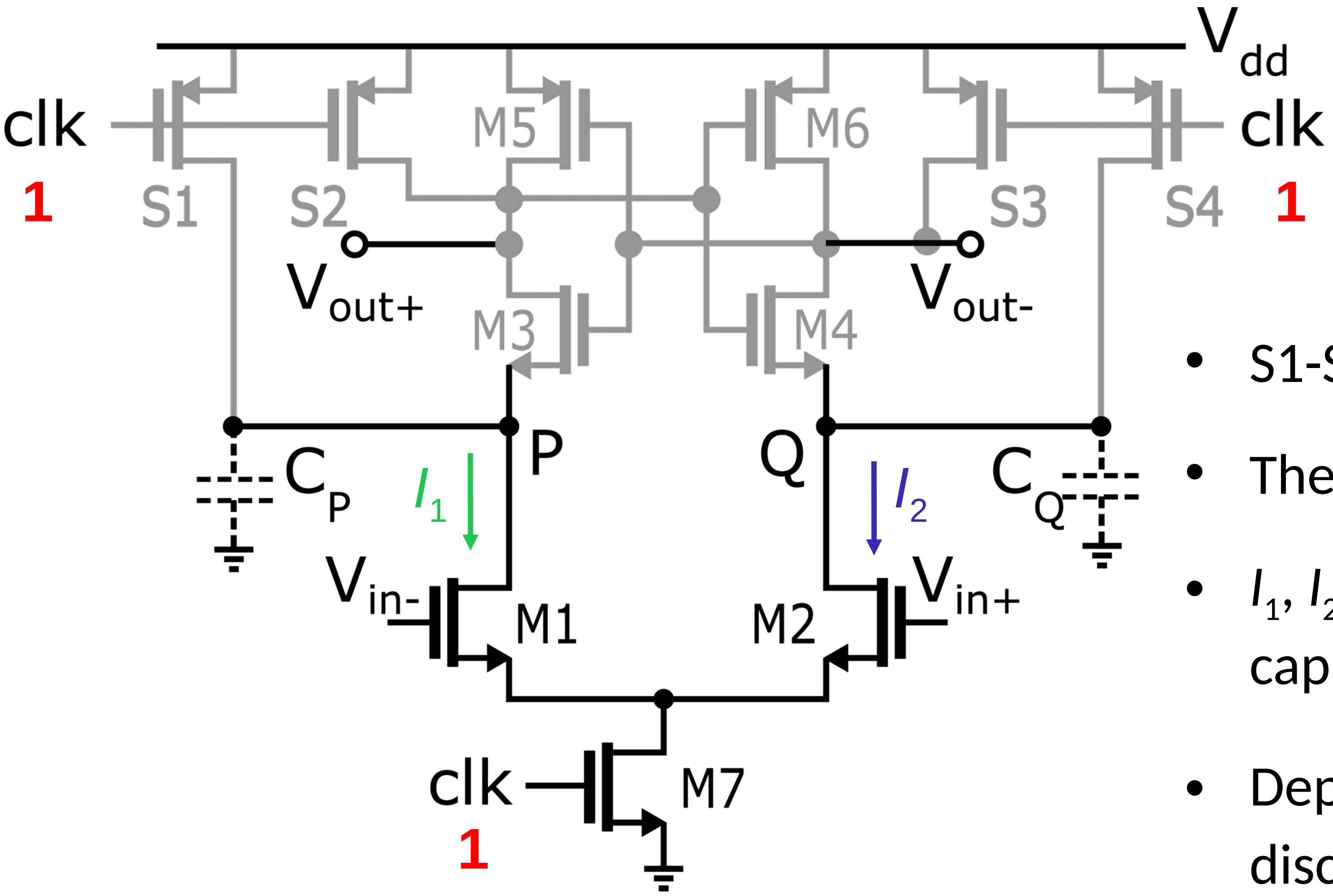
- **Zero input-referred hysteresis:** at each reset phase, the comparator loses 'memory' of the previous cycle state.
- <u>Nevertheless:</u> the comparator will evolve to a full logical state. (Latch: level regeneration)
- Operation in <u>3 phases</u>: (i) **Reset**, (ii) **Amplification**, (iii) **Regeneration**

StrongARM: Reset Phase



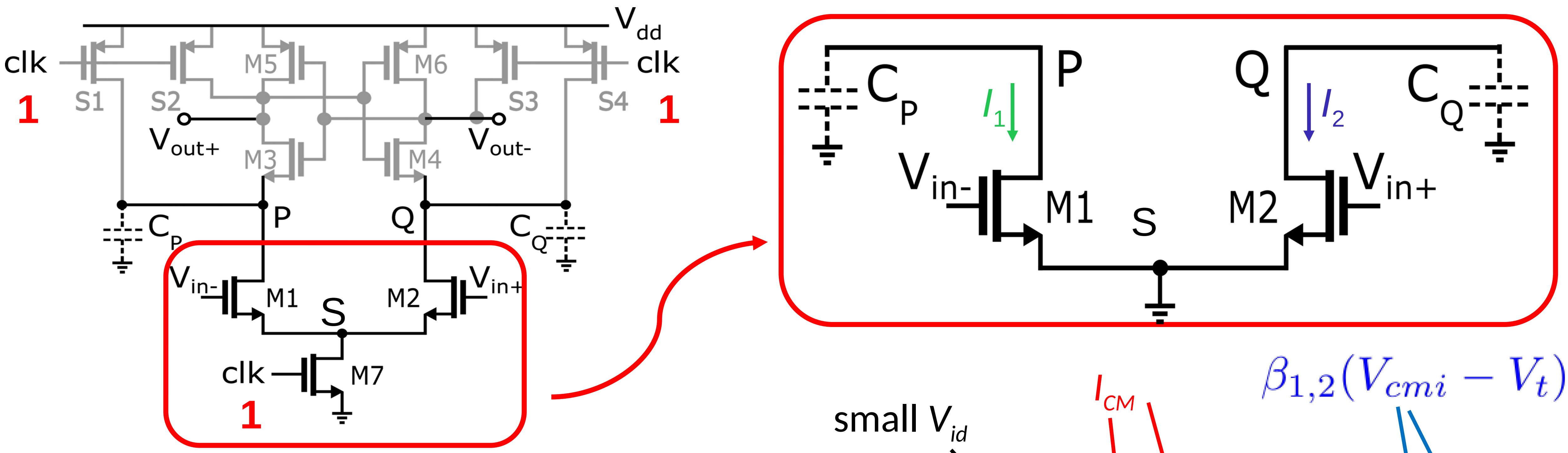
- The input pair devices are off
- Nodes P, Q, V_{out+}, V_{out-} are connected to V_{dd} through S1-S4
- Latch is inactive
- Parassitic C_P and C_Q are precharged to V_{dd}

StrongARM: Amplification Phase



- S1-S4 go off, M7 goes on
- The input pair is on
- I_1, I_2 start discharging the parasitic capacitances C_P, C_Q at nodes P, Q
- Depending on $V_{id}= V_{in+} - V_{in-}$ node P is discharged faster/slower than node Q

StrongARM: Amplification Phase

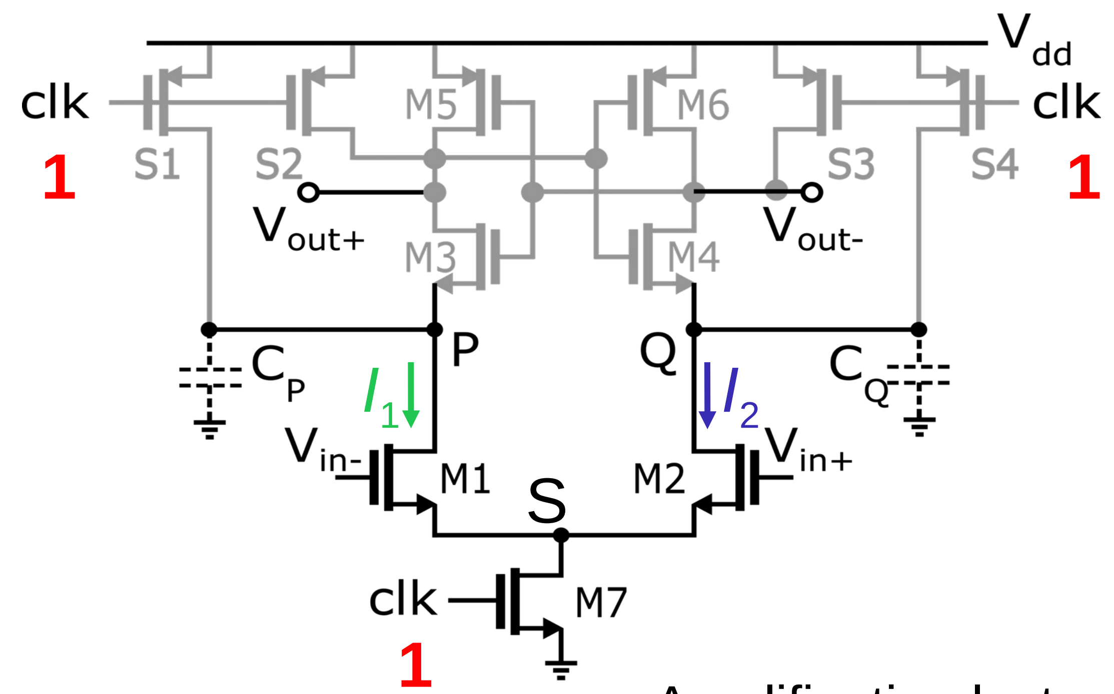


Pseudo-differential pair (when clk=1, M7 connects node S to gnd)

small V_{id} $\quad I_{CM}$ $\quad \beta_{1,2}(V_{cmi} - V_t)$

$$\begin{cases} I_1 = \dfrac{\beta_{1,2}}{2}(V_{in}^{+} - V_t)^2 \approx \dfrac{\beta_{1,2}}{2}(V_{cmi} - V_t)^2 - g_{m1}\dfrac{V_{id}}{2} \\ I_2 = \dfrac{\beta_{1,2}}{2}(V_{in}^{-} - V_t)^2 \approx \dfrac{\beta_{1,2}}{2}(V_{cmi} - V_t)^2 + g_{m1}\dfrac{V_{id}}{2} \end{cases}$$

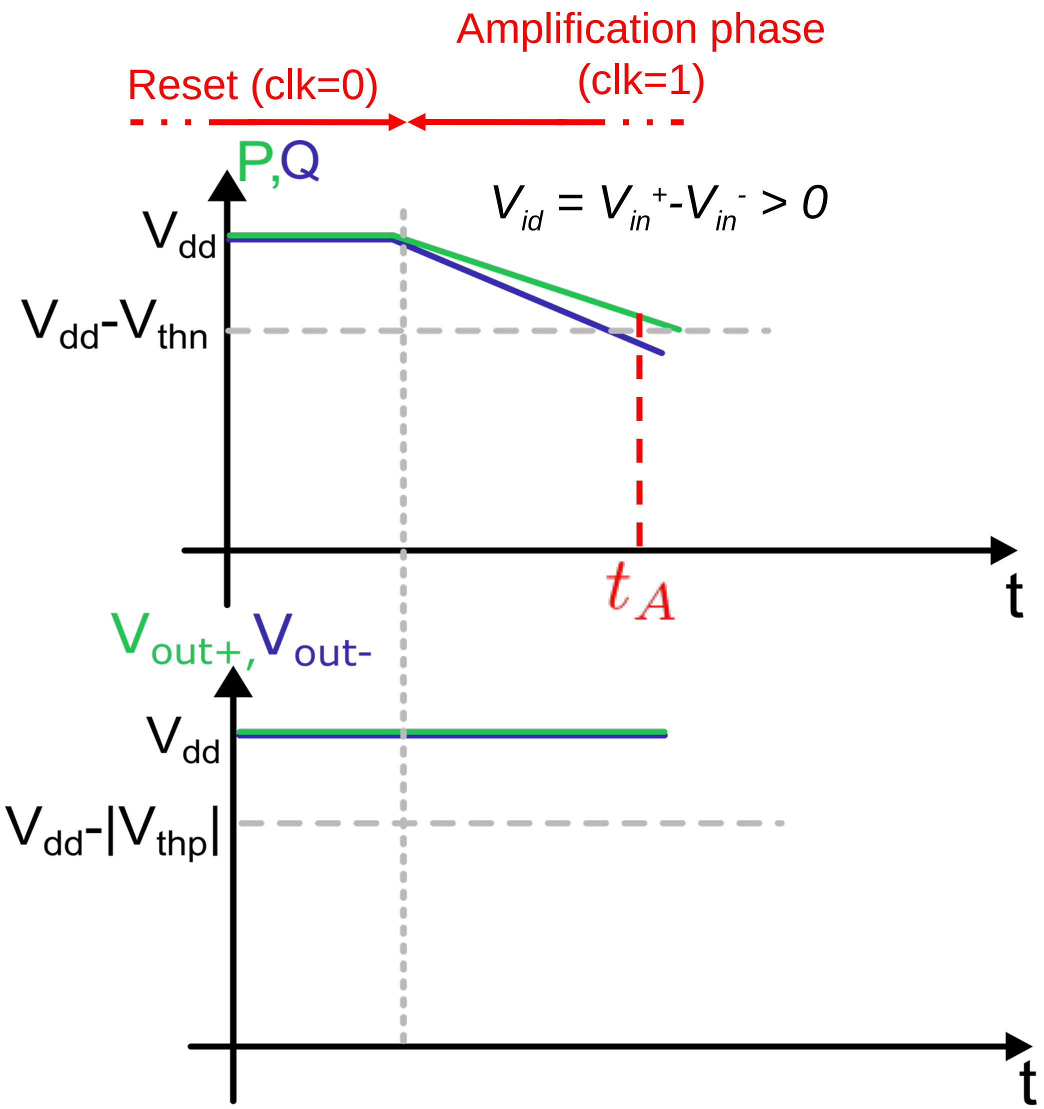
StrongARM: Amplification Phase



$$\begin{cases} \dfrac{dV_P}{dt} = -\dfrac{I_1}{C_P} \\ \dfrac{dV_Q}{dt} = -\dfrac{I_2}{C_P} \end{cases}$$

Amplification lasts appromidatively until $(V_P+V_Q)/2$ reaches V_{dd}-V_{thn}

$$t_A \approx \frac{C_{P,Q} V_{thn}}{I_{CM}}$$



StrongARM: Amplification Phase

$$t_A \approx \frac{C_{P,Q} V_{thn}}{\boxed{I_{CM}}}$$

t_A is also dependent on input common mode, slower for lower V_{cmi}

gain A

$$V_P - V_Q = \boxed{\frac{g_{m1}}{C_{P,Q}} t_A} V_{id}$$

Gain A is not precise, and it is dependent on input common mode:

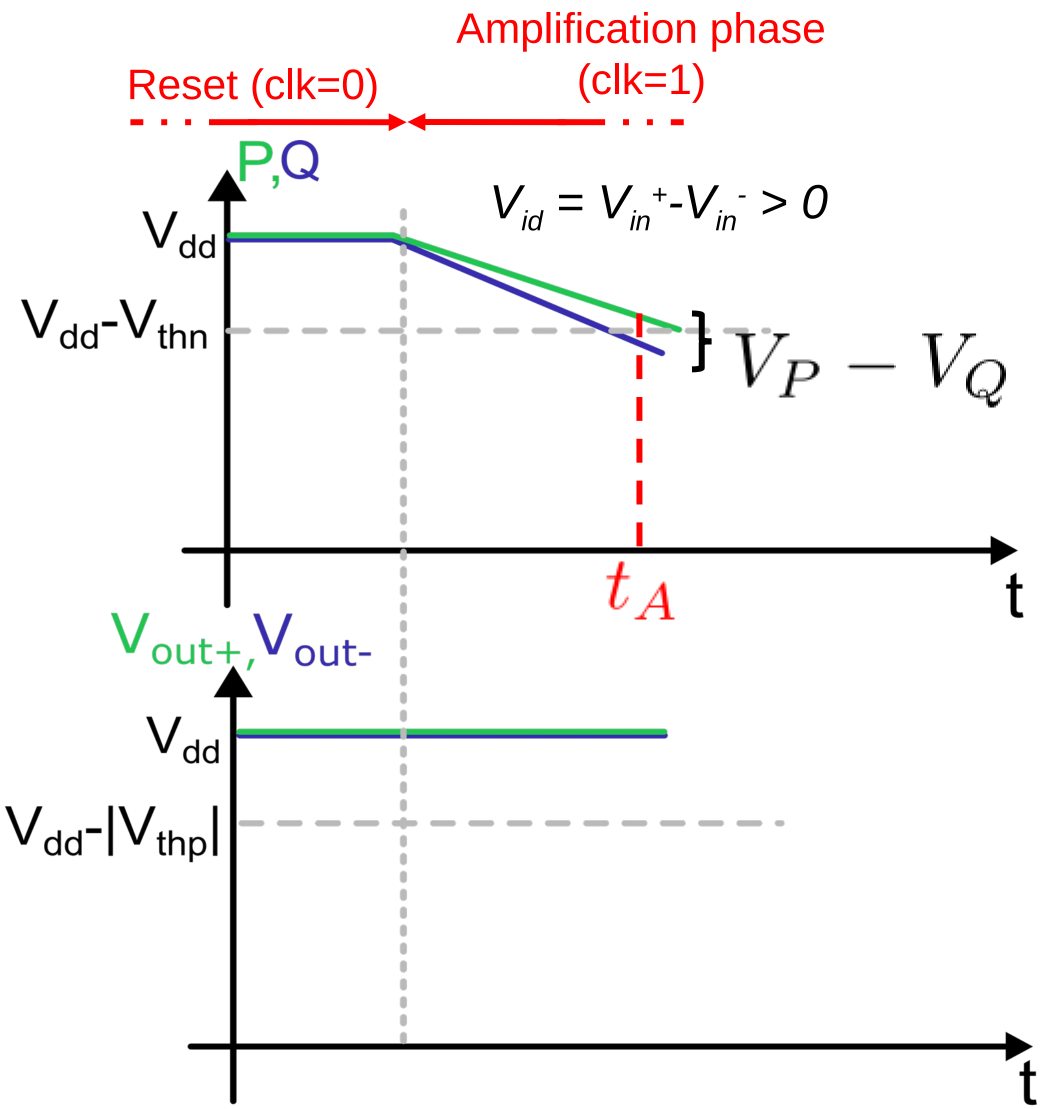
$$A = g_{m1} \cdot \frac{t_A}{C_{P,Q}} = \frac{2I_{CM}}{V_{cmi} - V_t} \cdot \frac{V_{thn}}{I_{CM}} = \frac{2V_{thn}}{V_{cmi} - V_t}$$

Is the condition A>1 always guaranteed?

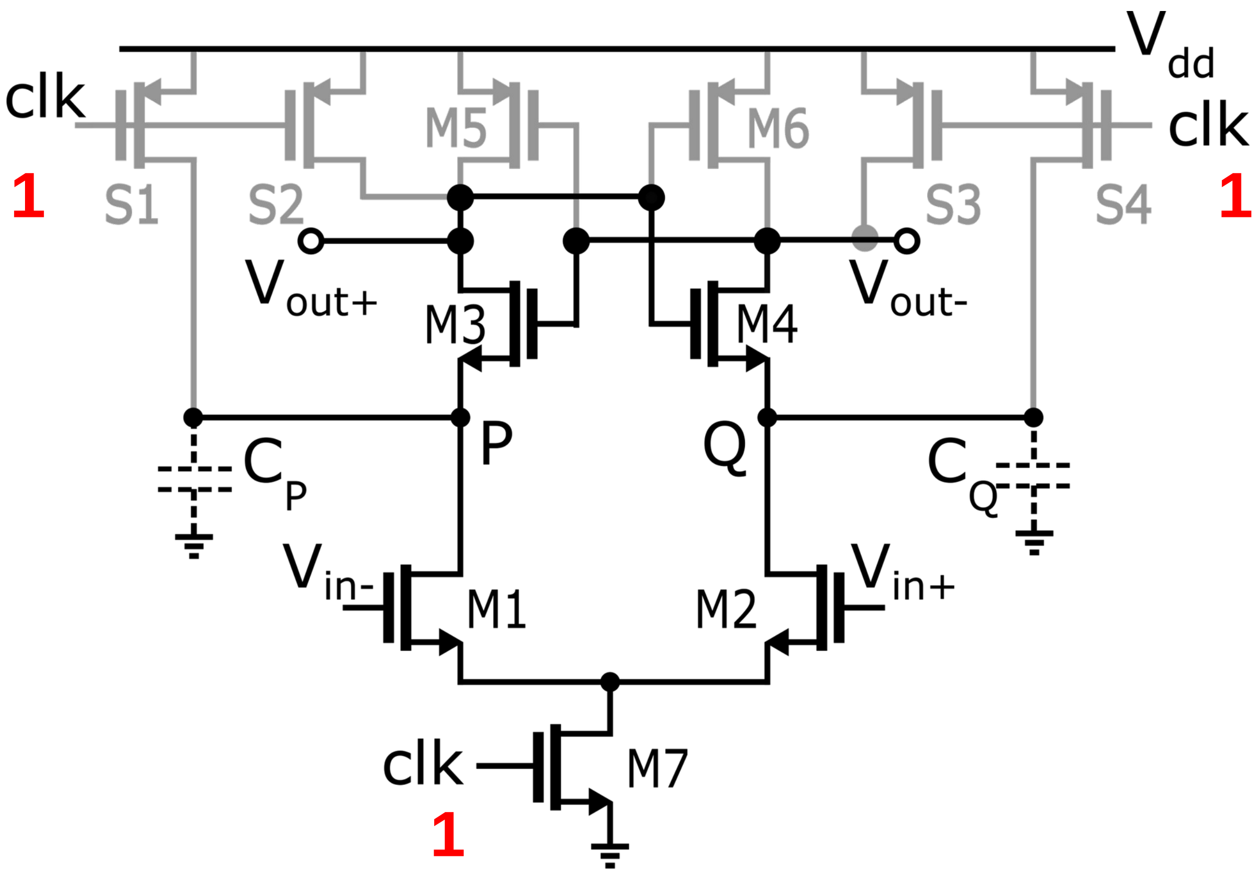
Numerical example: V_{cmi}=1.7 V, V_t = 0.5 V (input pair)

V_{thn} = 0.6 V (cross coupled NMOS, beneficial body effect)

→ A = 1. For V_{cmi} > 1.7 V, there is no amplification!



StrongARM: Amplification Phase, continued

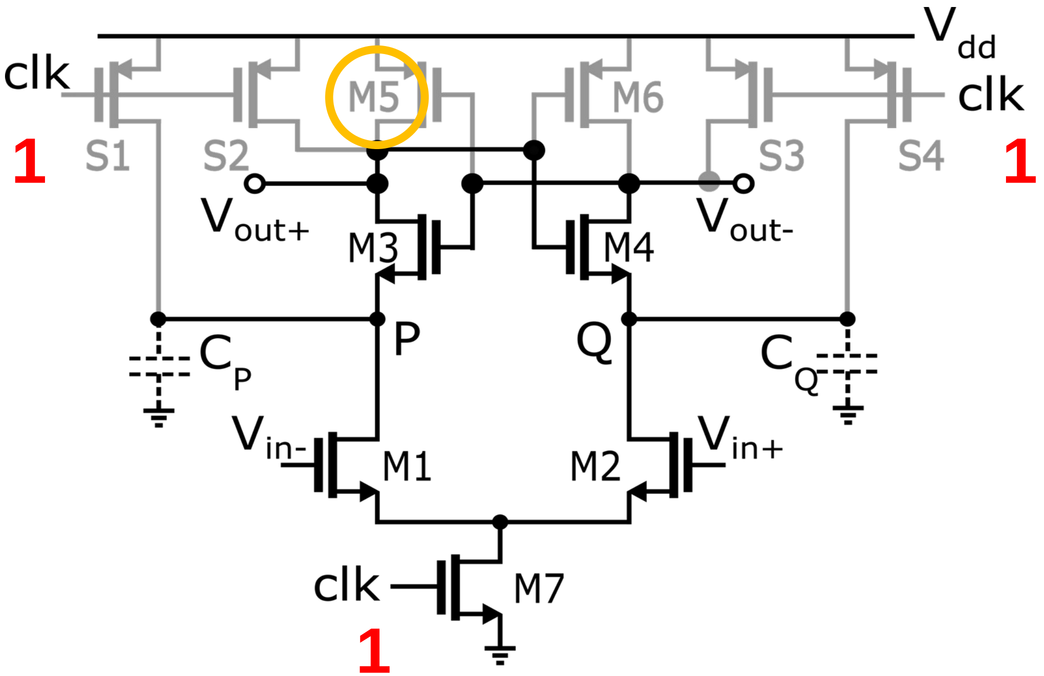


- When voltages at nodes P,Q go lower than V_{dd}-V_{thn}, M3-M4 turn on
- Once on, M3-M4 can be regarded as batteries (~V_{thn}):

$$\begin{cases} V_{out}^{+} \approx V_Q + V_{thn} \\ V_{out}^{-} \approx V_P + V_{thn} \end{cases}$$

- Nodes P,Q keep discharging and V_{out+}, V_{out-} start discharging differently according to the unbalance of P and Q

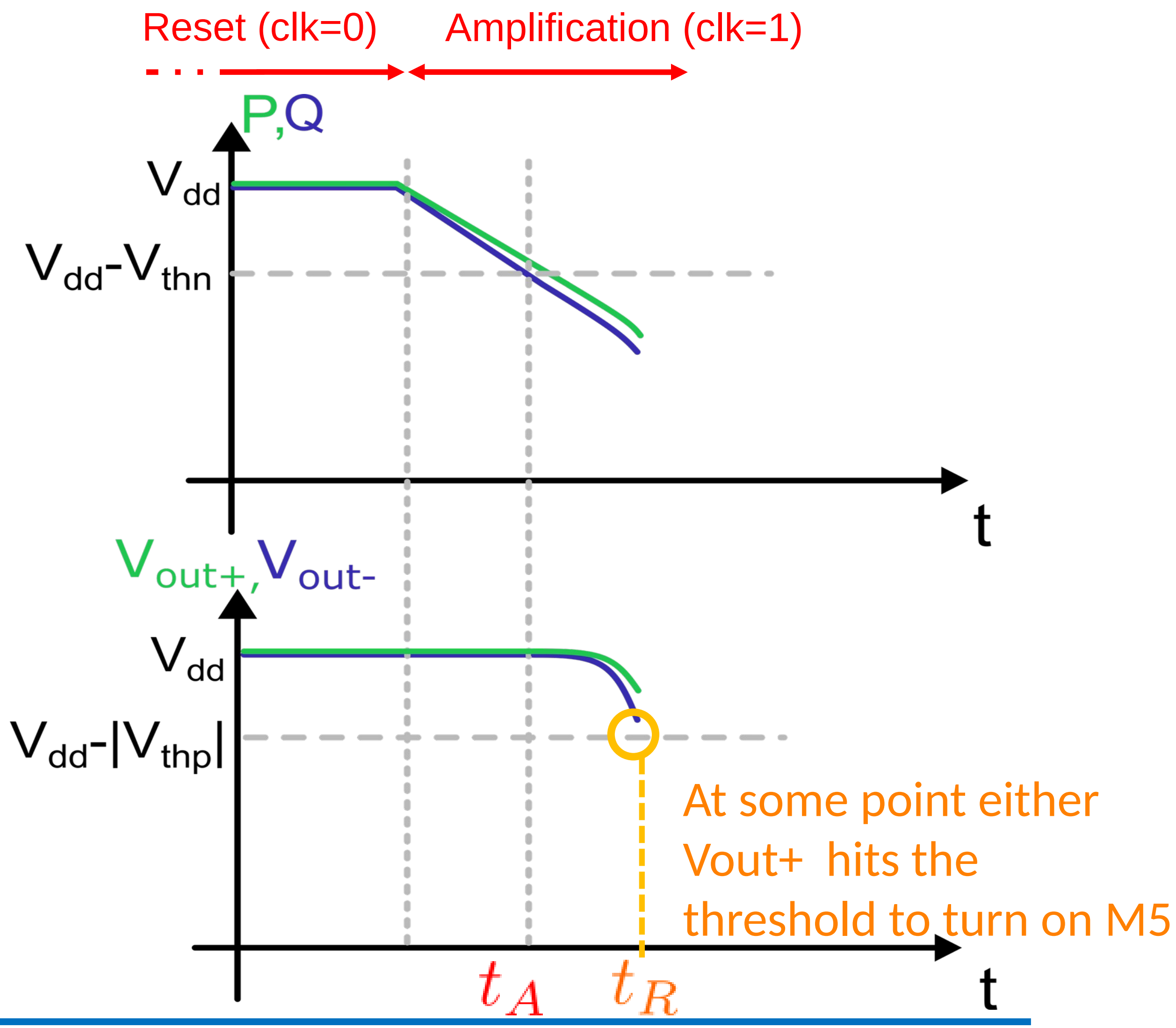
StrongARM: Amplification Phase, continued



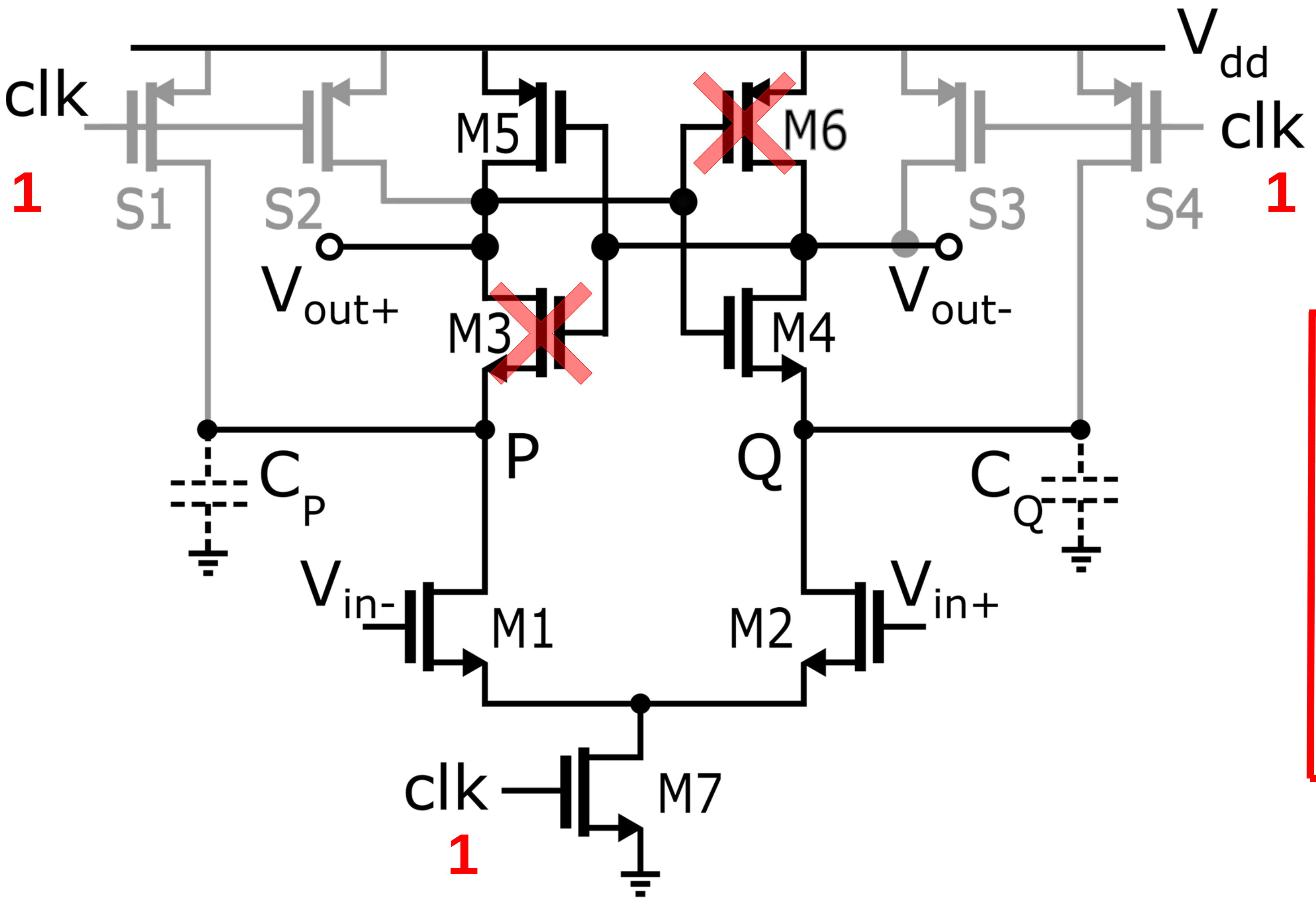
$$V_{id} = V_{in}^{+} - V_{in}^{-} > 0$$

$$V_P - V_Q = AV_{id} > 0$$

$$V_{out}^{+} - V_{out}^{-} \approx AV_{id} > 0$$



StrongARM: Regeneration Phase

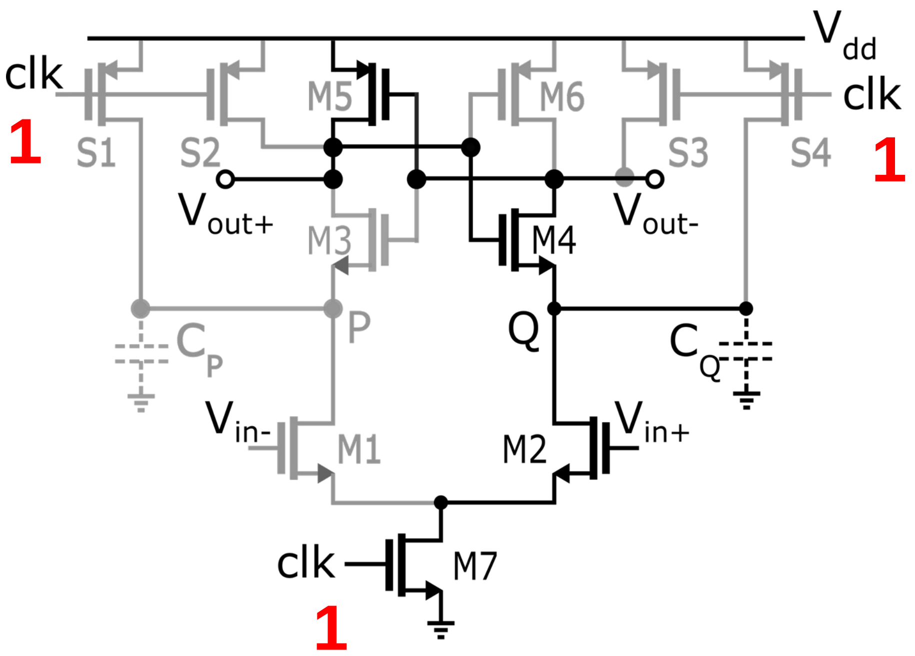


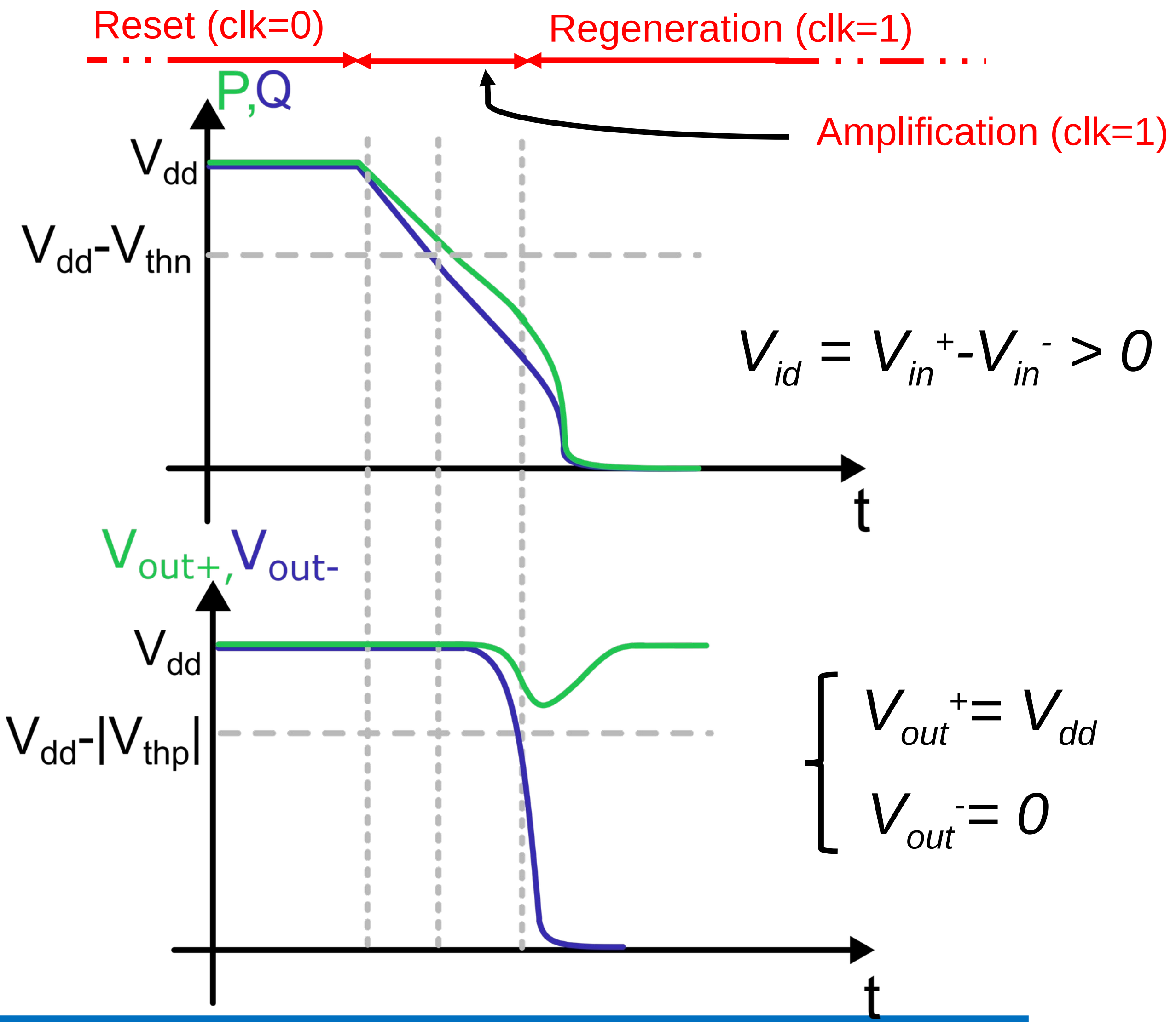
- When V_{out}^{+} or V_{out}^{-} goes lower than $V_{dd}-|V_{thp}|$, one between M5 and M6 turns on:

1) If Vout- hits first, M5 turns on, and Vout+ is pulled towards Vdd (M6 is off)
2) M4 is more "conductive" allowing Vout- to lower. M2 evuentually enters linear region.
3) M3 progressively turns off due to lowering Vout-. Hence it cuts the M5-M3 DC path

Positive feedback loop (regenerative)

StrongARM: Regeneration Phase

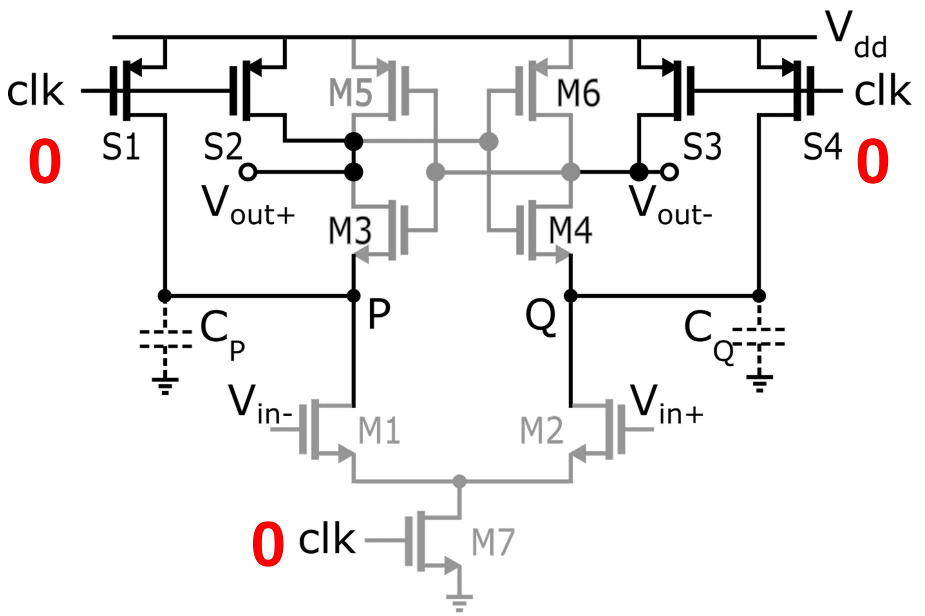


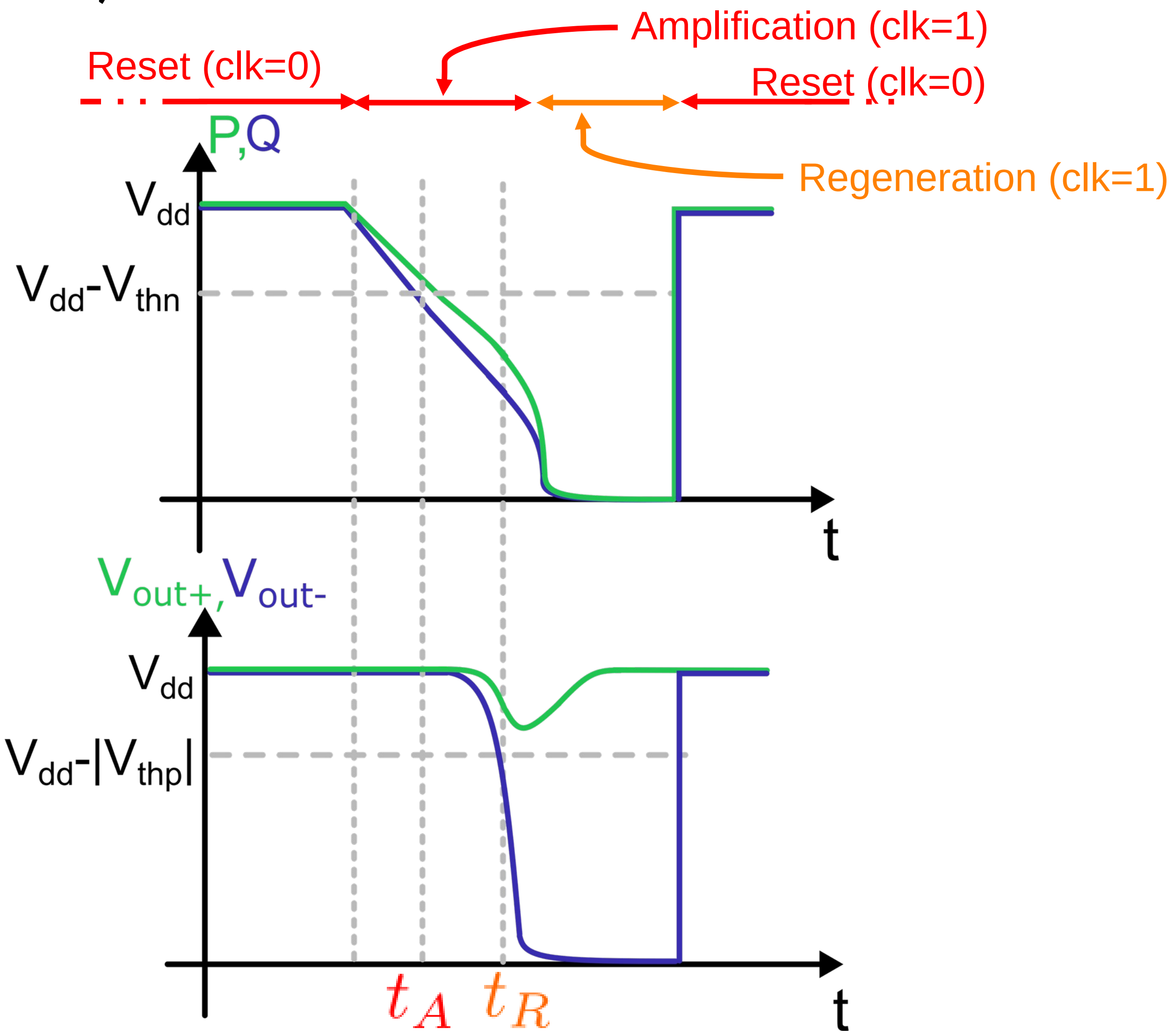


Regeneration Phase: Vout- is allowed to reach gnd

Once the regeneration is finished, **no static power consumption** is present
(M3 cuts off the current path from V_{dd} to ground)

StrongARM: (Next) Reset Phase

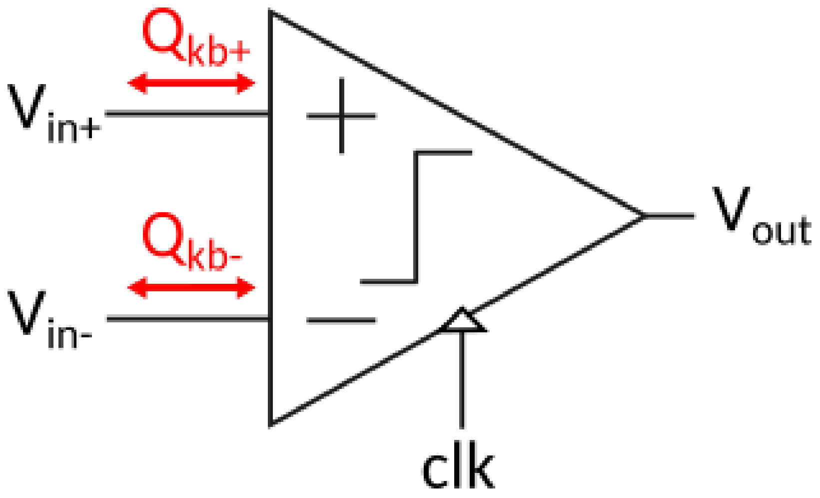




- S1-S4 recharge node P, Q, V_{out}^{+}, V_{out}^{-} to V_{dd}
- Need of a second latch to store the result of the comparison during the reset phase

StrongARM: Kick back effect

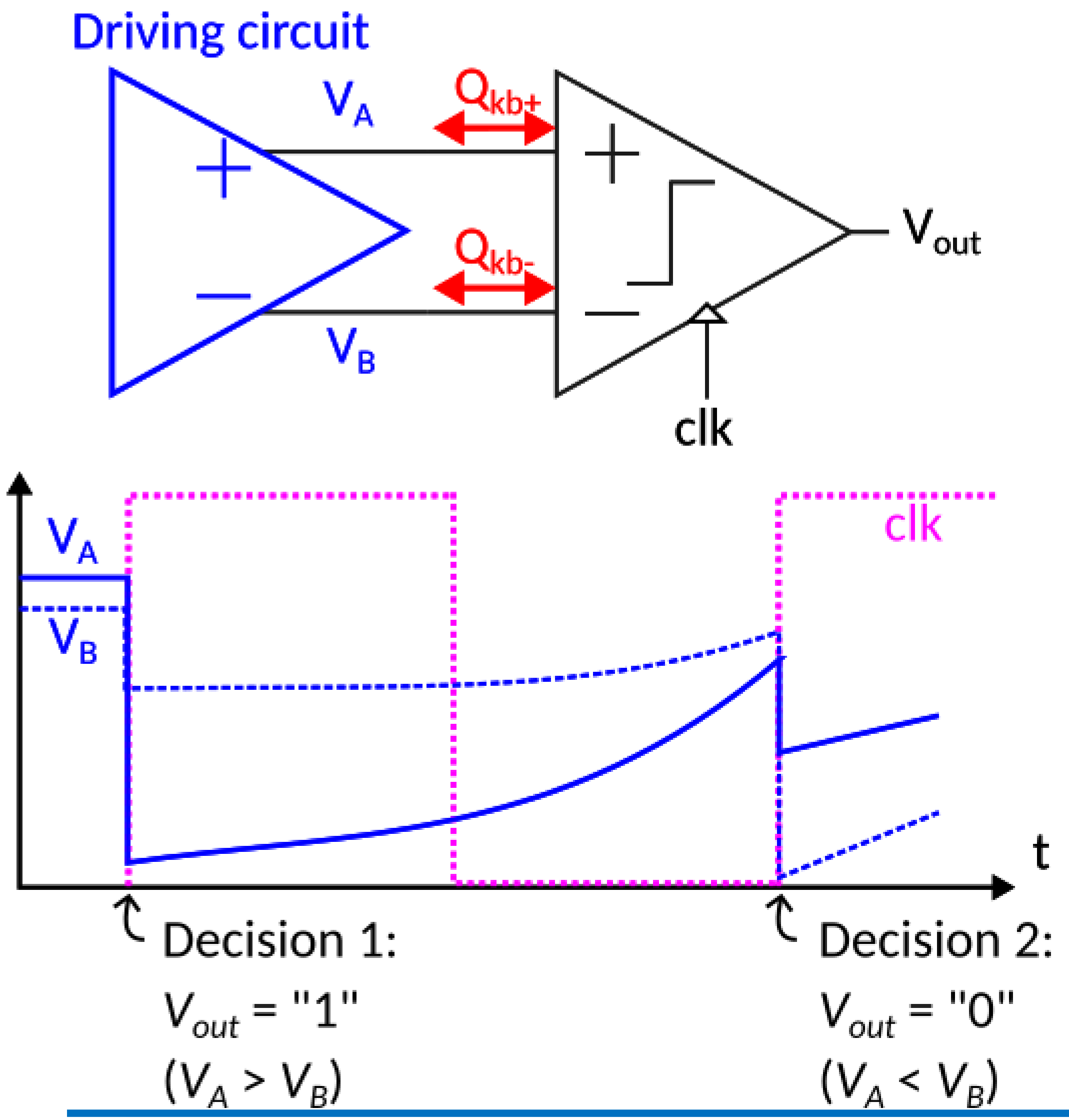
- The kick back effect is evident at the comparator inputs Vin- and Vin+
- It implies a sudden demand of charge seen at those input terminals due to the **sharp transition of the internal voltages**, similar to the charge injection effects of a switch turn-on and turn-off
- For each comparison cycle, input pair devices (M1, M2) are first turned on, and the regenerative action of the latch bring them again to the off state
- Charge demand is different from port Vin- and port Vin+: it has a differential-mode component (Qkbd) and a common-mode component (Qkbc)
- Qkbd depends on Vid (input differential voltage)



$$Q_{kbd} = Q_{kb+} - Q_{kb-}$$

$$Q_{kbc} = \frac{Q_{kb+} + Q_{kb-}}{2}$$

StrongARM: Kick back effect



1. Suppose a “weak” driving circuit: (Typically an OTA with high impedance output nodes, cap-loaded, or a compensated 2-stage OTA)

2. Suppose the case of a constant VA > VB

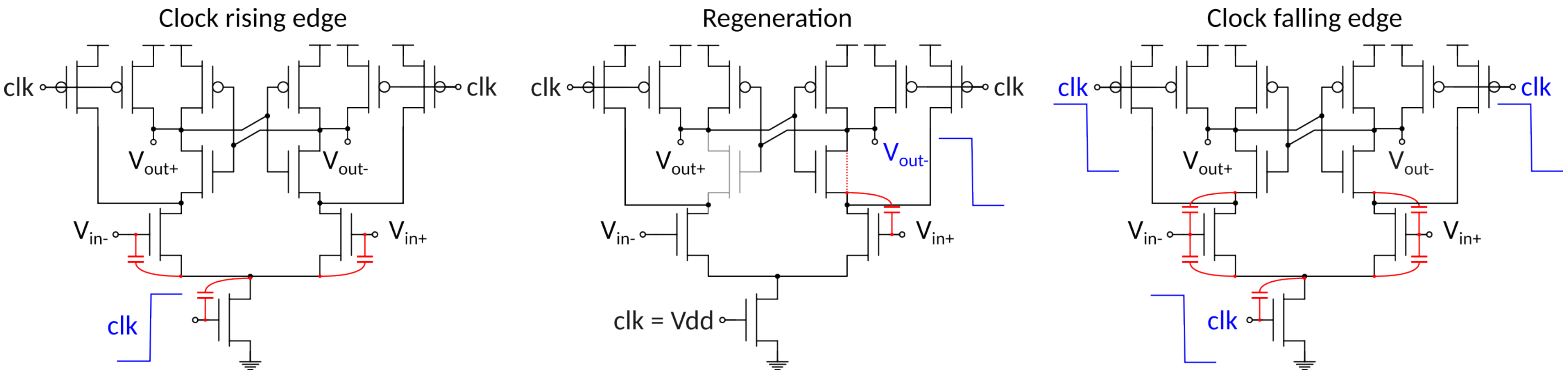
The first decision is correct (Vout=”1”), if VA and VB would be kept constant all the following decisions should be “1”

However: VA and VB are upset by a different amount due to Qkbd

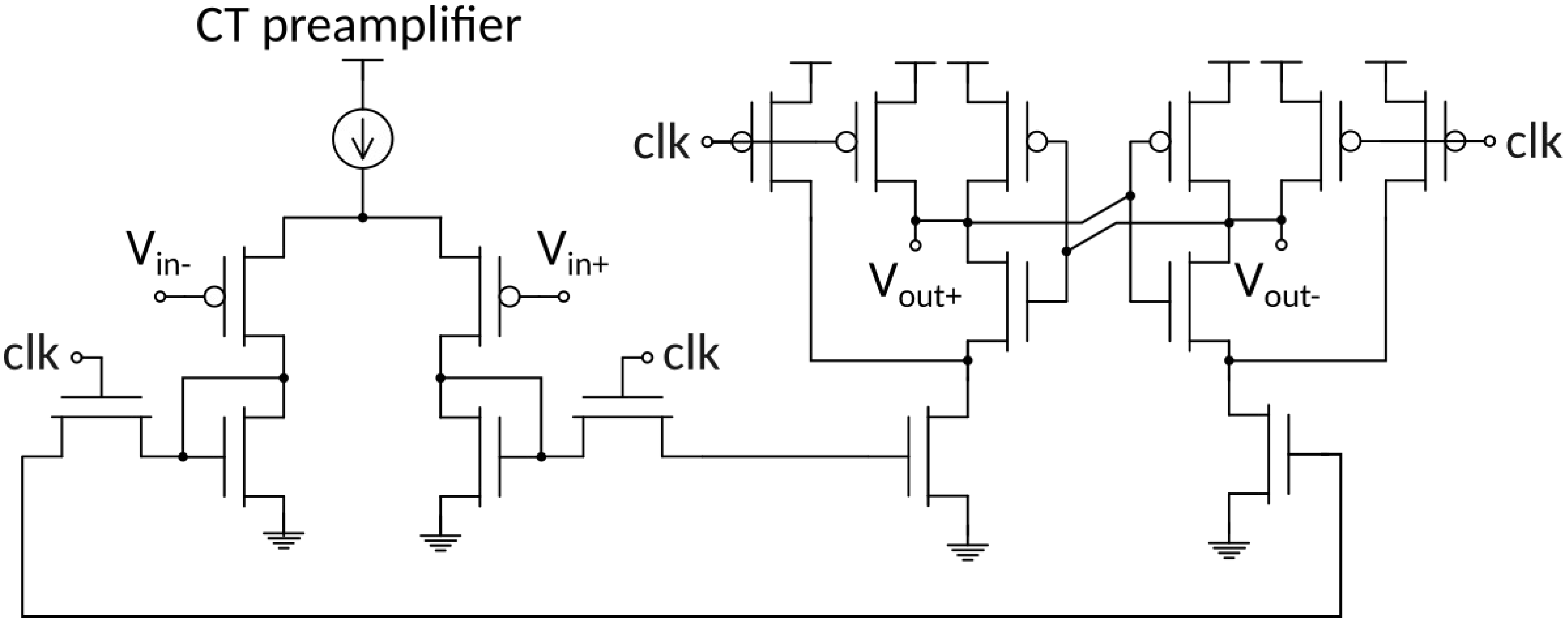
The system is slow to recover, hence when the second clk rising edge occurs VA < VB: the comparator now provides a wrong decision

The result of the second decision has been influenced by the result of the previous decision: this is similar to an hysteretic effect (undesired in this case)

StrongARM: Kick back effect



StrongARM: Kick back effect, possible solution



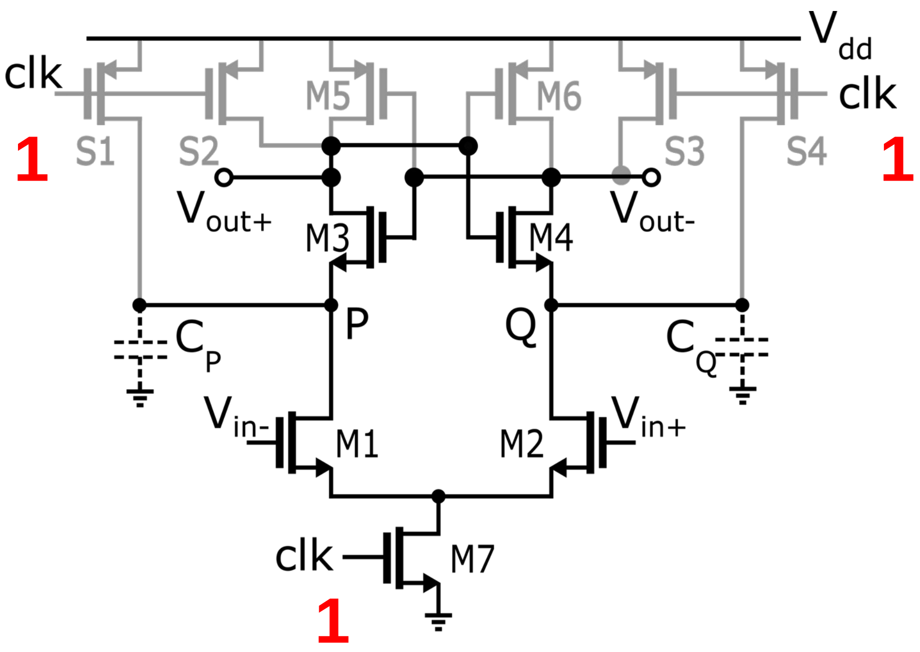
Use of a preamp-like structure:

✓Greatly reduces signal swing coupled to the input pair.

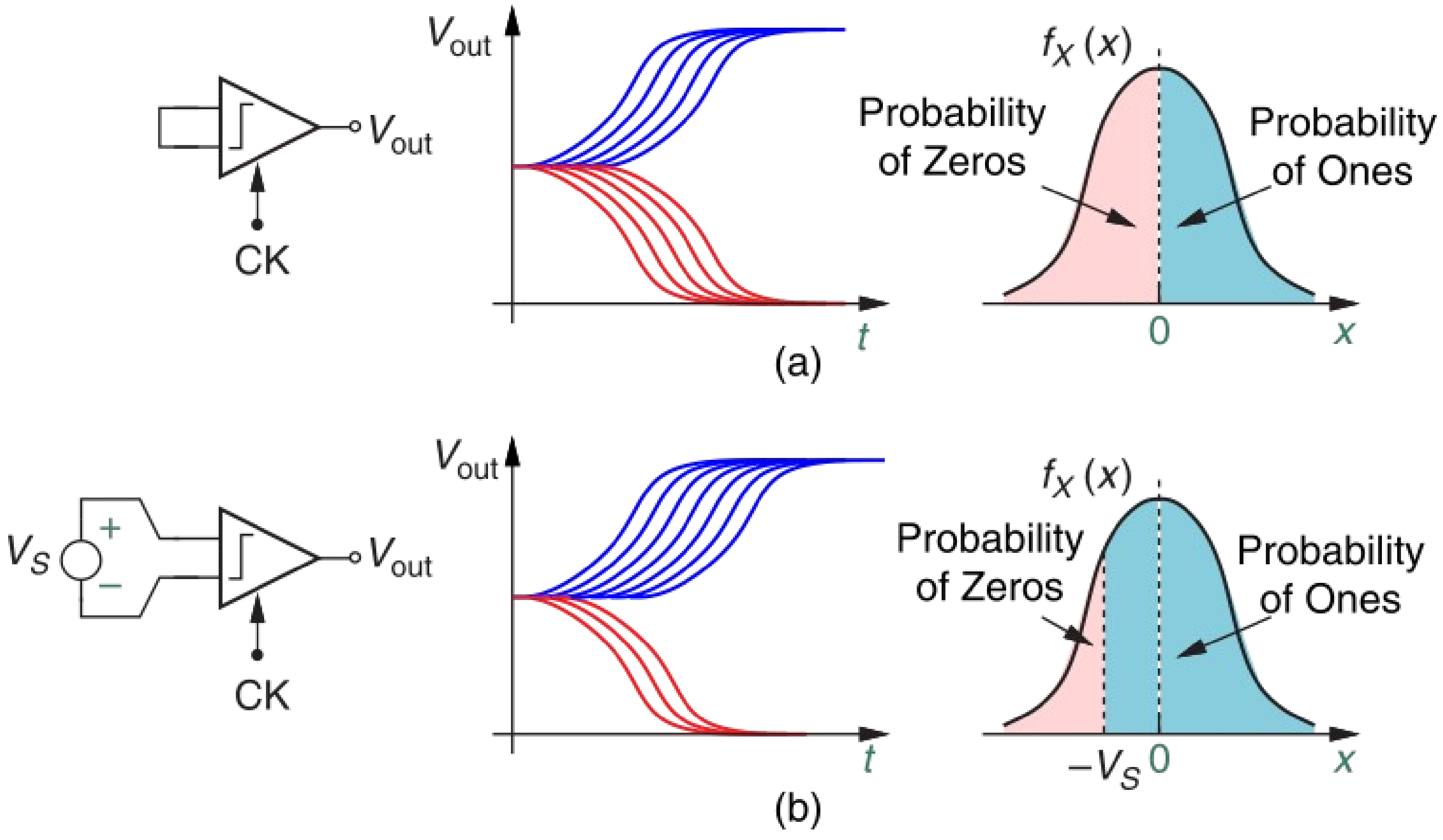
✘ Implies static power consumption

StrongARM: input referred noise characterization

- For such **strongly non-linear circuit** transfer function is undefined, hence there exist no straight-forward “referring to input” procedure
- Most of the noise that may affect the decision is produced **before the regeneration phase** (i.e. during the amplification phase)
- The amplification phase is governed by the input pair (**M1, M2**). Once the cross coupled M3 and M4 turn on (during the last part of the amplification phase) they also provide a small contribution to total accumulated noise charge on CP, CQ.
- The gain during the amplification phase is “dynamic”: it depends on a time interval (t_A, t_R). Analytical expressions can be found but are complex



StrongARM: input referred noise characterization



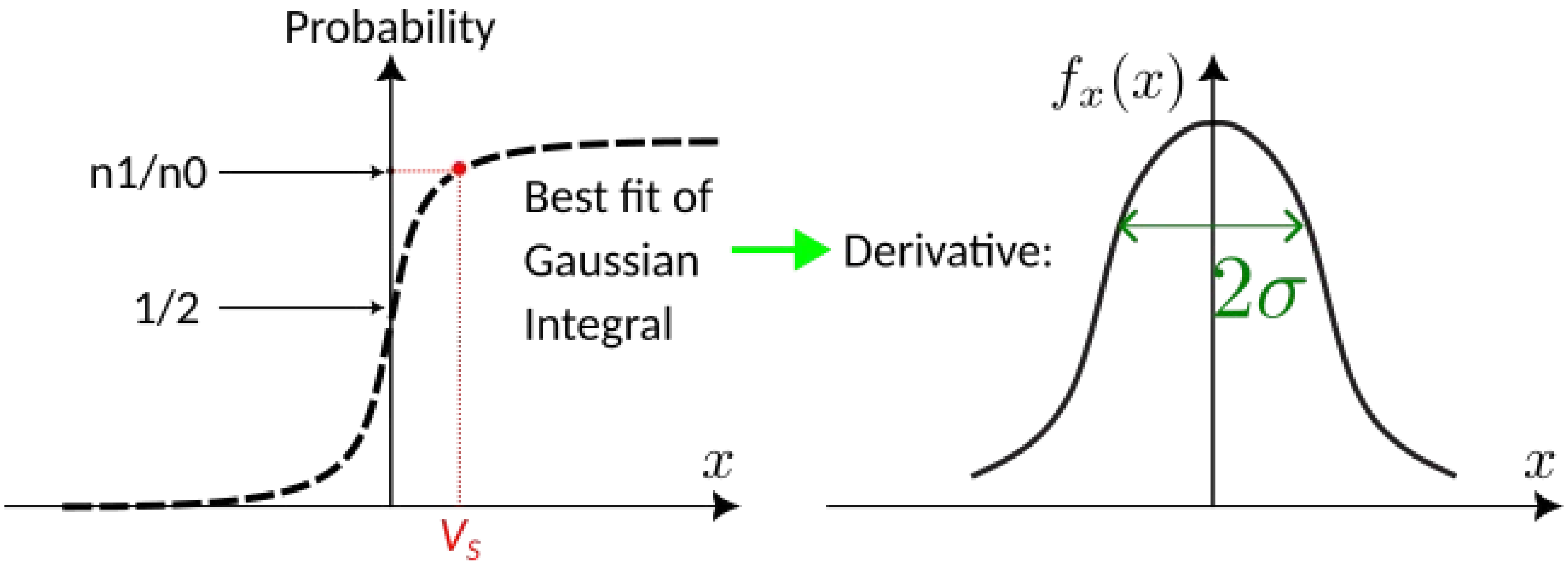
The goal is to find the sigma of a supposed normal distribution (Transient Noise simulations)

If inputs are at the same potential there is equal probability of having “0s” (n0) and “1s” (n1)

Differential input slightly skewed to have different n0 and n1 counts. In the example n1>n0

$$\frac{n_0}{n_1} = \frac{\int_{-\infty}^{V_S} f_x(x)\,dx}{1 - \int_{-\infty}^{V_S} f_x(x)\,dx}$$

StrongARM: input referred noise characterization



Eventually try a couple of VS values to provide more points for best fit algorithm

Note: VS should be chosen to be reasonably distant from probability = 1, 0 and ½