# Introducing myself

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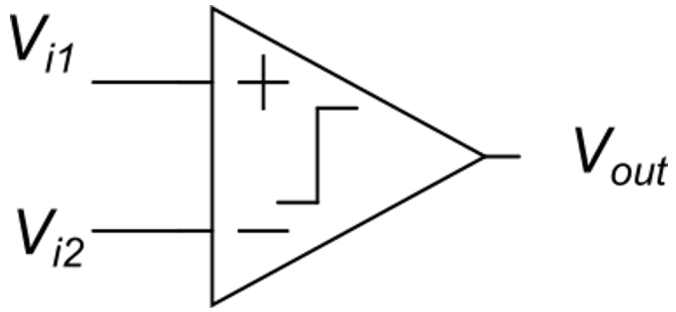
Teaching during this year:
~20 hours

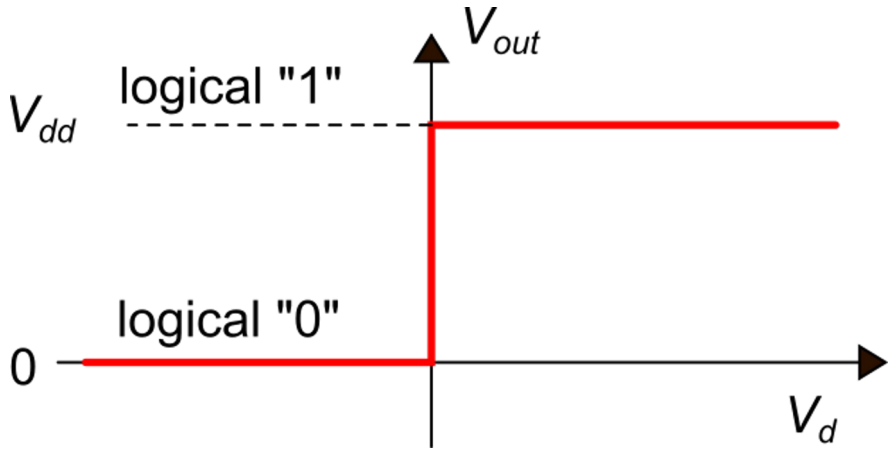
Topics:
Comparators, ADCs, DACs, Integrated Filters

New here!
My hope is to maintain the high standards of this teaching

# Comparators




Symbol (differential input kind)




**1)** **<u>Detect</u>** the sign of a differential analog signal.
Sometimes S/E input case:
$V_{i2}$ is derived from an internal voltage reference

$$V_d = V_{i1} - V_{i2}$$

**2)** **<u>Codify</u>** the outcome in digital domain

$$V_{out} = \begin{cases} \text{"0" if } V_d \leq 0 \\ \text{"1" if } V_d > 0 \end{cases}$$

# Applications

**Building block in:**

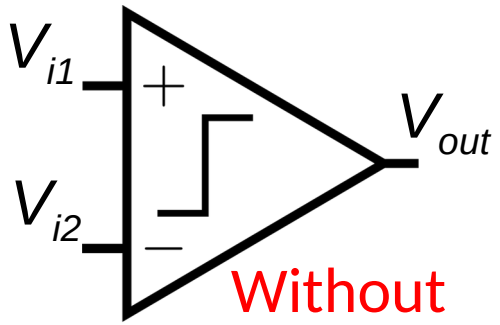
- Mixed-signal front-ends:
  sensors AFEs;
  signal-processing (ADCs, DACs)
- Signal-and-function generation
- Digital communication (symbol recognition in a noisy channel)
- Artificial neural networks (perceptron: linear binary classification)

# Continuous-time vs dynamic comparator

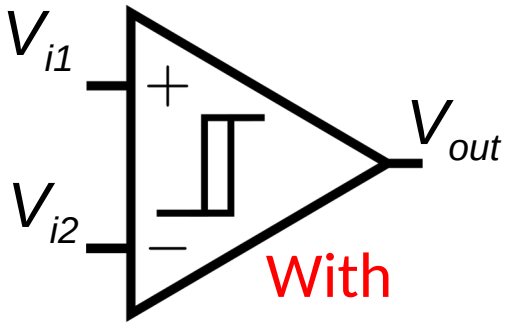
**Continuous-time (CT) comparator:**

Used in level-crossing event-driven circuits

- ✘ Static power consumption
- • Can be designed in order to embed hystheresis
- ✓ Output always valid




Without hystheresis

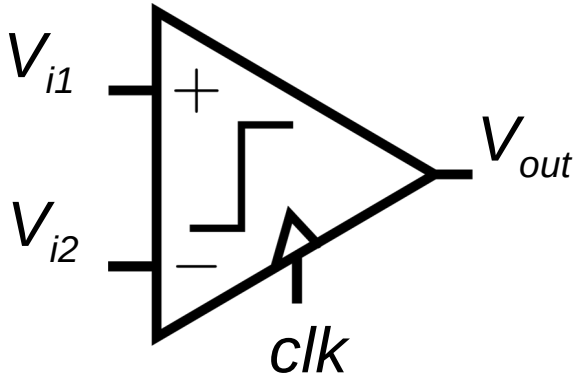



With hystheresis

**Dynamic comparator (or latched comparator):**

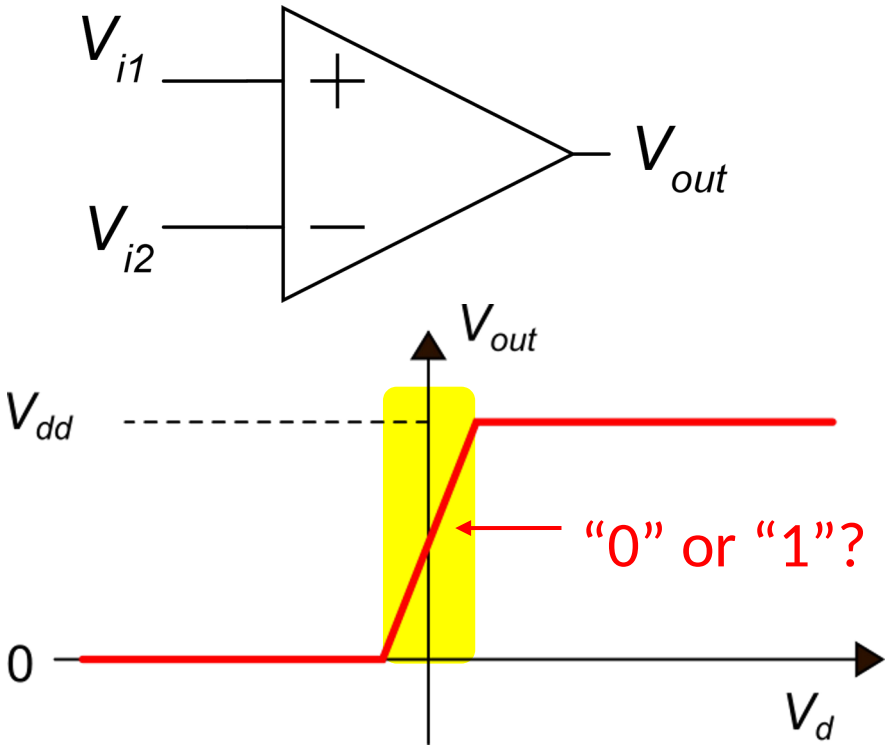
Used in clock-synchronous circuits (as the comparator needs a driving clock signal)

- ✓ No static power consumption (in basic single-stage configuration)
- • No hysteresis
- ✘ Sometimes: output valid only during half clock period



# CT Comparators: amplifier-based implementations

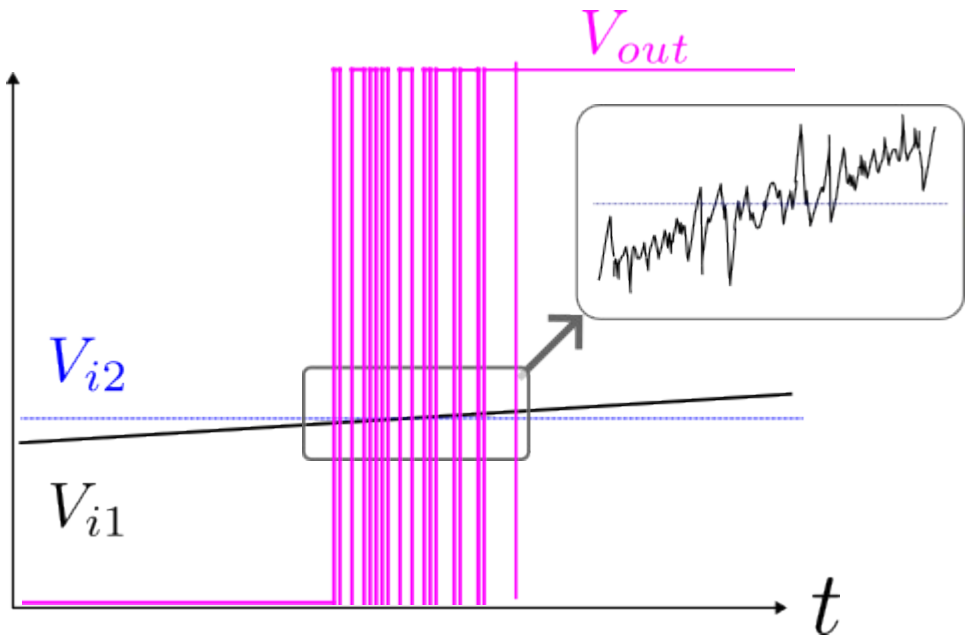
A high-gain amplifier can be used as a comparator:
Op-amp topologies can be used in open loop or even positive feedback:
Speed is prime: no frequency compensation (no stability issues)




- ✘ **Accuracy loss**: a region exists where the logical level is undefined
- ✘ In several applications this may lead to unwanted stable or metastable states (→)

# CT Comparators: amplifier-based implementations

Transient behaviour:
(RTI noise on Vi1 port)

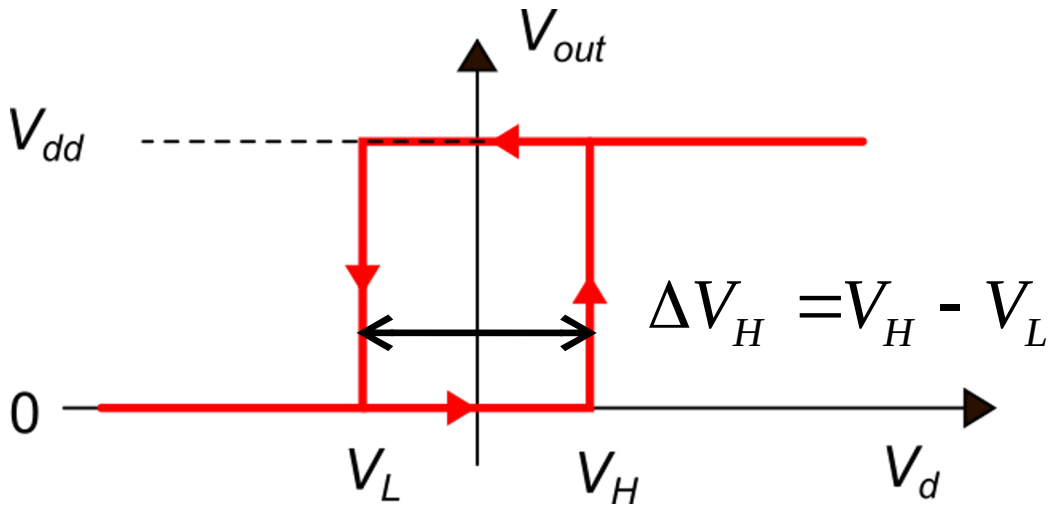


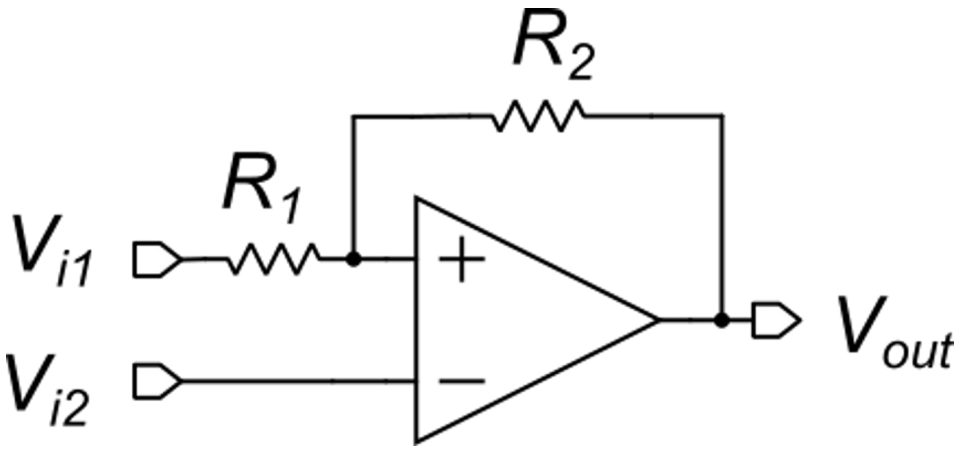

**Glitches for slow varying input**
common issue to all CT comparators without hysteresis

If level crossing is used as trigger in a complex system with feed back: time uncertainty and/or stability issues

If the comparator is interfaced with a synchronous digital FSM: $T_{hold}$, $T_{setup}$ violation (need for synchronizer circuit otherwise data are loss)

# Regenerative comparators: hysteresis




Thanks to the hysteresis, the comparator produces a **valid output** level across the whole input range. Use of positive feedback: **"vertical" edges**.

The hysteresis introduces an **uncertainty band** that reduces the accuracy but helps rejecting noise when the input differential voltage is close to zero.

Possible regenerative comparator: Op-amp-based Schmitt trigger.

**Drawbacks**

- Over-sized solution for integrated cells
- Low impedance on the non-inverting input

# Off-the-shelf devices

TEXAS INSTRUMENTS

TLV9022, TLV9032, TLV9024, TLV9034
SNOSDA3B – JUNE 2020 – REVISED NOVEMBER 2020

**TLV902x and TLV903x High-Precision Dual and Quad Comparators**

- Rail-to-Rail input with fault-tolerance
- 100ns Typ propagation delay

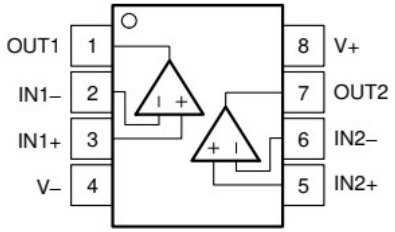
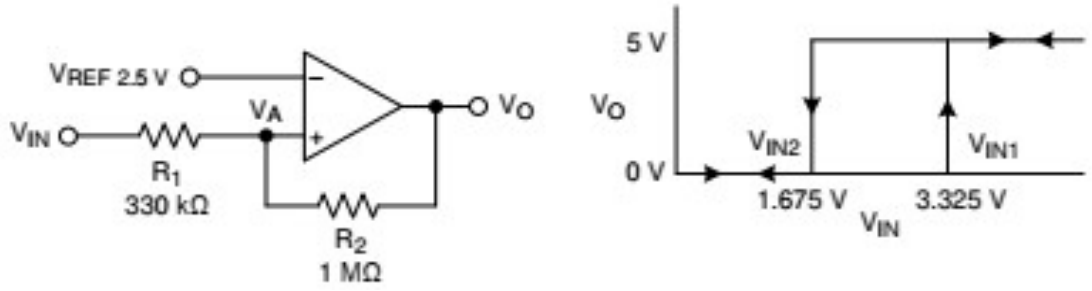



Figure 5-1. D, DGK, PW, DDF Packages
8-Pin SOIC, VSSOP, TSSOP, SOT-23-8
Top View

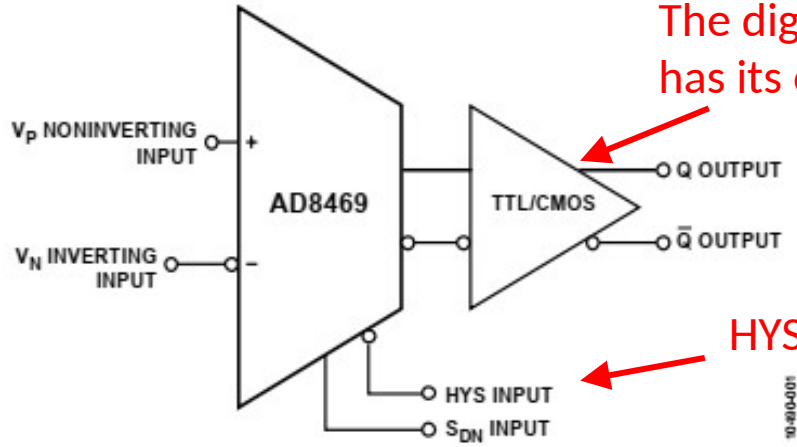
No built-in hysteresis.
Datasheet suggests Schmitt trigger configuration




ANALOG DEVICES

**Fast, Rail-to-Rail, Low Power, 2.5 V to 5.5 V, Single-Supply TTL/CMOS Comparator**

Data Sheet **AD8469**




The digital output has its own $V_{DD}$

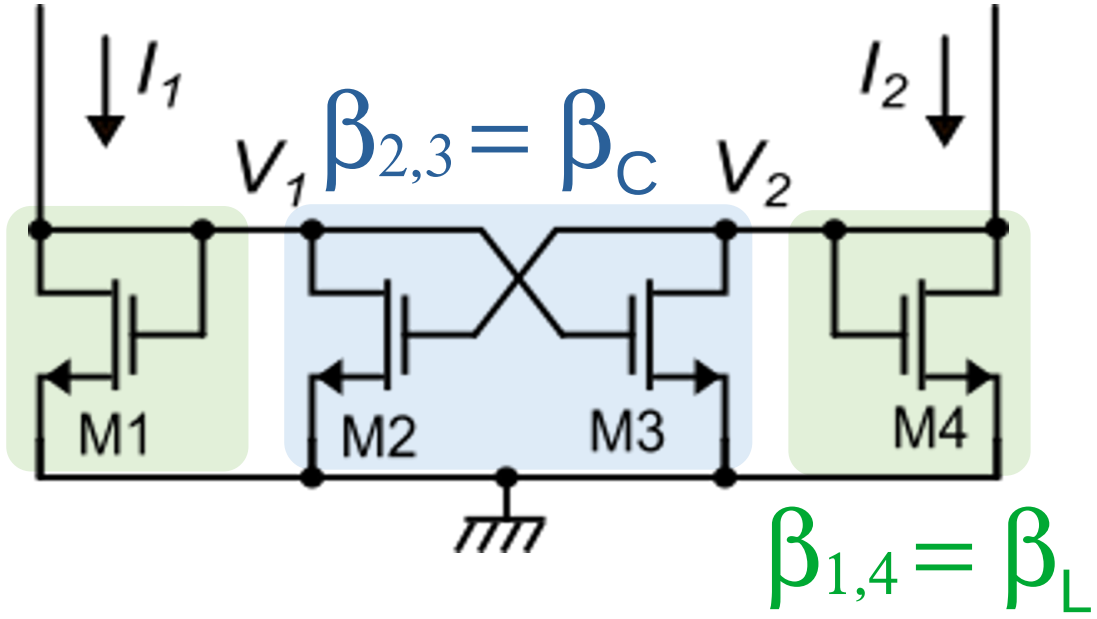
HYS input

*Figure 1.*

Programmable hysteresis from 0 to 160 mV ($\Delta V_H$) depending on current on pin

**Input common-mode voltage: $V_{EE}$ – 0.2 V to $V_{CC}$ + 0.2 V**
**Low glitch TTL-/CMOS-compatible output stage**
**40 ns propagation delay**

# Compact comparator cell for Systems on a Chip




**Four-transistor hysteresis cell**

Inputs: $I_1$, $I_2$

Outputs: $V_1$, $V_2$

*Formed by:*

Cross-coupled MOSFETs M2-M3

Load MOSFETS M1, M4

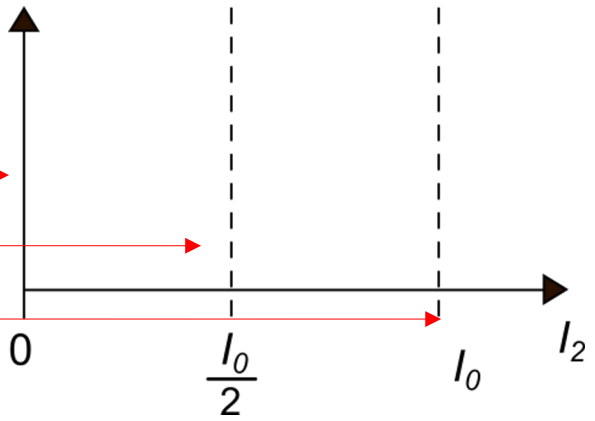
*Constraint*:

$I_1 + I_2 = I_0$ = constant

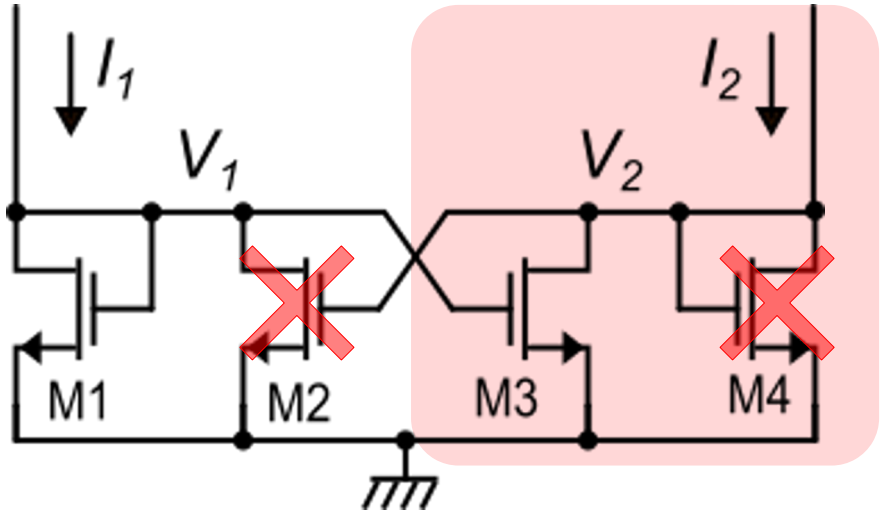
Analysis: $I_2$ in [0, $I_0$]

Notable points:

- $I_2 = 0$; $I_1 = I_0$
- $I_2 = I_1 = I_0/2$
- $I_2 = I_0$; $I_1 = 0$



# Analysis of the four-transistor cell: starting point




Let us start from: $I_2$=0 ($I_1$=$I_0$)

$$I_2 = I_{D3} + I_{D4} = 0$$

since: $I_{D3}, I_{D4} \geq 0 \qquad I_{D3} = I_{D4} = 0$

Considering M4 and M2:

$$V_{GS4} \leq V_t \qquad V_{GS2} = V_{GS4} \qquad I_{D2} = 0$$

Then it is M1 that carries all current $I_1$:

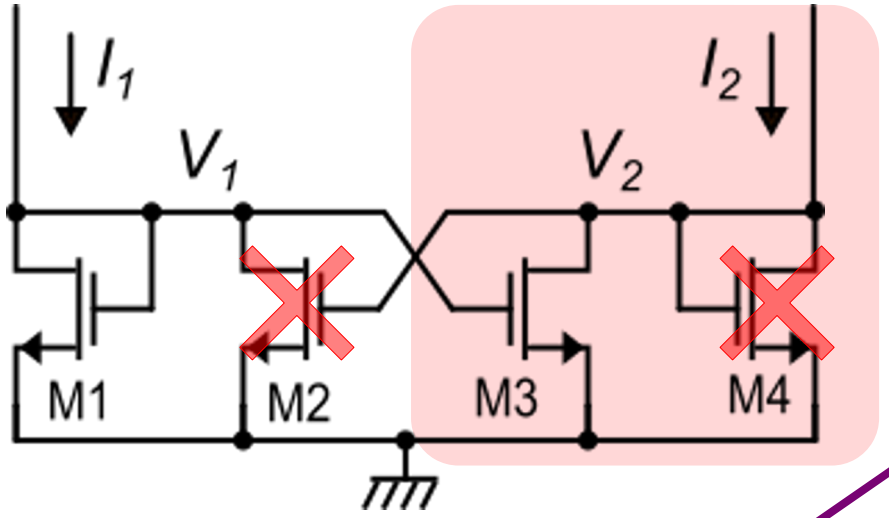
$$V_{GS3} = V_{GS1} \geq V_t \quad \text{(M3 is on)}$$

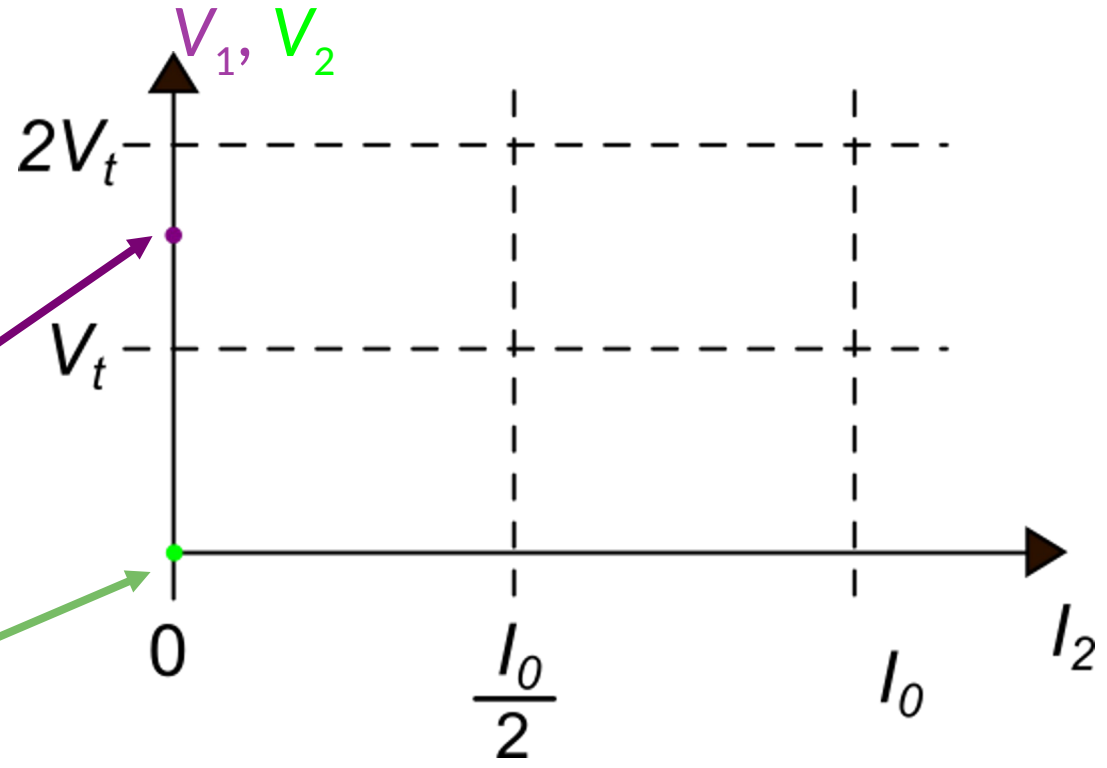
$$I_{D3} = 0$$

$$V_{DS3} = V_2 = 0$$

$$V_1 = V_{GS1} = V_t + \sqrt{\frac{2I_1}{\beta_L}} = V_t + \sqrt{\frac{2I_0}{\beta_L}}$$

# Analysis of the four-transistor cell: starting point



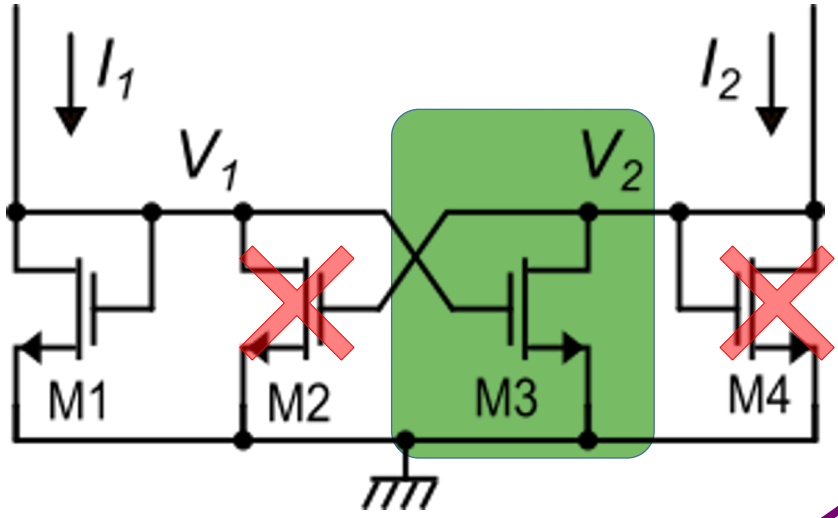

$$V_1(0) = V_t + \sqrt{\frac{2I_0}{\beta_L}} \qquad V_2(0) = 0$$

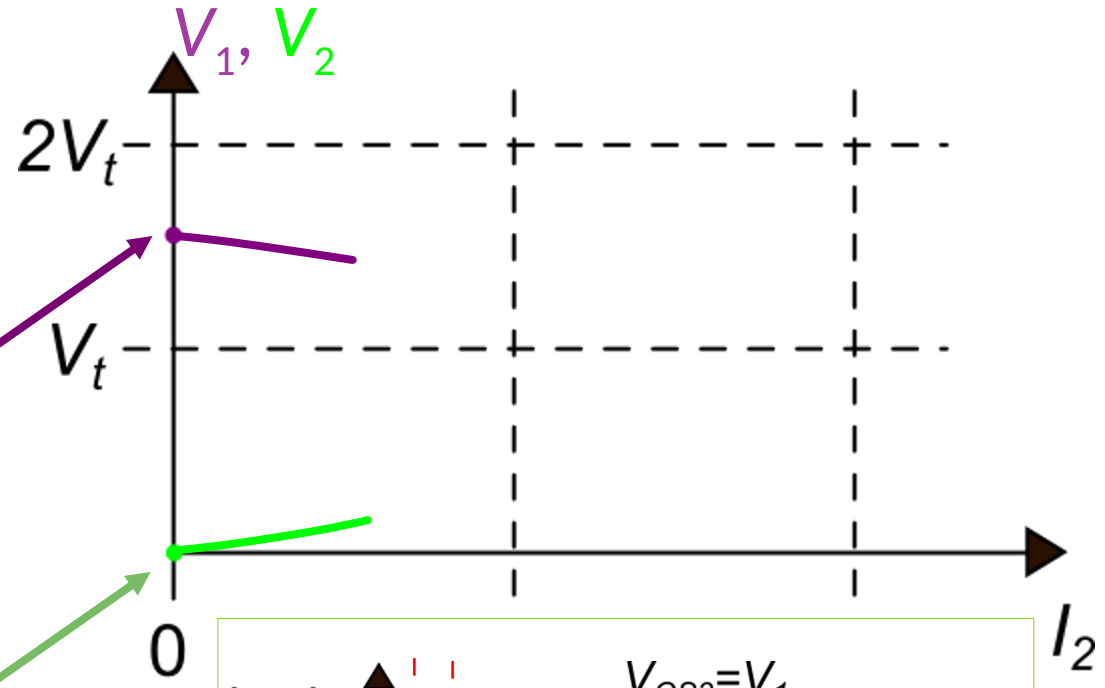
**Design condition:** we size $\beta_L$ in such a way that:

$$V_1(0) = V_{GS1}(0) < 2V_t \Rightarrow V_{GS1}(0) - V_t < V_t$$

The reason will be clear later

# Analysis of the four-transistor cell: increasing $I_2$



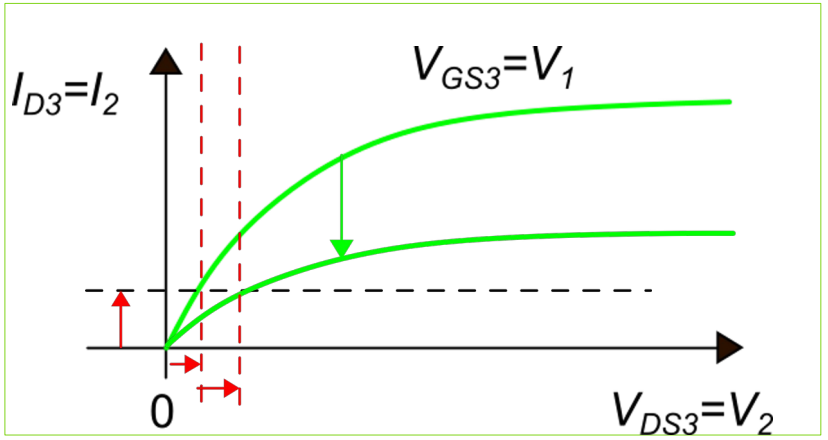




As $I_2$ increases, $I_1$ decreases by the same amount, then $V_1$ decreases:

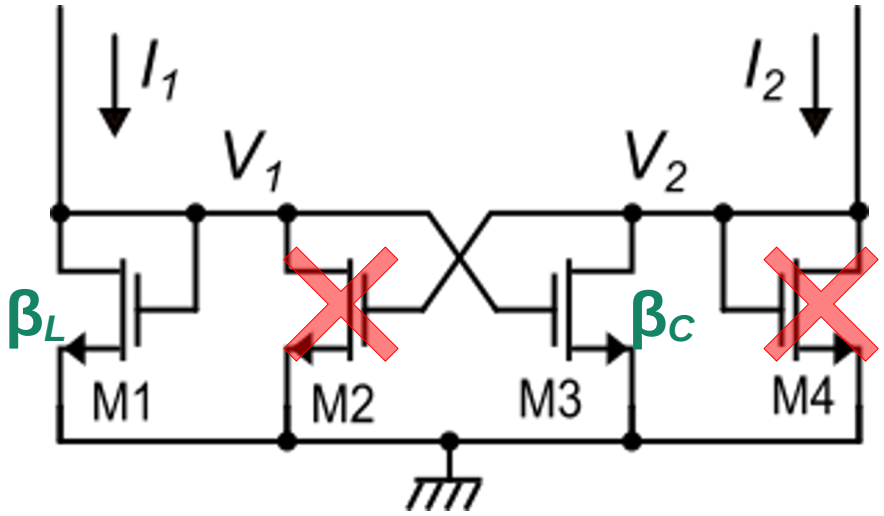
$$V_1 = V_{GS1} = V_t + \sqrt{\frac{2I_1}{\beta_L}}$$

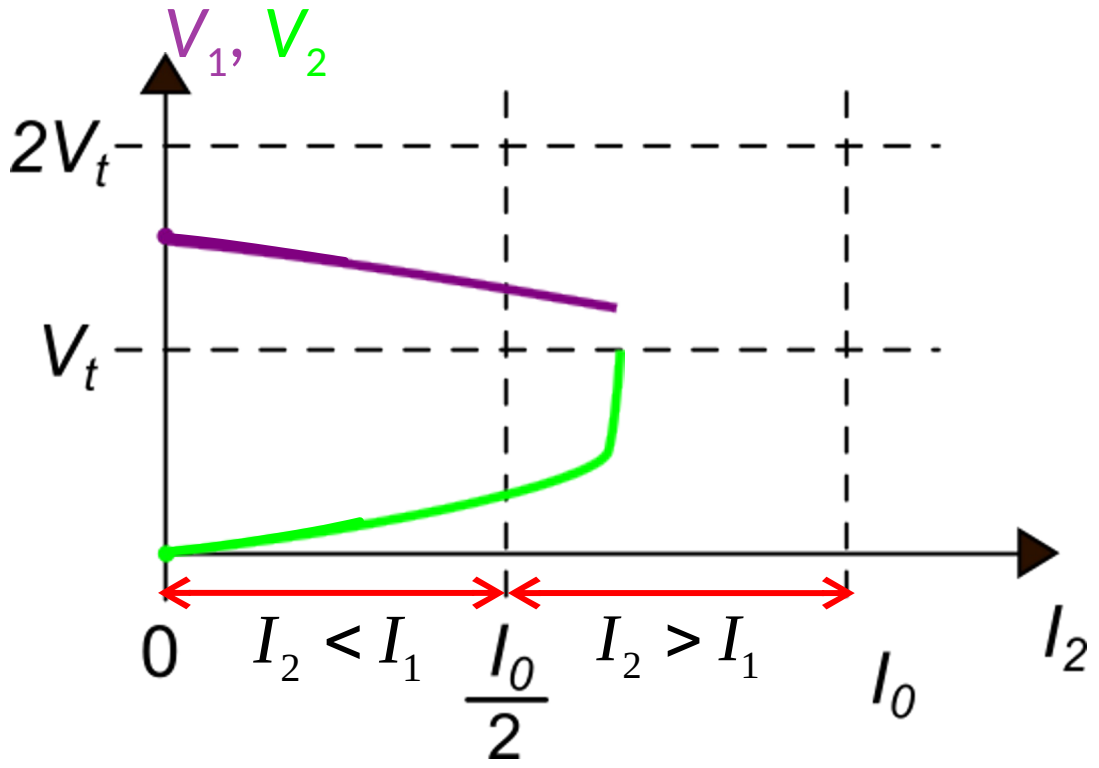
Until $V_2 < V_t$: M2, M4 are off

$V_2$ increases:
as a consequence
of $I_2$ increase
while $V_{GS3}=V_1$ decrease



# Analysis of the four-transistor cell: $V_2$ reaches $V_t$




For $V_2 = V_t$, M2 and M4 are still off.

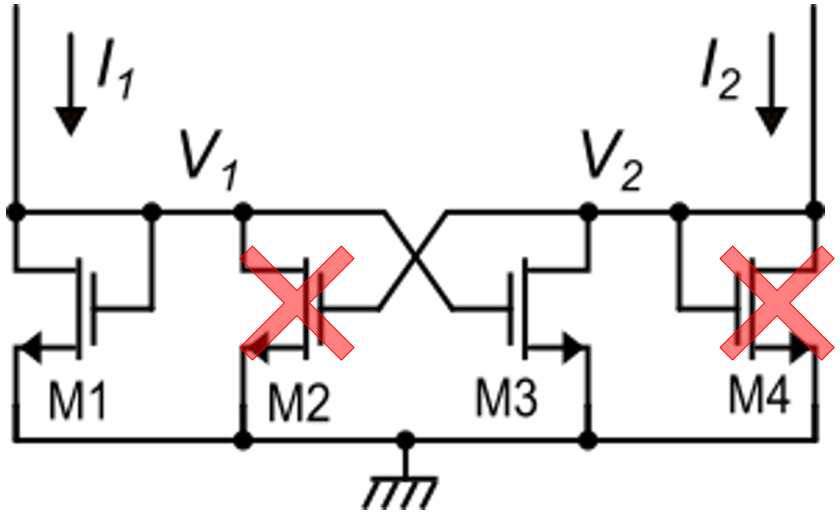
Then (M1 and M3 have the same VGS):

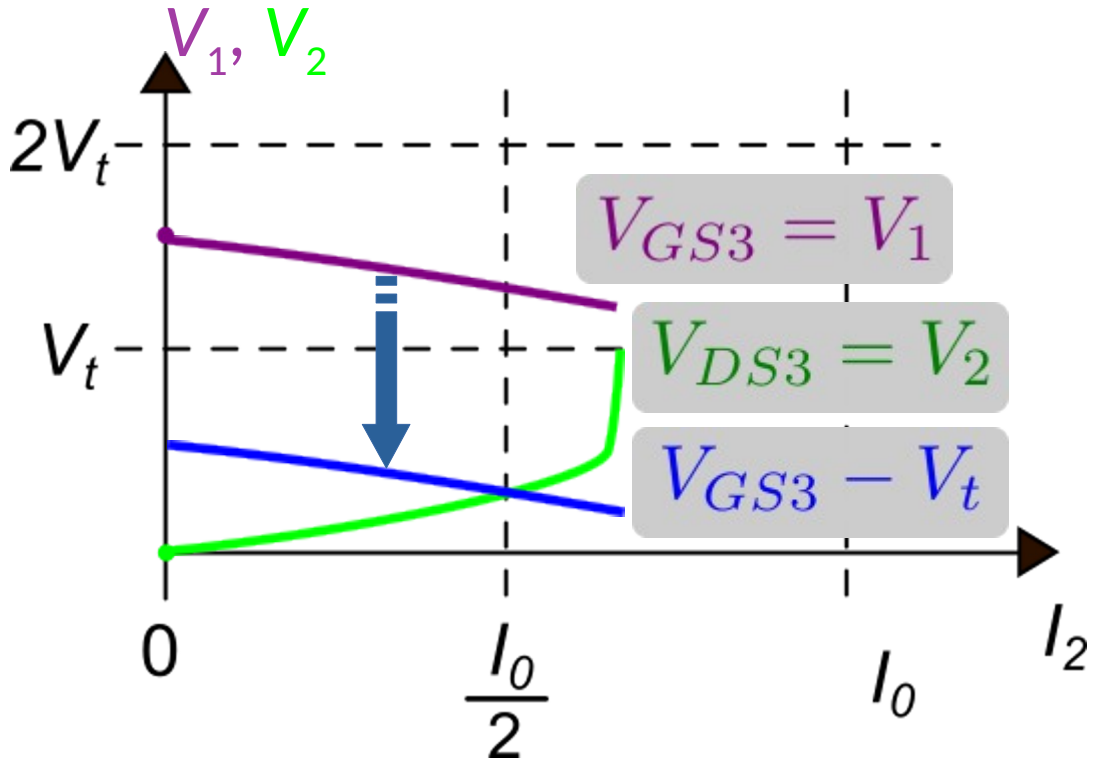
$$I_1 = I_{D1} \qquad I_2 = I_{D3}$$

→ **Hypothesis**: If M3 is now in saturation:

$$\frac{I_2}{I_1} = \frac{\beta_C}{\beta_L} > 1 \longrightarrow I_2 > I_1 : \qquad I_2 > \frac{I_0}{2}$$

# Analysis of the four-transistor cell: M3 saturation hypothesis




$$V_2 = V_t$$

Let us check whether M3 is now in saturation (was in triode region at the beginning)

$$V_{DS3} = V_2 = V_t$$

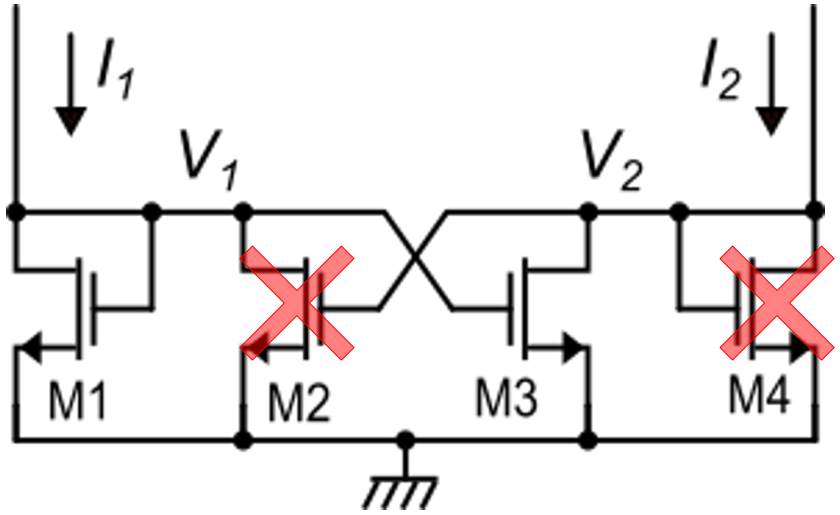
$$V_{GS3} = V_1 < V_1(0) < 2V_t$$

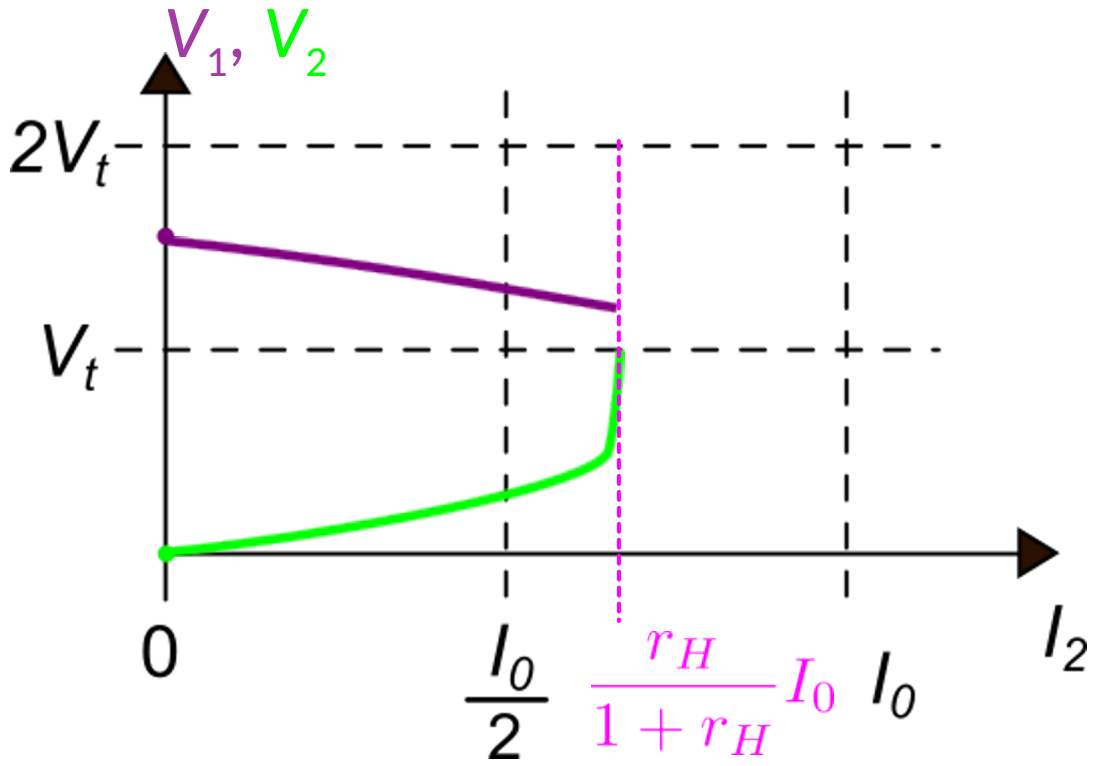
For the design condition mentioned earlier

$$V_{GS3} - V_t < V_t = V_{DS3}$$

$$V_{DS3} > V_{GS3} - V_t \quad \checkmark \text{OK}$$

# Analysis of the four-transistor cell: $V_2$ reaches $V_t$

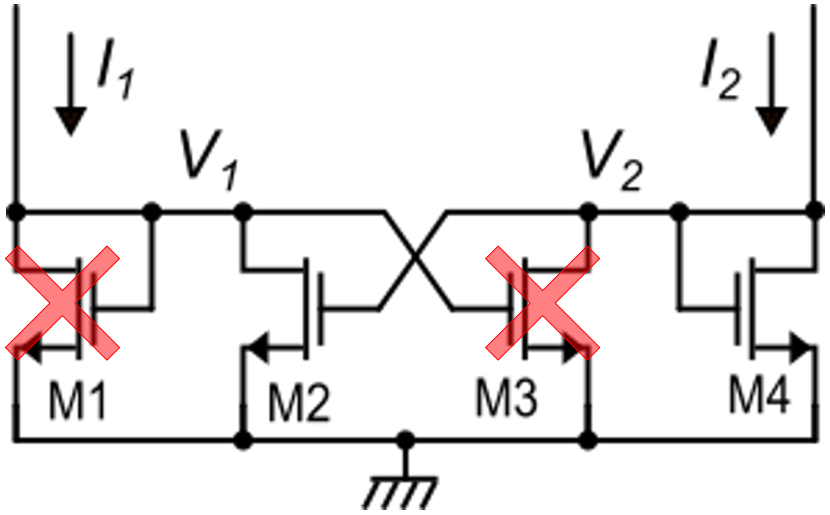


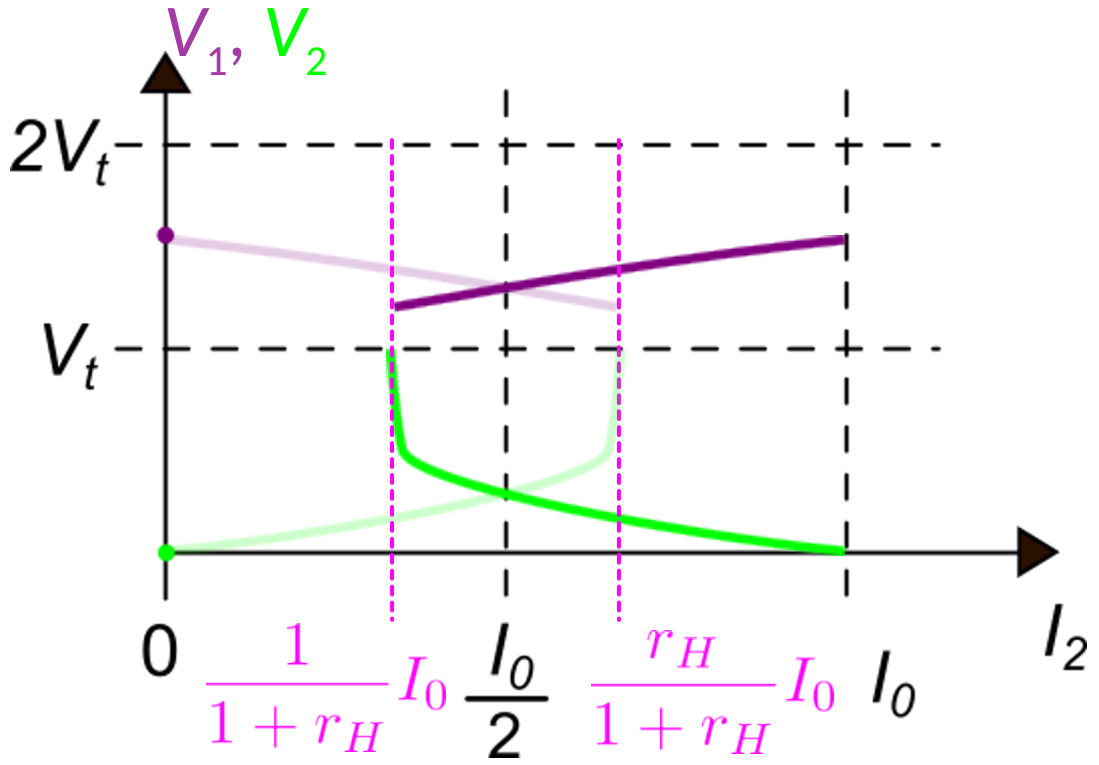




$$V_2 = V_t: \quad \frac{I_2}{I_1} = \frac{\beta_C}{\beta_L} \equiv r_H > 1$$

$$I_0 = I_1 + I_2 = (1 + r_H) I_1 = \frac{1 + r_H}{r_H} I_2$$

# Analysis of the four-transistor cell: starting from the opposite end point

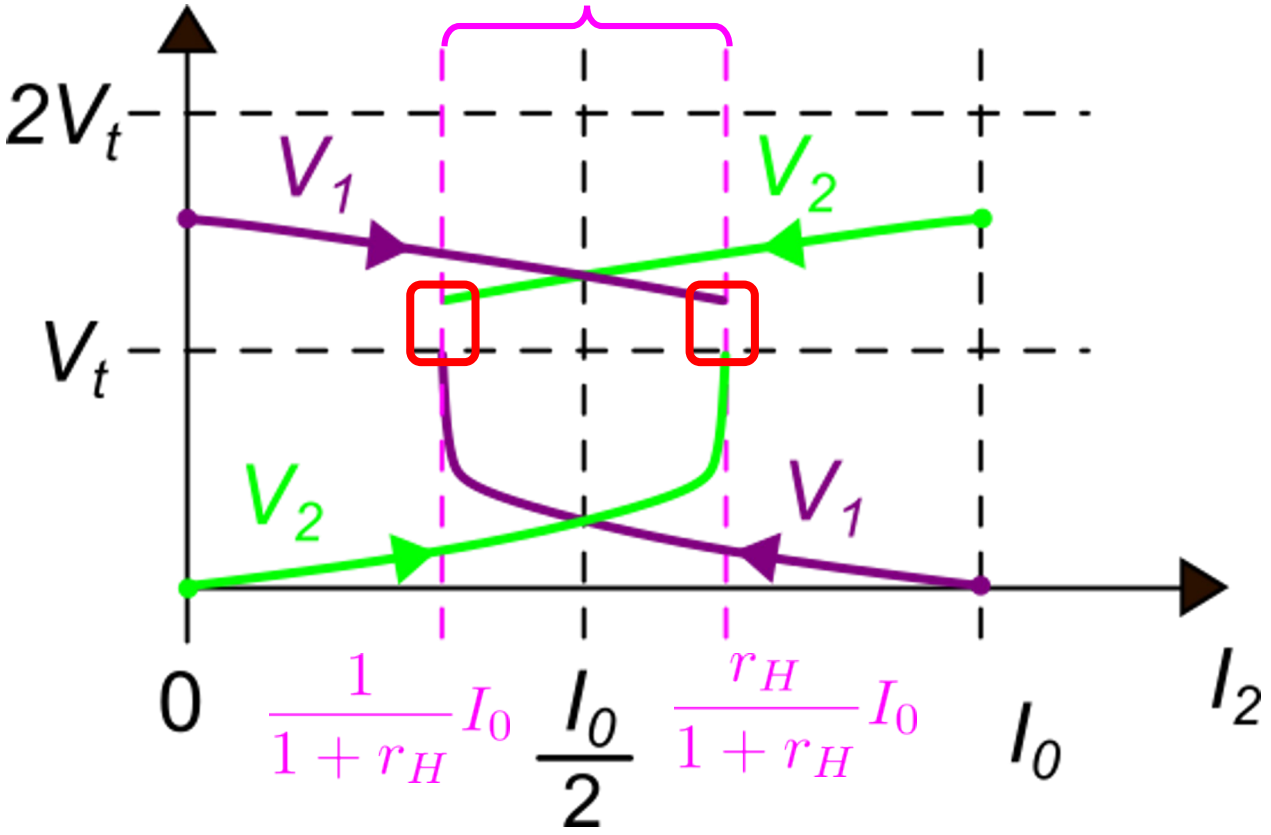



Repeating the same procedure but starting from the rightmost point ($I_1 = 0$, $I_2 = I_0$), we obtain a <u>symmetrical behavior</u> (around $I_0/2$) with $V_1$ and $V_2$ interchanged.

Now $V_1$ reaches $V_t$ for $I_1/I_2 = r_H$.

# Analysis of the four-transistor cell: combining the two behaviours

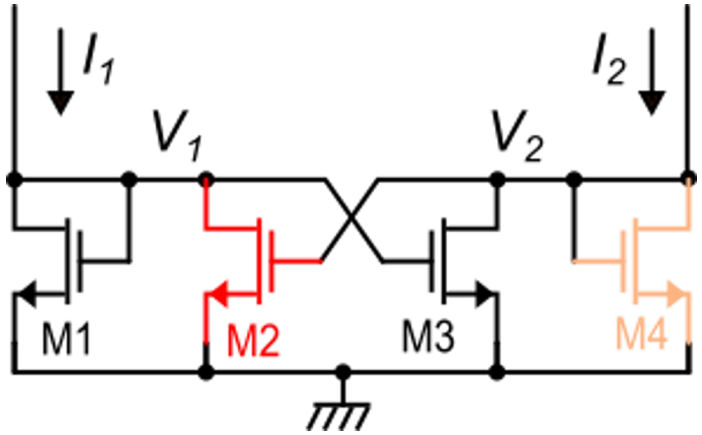


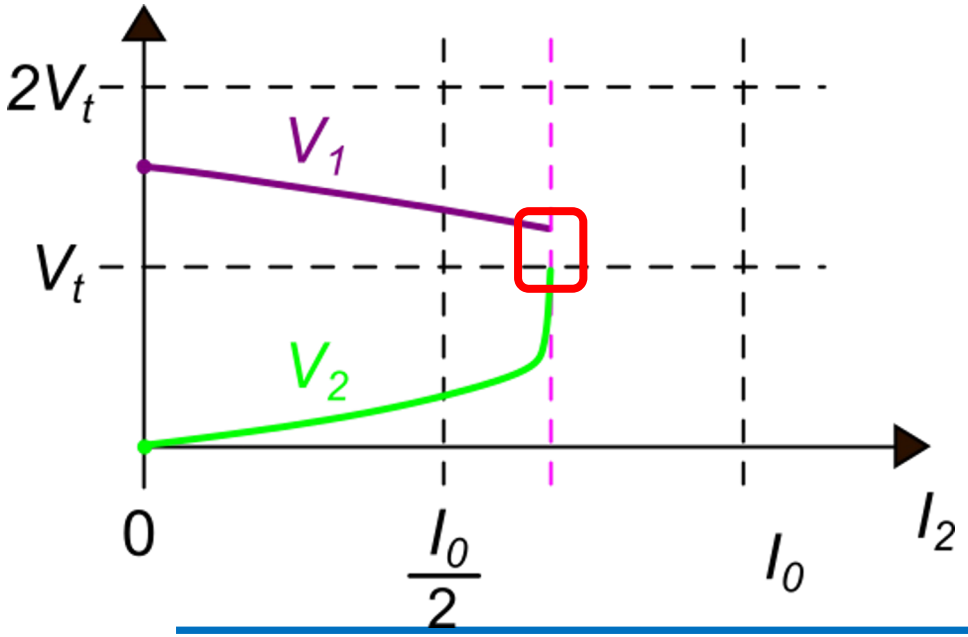

In this **region**, there are two possible stable states, depending on which extreme we started from:

This means that there is **hysteresis**

Now, we investigate what happens when the lower voltage hits the $V_t$ line

# Analysis of the four-transistor cell: phenomena that happen when $V_2$ overcome $V_t$




M2 and M4 turn on (while M1 and M3 are still on)

Let us focus on M2 — **Positive feedback loop**

**1.** As M2 turns on, it start stealing current from M1

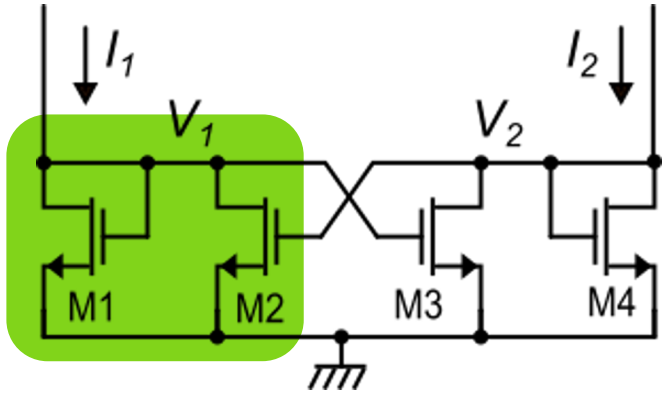
**2.** $V_1$ decreases: $V_1 = V_{GS1} = V_t + \sqrt{\frac{2I_{D1}}{\beta_L}}$

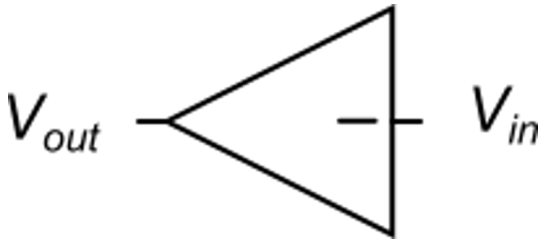
**3.** $V_{GS3} = V_1$, then $I_{D3}$ reduces, increasing the current that flows into M4

**4.** $V_2$ increases: $V_2 = V_{GS4} = V_t + \sqrt{\frac{2I_{D4}}{\beta_L}}$

**5.** $V_{GS2} = V_2$, then $I_{D2}$ increases further

# Positive feedback loop: small-signal analysis

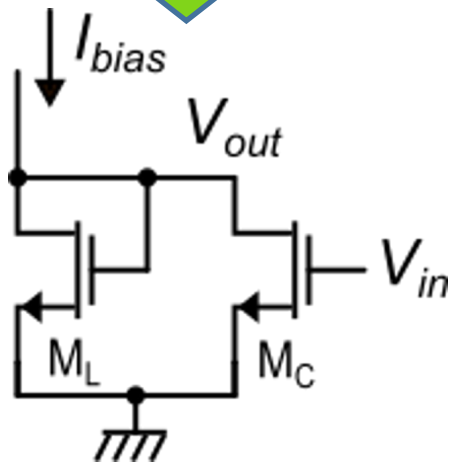


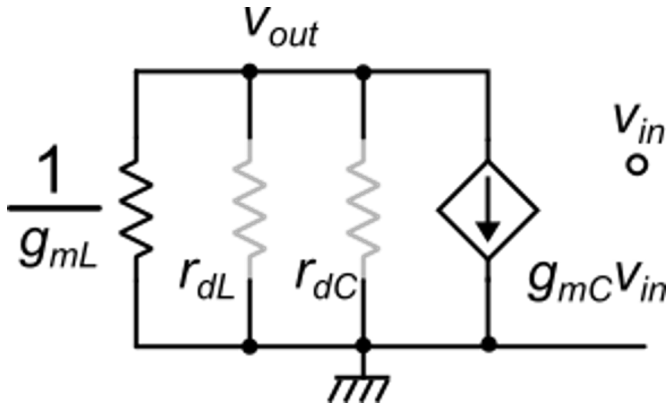

$$A = \frac{v_{out}}{v_{in}} = -g_{mC}\left(\frac{1}{g_{mL}} // r_{dL} // r_{dC}\right)$$

$$A \cong -\frac{g_{mC}}{g_{mL}}$$

Each half circuit is equivalent to an amplifier




Small signal equivalent circuit

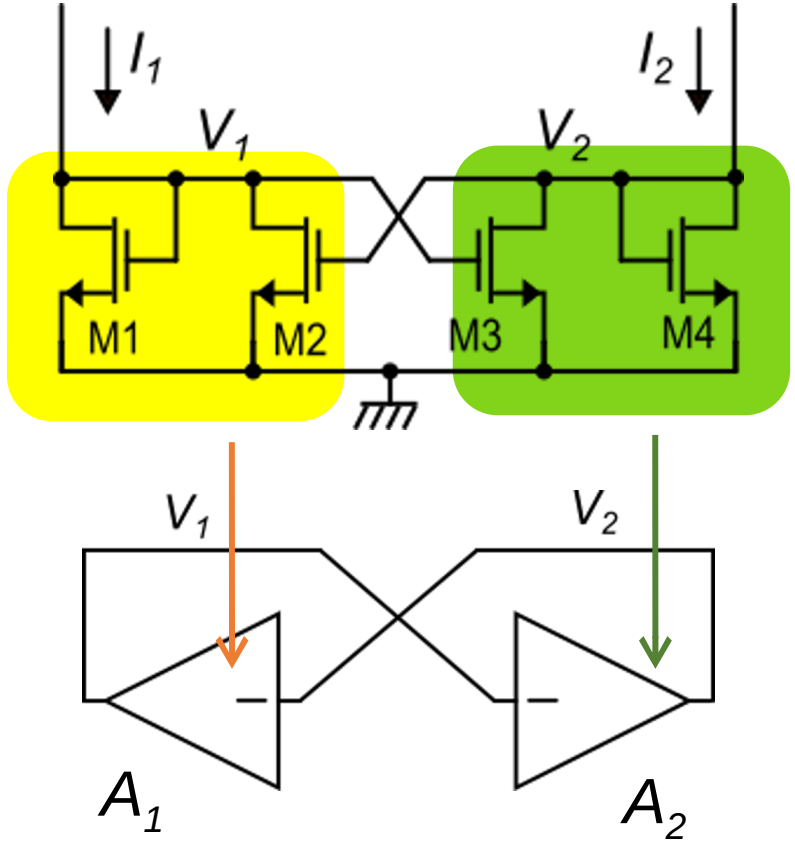



Due to the presence of the $r_d$'s, the magnitude of A is slightly less than

$$\frac{g_{mC}}{g_{mL}}$$

# Positive feedback loop: small-signal analysis

When $V_2$ overcomes $V_t$, all MOSFETs are on:




$$A_1 = -\frac{g_{m2}}{g_{m1}};\quad A_2 = -\frac{g_{m3}}{g_{m4}}$$

$$\beta A = A_1 A_2 > 0$$ Positive feedback

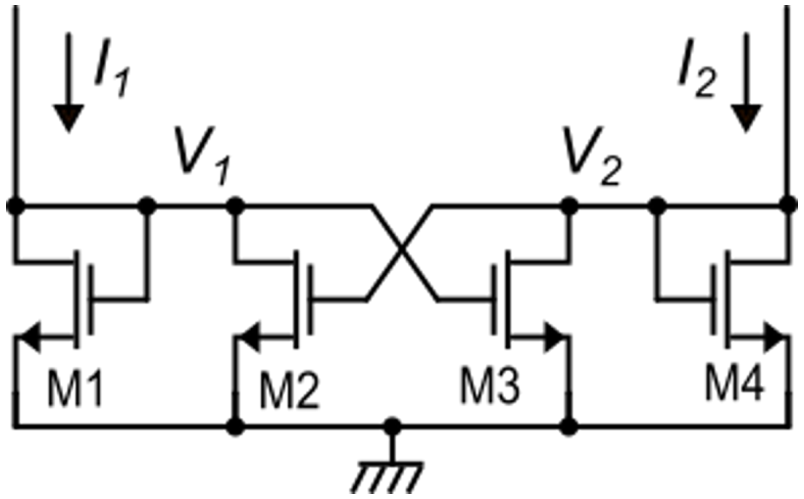
$$g_{m1} = \beta_L (V_{GS1} - V_t),\ g_{m2} = \beta_C (V_{GS2} - V_t)$$

$$g_{m3} = \beta_C (V_{GS3} - V_t),\ g_{m4} = \beta_L (V_{GS4} - V_t)$$

$$V_{GS1} = V_{GS3} = V_1,\ V_{GS2} = V_{GS4} = V_2$$

$$\beta A = \frac{\beta_C (V_2 - V_t)}{\beta_L (V_1 - V_t)} \cdot \frac{\beta_C (V_1 - V_t)}{\beta_L (V_2 - V_t)} = \left(\frac{\beta_C}{\beta_L}\right)^2$$

# Positive feedback loop: regeneration




$$\frac{\beta_C}{\beta_L} = r_H > 1 \Rightarrow |\beta A| > 1 \quad \text{(DC instability)}$$

Therefore, a stable condition cannot exist if all MOSFETs are on.

**Important condition**

$V_1$ and $V_2$ cannot be greater than $V_t$ <u>at same time</u> in a stable condition

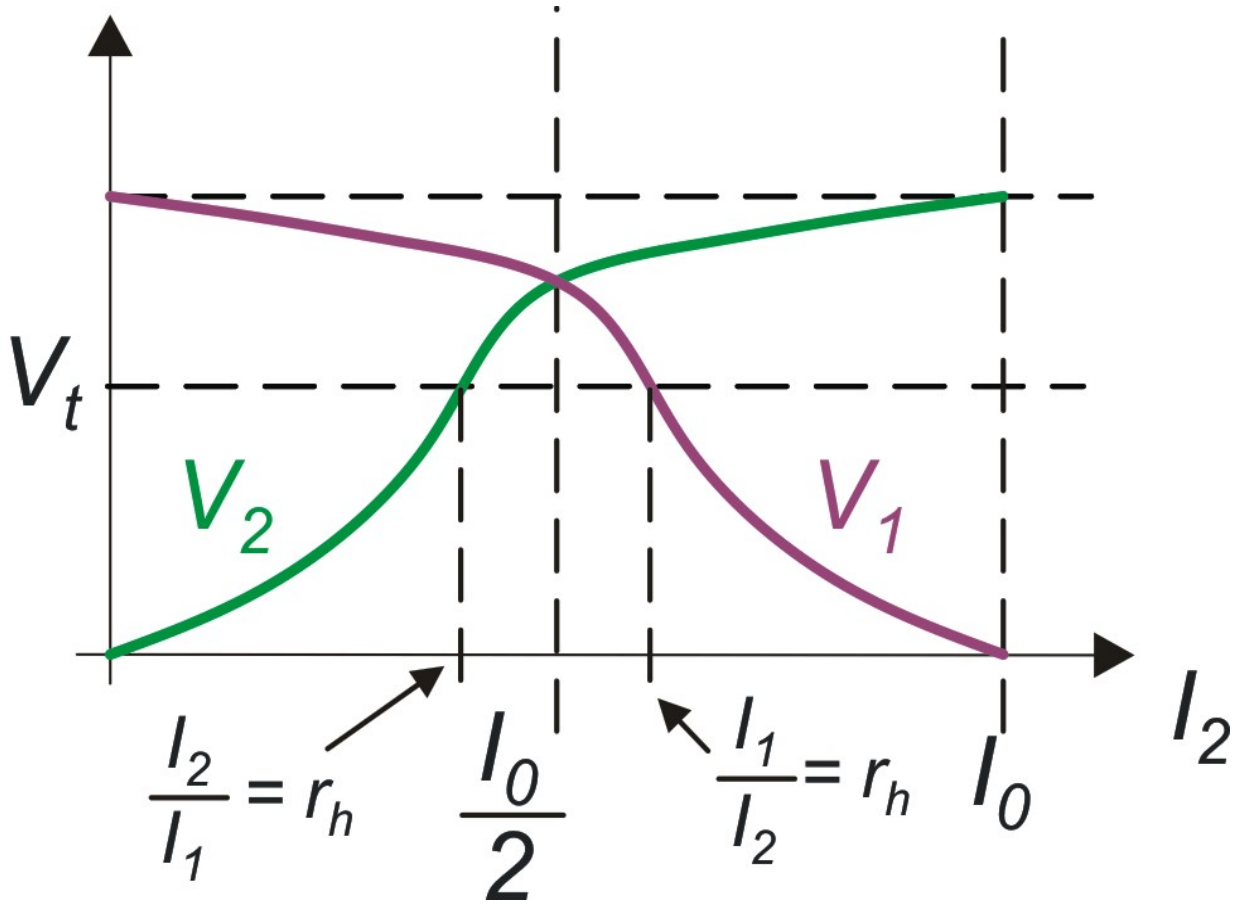
Then, when M1 is on, M4 is off and *vice versa*

# Positive feedback loop: non-regenerative case (no hysteresis)

$$\frac{\beta_C}{\beta_L} = r_H < 1$$

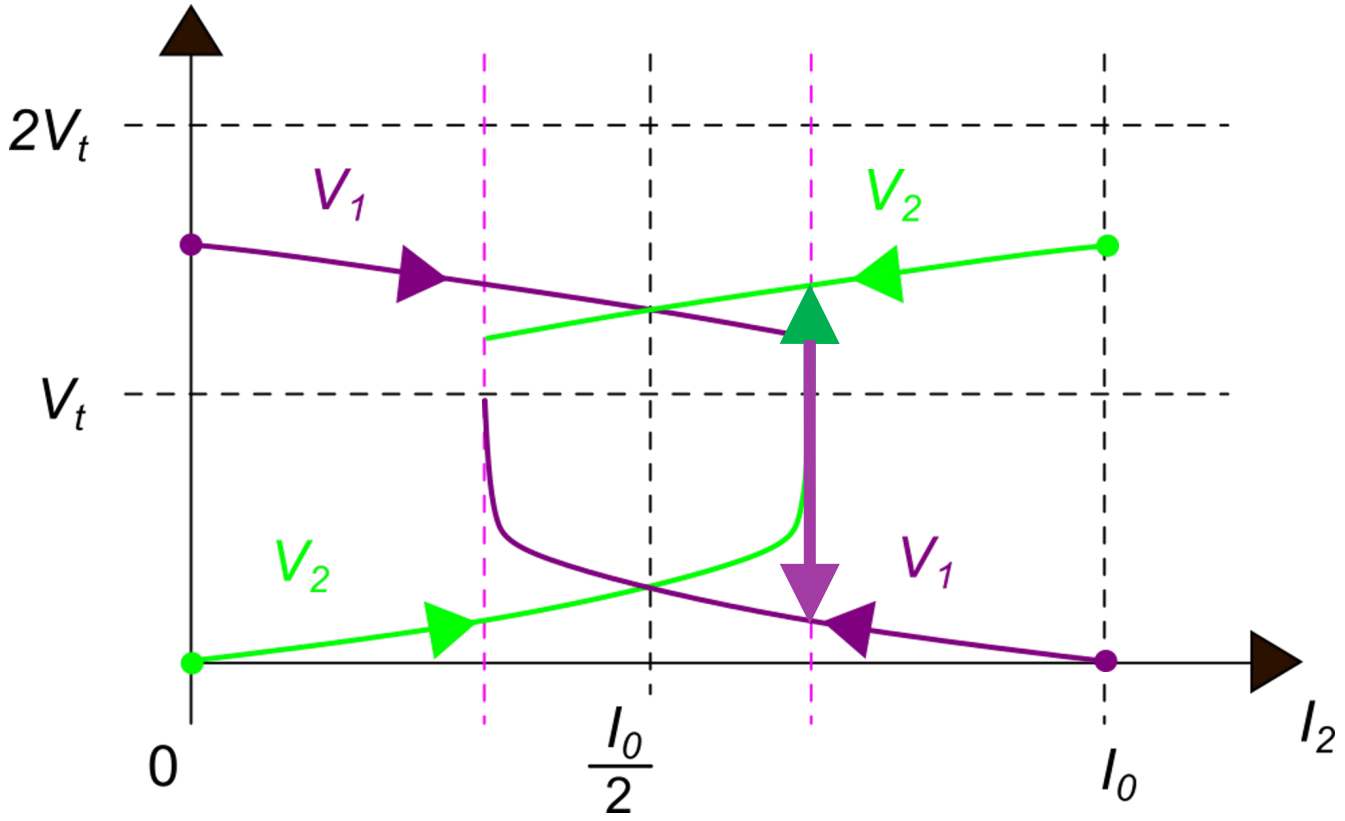
$$|\beta A| = \left(\frac{\beta_C}{\beta_L}\right)^2 < 1$$

In this case, the positive feedback is unable to cause an abrupt transition:
Hysteresis is not present




**This configuration is never used (should be regarded as a design error)**

# Positive feedback loop: the “click”

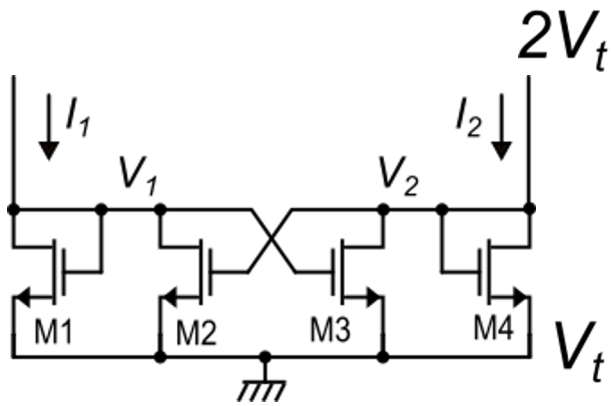


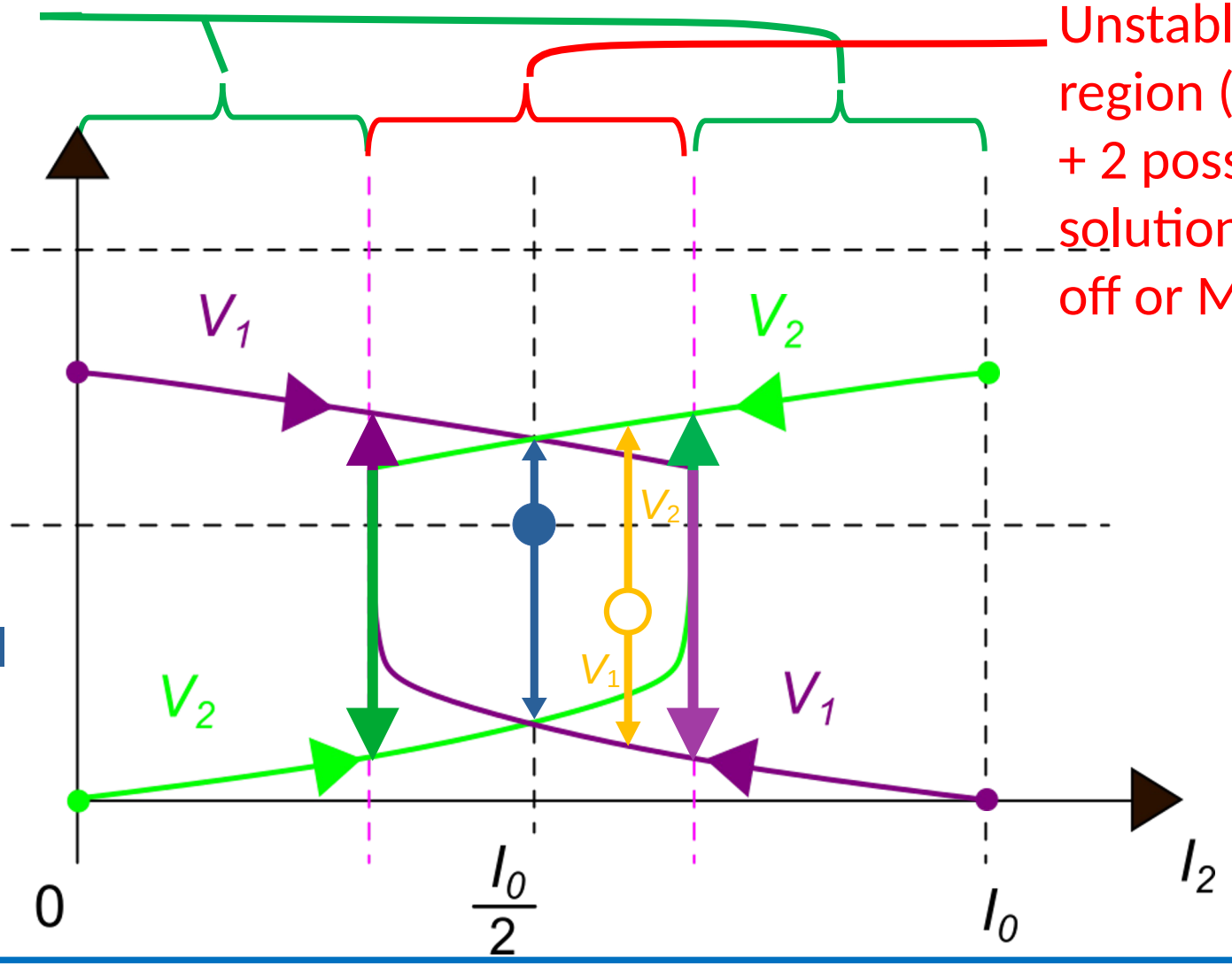

Proceeding from the left, when $V_2$ overcomes the $V_t$ line, the positive feedback makes the voltage evolve autonomously

The new stable solution is the one we already found proceeding back from the right: the regeneration stops when loop gain is no longer > 1

# Positive feedback loop: stable characteristics and unstable solution

Only one stable solution exists in these regions



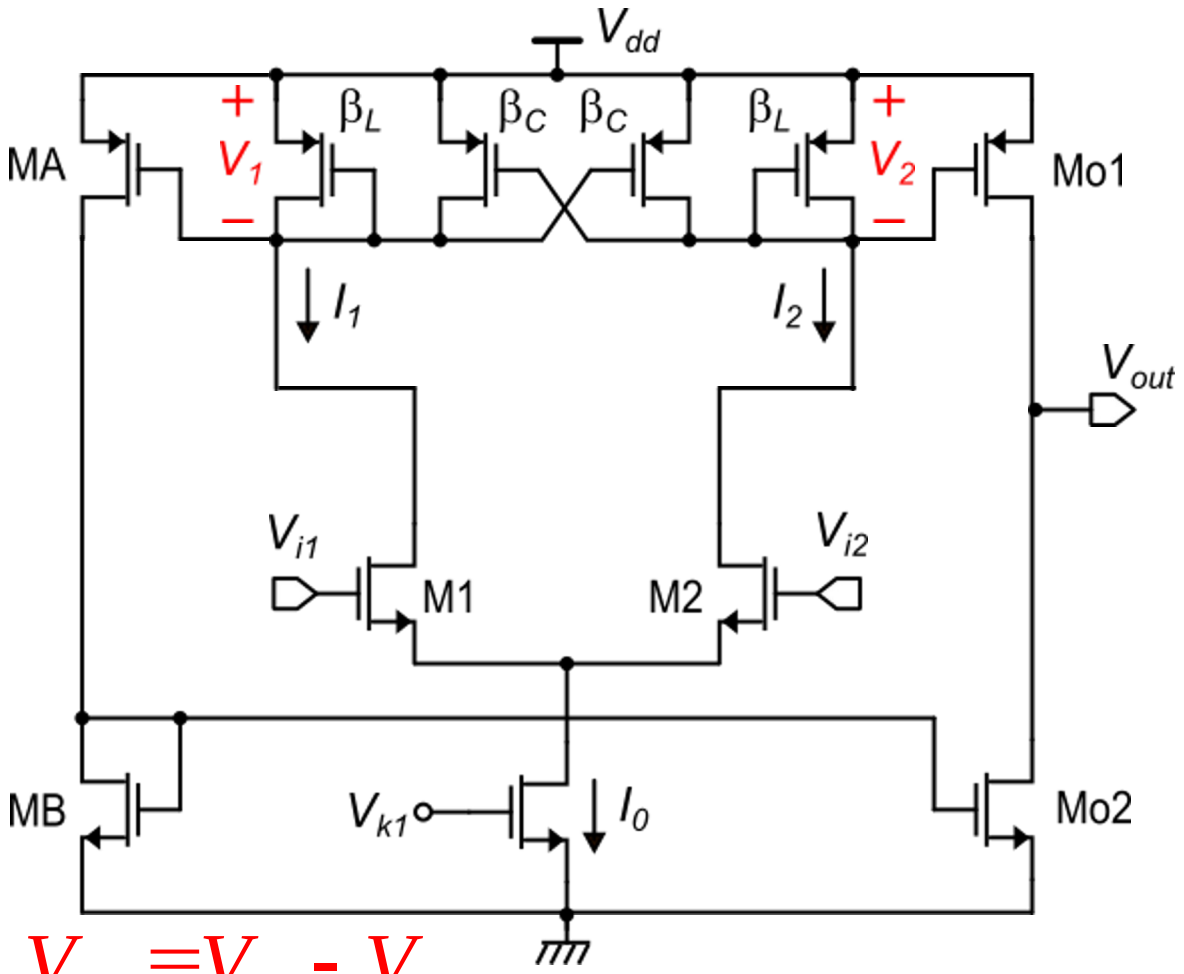

Unstable solutions in this region (all devices are on) + 2 possible stable solutions (either M1, M3 off or M2, M4 off)

- Suppose forced initial condition:
  ½ probability to evolve to one of the two stable solutions

○ Most probable evolution?

$I_2 > I_1$:
$V_2$ up, $V_1$ down

# A simple comparator based on the 4-transistor hysteresis cell




$V_{id} \equiv V_{i2} - V_{i1}$

We start with a p-version of the hysteresis cell

Currents $I_1$ and $I_2$ are derived from the input voltage $V_{id}=V_{i2}-V_{i1}$ by means of a differential pair

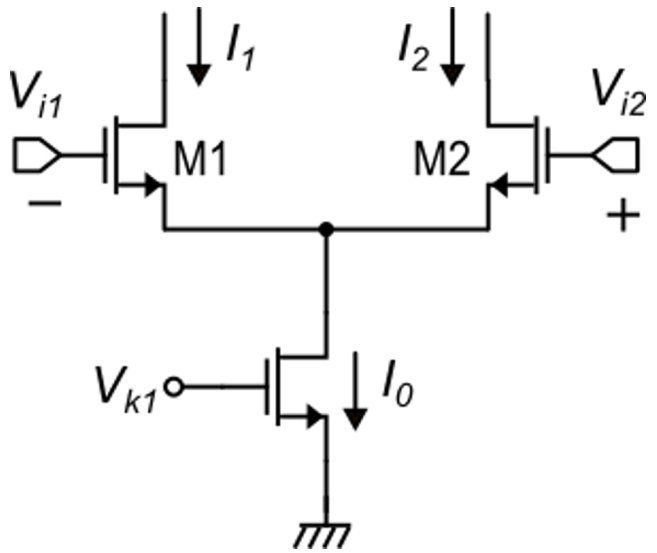
Only one at a time between $V_1$ and $V_2$ is greater than the p-mos threshold voltage.

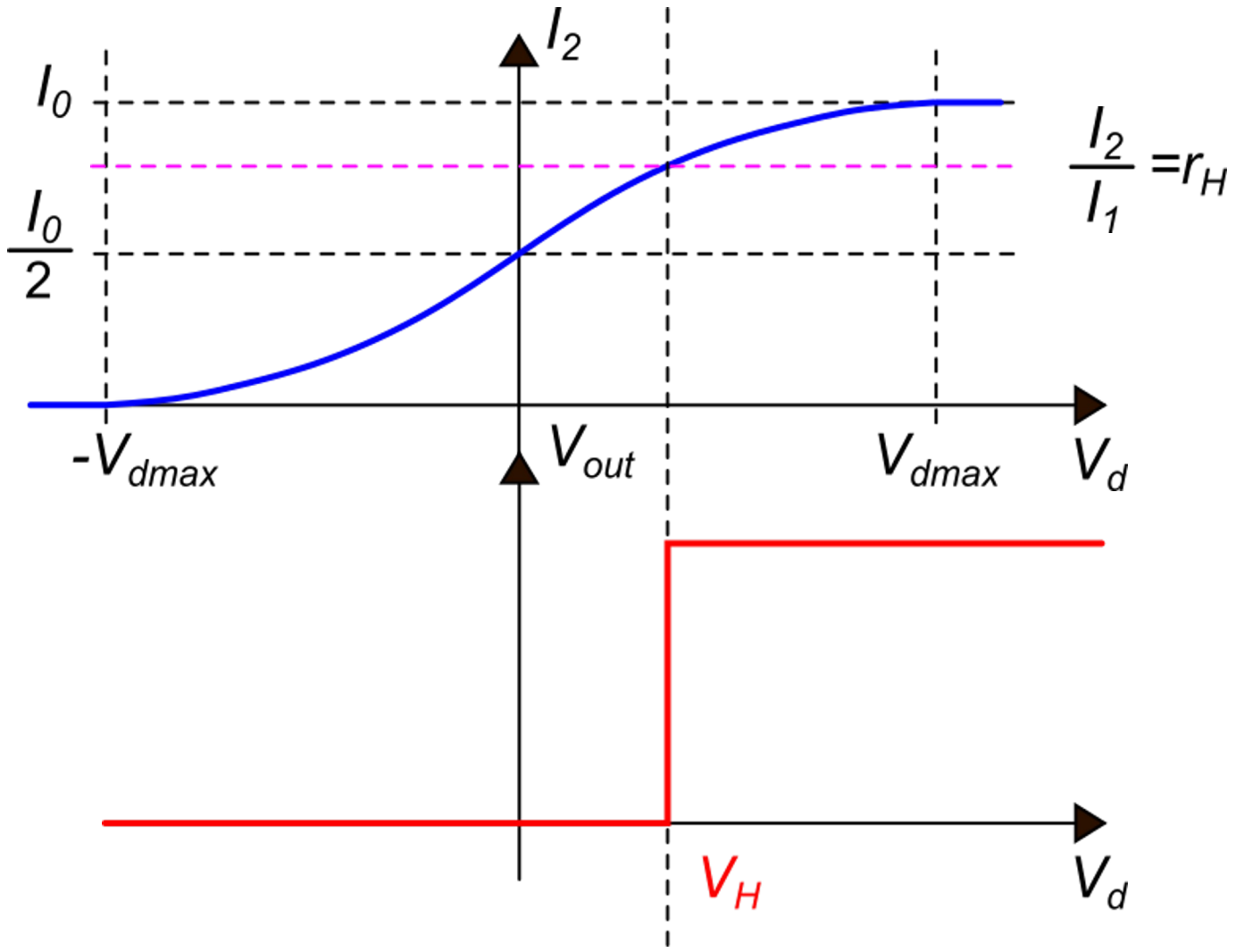
If $V_1 > |V_{tp}|$, $V_2 < |V_{tp}|$ MA, MB and Mo2 are on, while Mo1 is off: $V_{out} = 0$

If $V_2 > |V_{tp}|$, $V_1 < |V_{tp}|$, only Mo1 is on:

$V_{out} = V_{dd}$

# A simple comparator: upper threshold ($V_H$)




Using a linear approximation of the differential pair:

$$\begin{cases} I_2 - I_1 = g_{m1} V_{id} \\ I_2 + I_1 = I_0 \end{cases}$$

# A simple comparator: upper threshold ($V_H$)

$$\begin{cases} I_2 - I_1 = g_{m1} V_H \\ I_2 + I_1 = I_0 \\ \dfrac{I_2}{I_1} = r_H \end{cases}$$

$$I_2 - I_1 = I_1 (r_H - 1) = g_{m1} V_H$$

$$I_2 + I_1 = I_1 (r_H + 1) = I_0$$

Dividing the upper equation by the lower one:

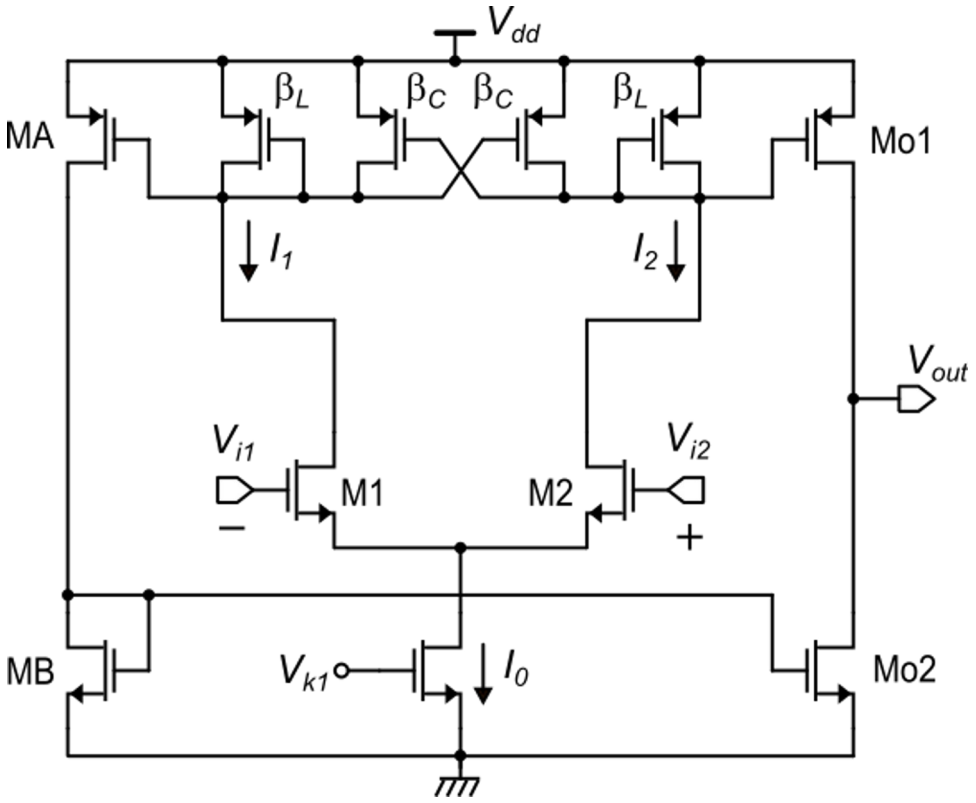
$$\frac{r_H - 1}{r_H + 1} = \frac{g_{m1}}{I_0} V_H$$

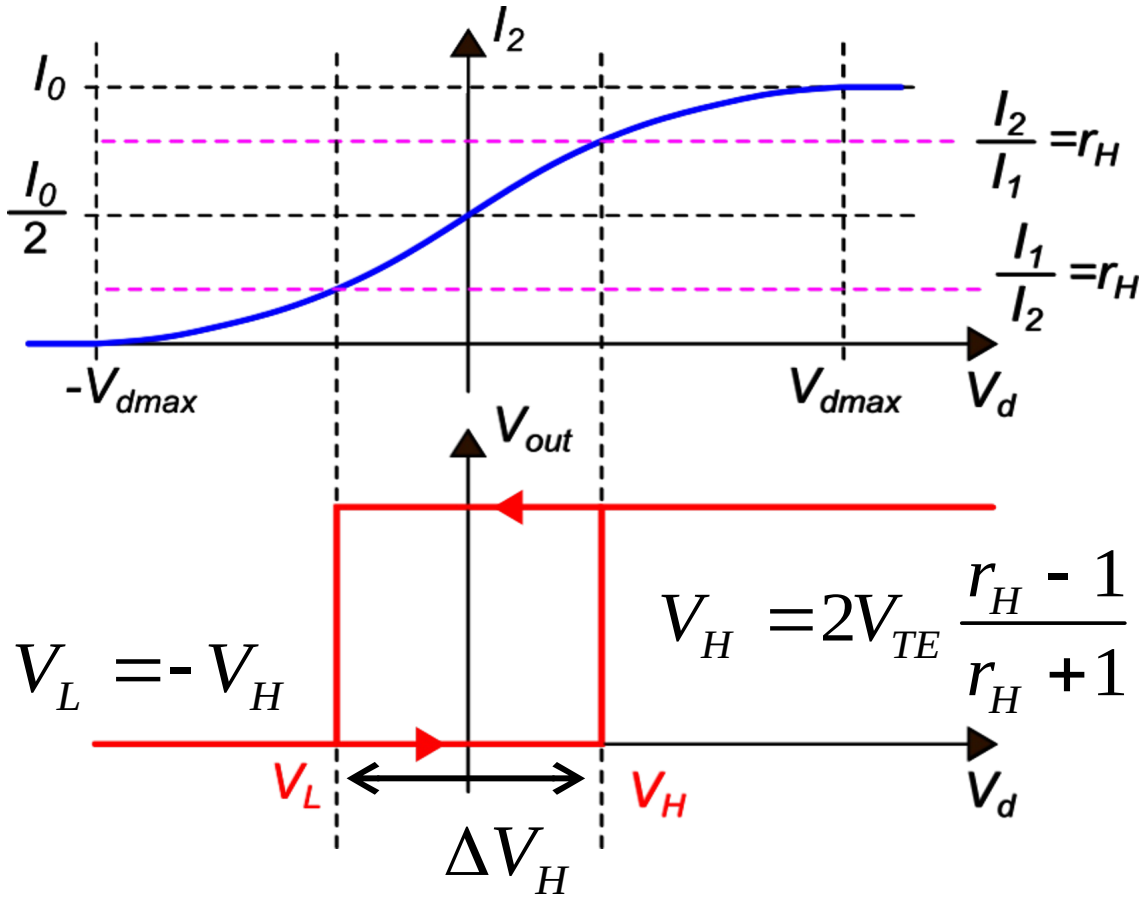
In quiescent conditions: $I_0 = 2 I_{D1-Q} = 2 V_{TE1} g_{m1}$

$$\frac{r_H - 1}{r_H + 1} = \frac{1}{2 V_{TE1}} V_H$$

$$V_H = 2 V_{TE1} \frac{r_H - 1}{r_H + 1}$$

# A simple comparator: complete characteristics




$$\Delta V_H = V_H - V_L = 4V_{TE}\frac{r_H - 1}{r_H + 1}$$

In strong inversion: $\Delta V_H = 2(V_{GS} - V_t)_1 \frac{r_H - 1}{r_H + 1}$

# A simple comparator: minimum achievable hysteresis

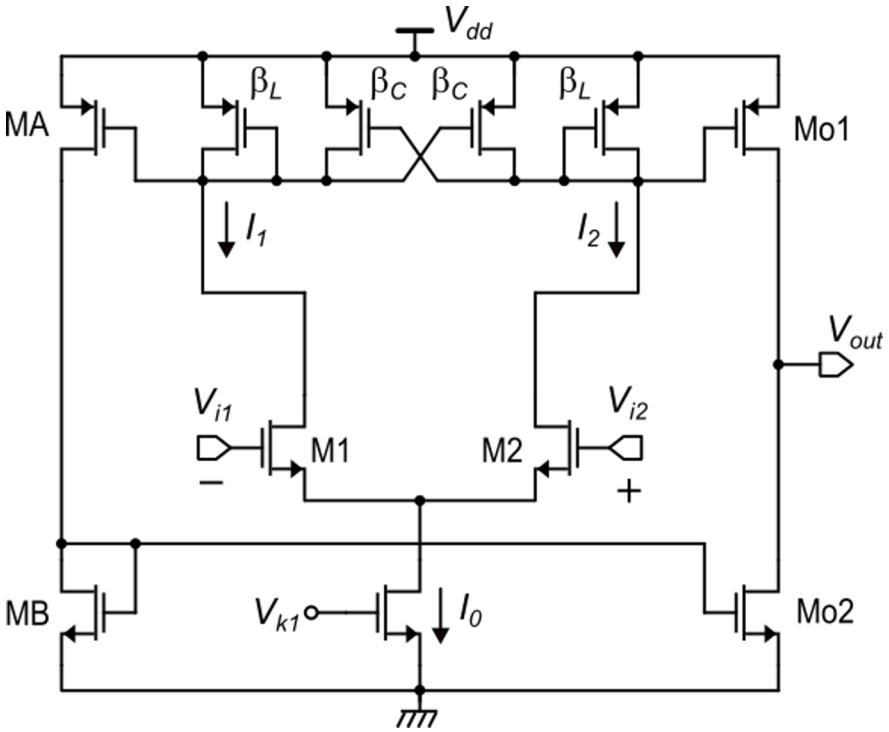
$$\Delta V_H = V_H - V_L = 4V_{TE}\frac{r_H - 1}{r_H + 1}$$

**To obtain a small hysteresis**

- Make $V_{TE1}$ as small as possible
- Make $r_H$ just slightly larger than 1

<u>However</u>, other requirements impose to make $r_H$ significantly larger than 1, because:

1) The calculated $|\beta A|=(r_H)^2$ is overestimated, since we have neglected the $r_d$'s
2) Process error can make $r_H < 1$ if the margin to 1 is too small
3) The transition is faster with larger $|\beta A|$



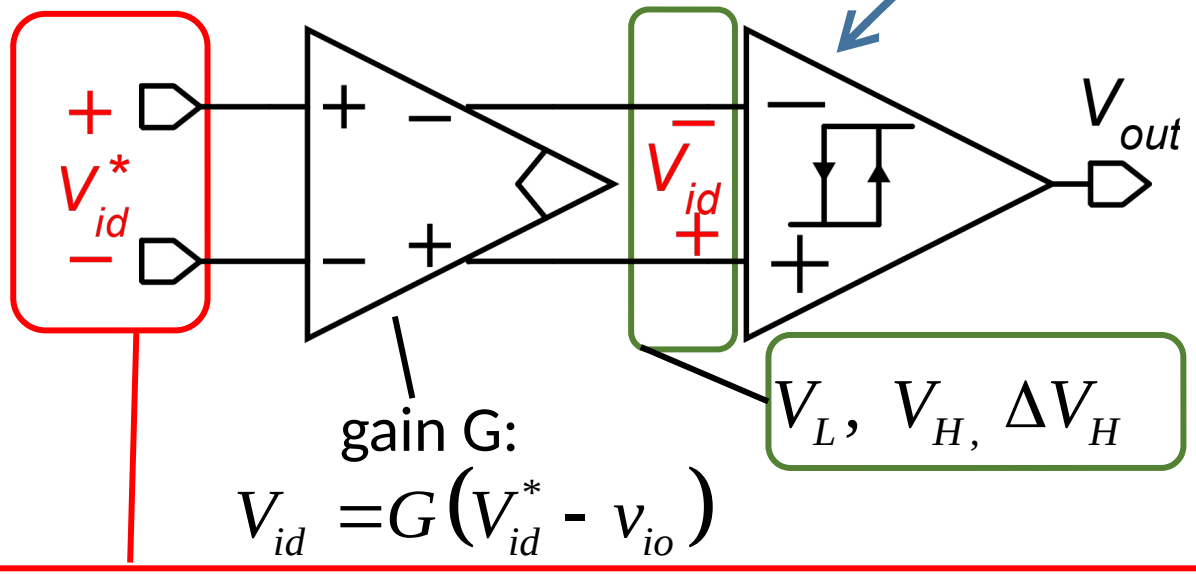

**A typical robust choice:**

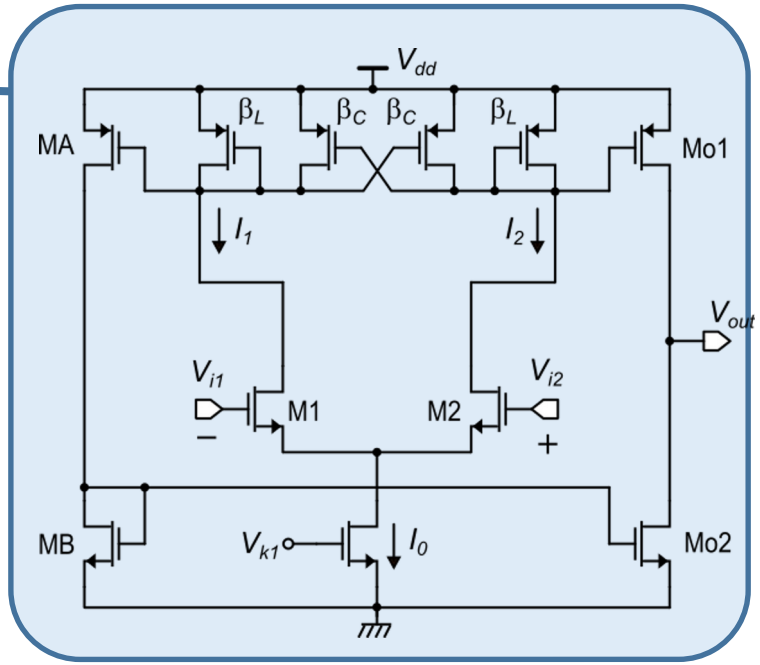
$$r_H = 2 \Rightarrow \Delta V_H = \frac{4}{3}V_{TE}$$

$\Delta V_H$ as small as **50 mV**

# A simple comparator: low hysteresis using a preamplifier

The simplest solution is using a pre-amplifier:



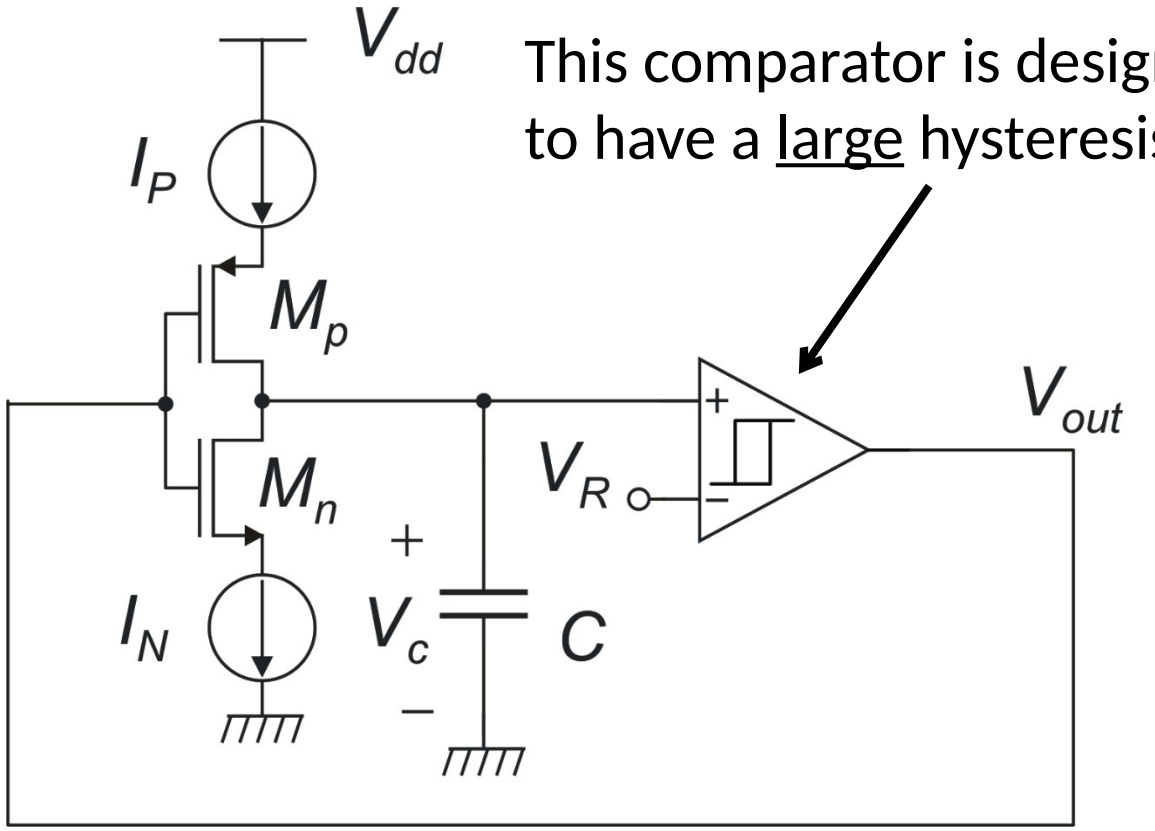

$$V^*_{id} = \frac{V_{id}}{G} + v_{io} \qquad V^*_H = \frac{V_H}{G} + v_{io}\ ,\ V^*_L = \frac{V_L}{G} + v_{io} \qquad \Delta V^*_H = \frac{\Delta V_H}{G}$$

In discrete time systems the amplifier offset can be canceled with CDS

The hysteresis is divided by the preamplifier gain (G)

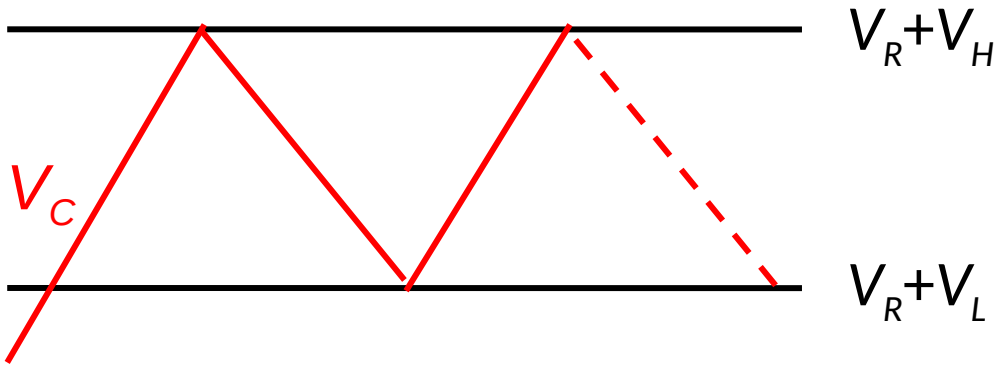
# A simple VCO for low-frequency applications

First step: place the comparator in a feedback loop with a current-controlled charging-discharging mechanism

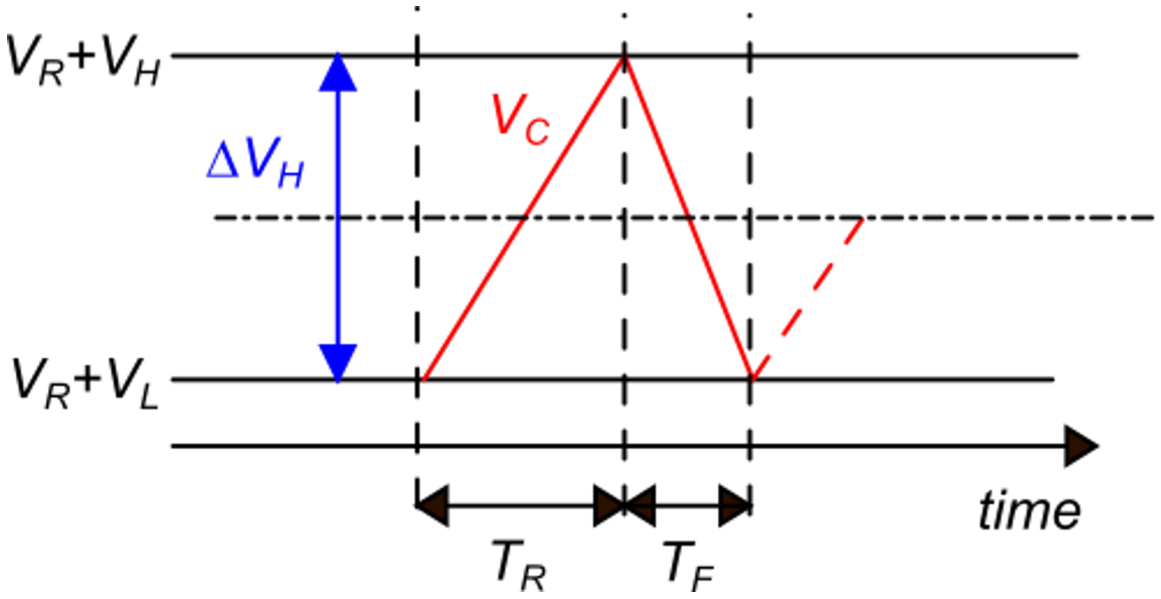


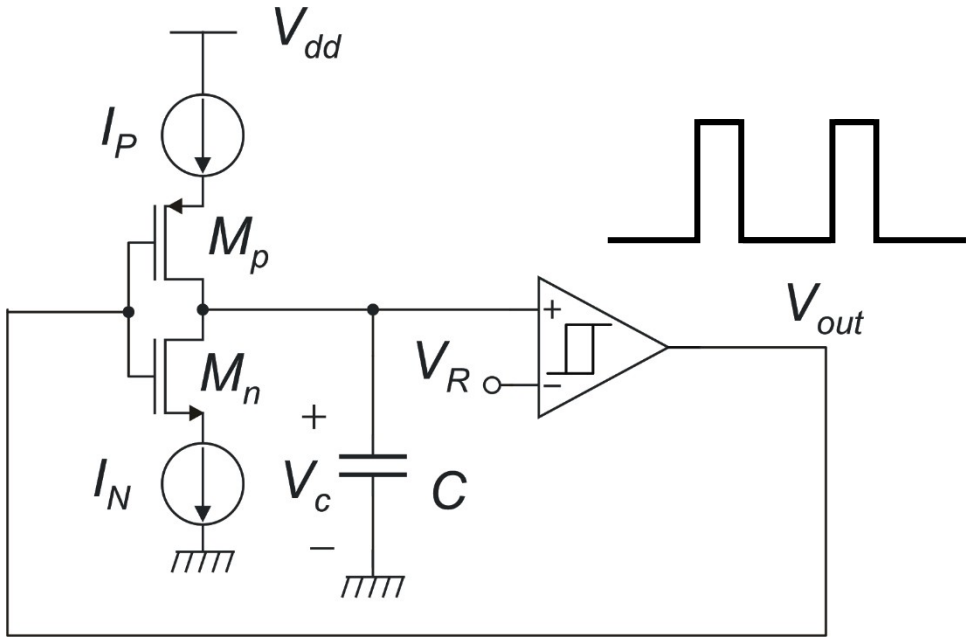

This comparator is designed to have a large hysteresis

- When $V_{out}$=0, the capacitor is charged by $I_P$
- When $V_{out}$=1, the capacitor is discharged by $I_N$



# A simple low-frequency VCO: oscillator frequency



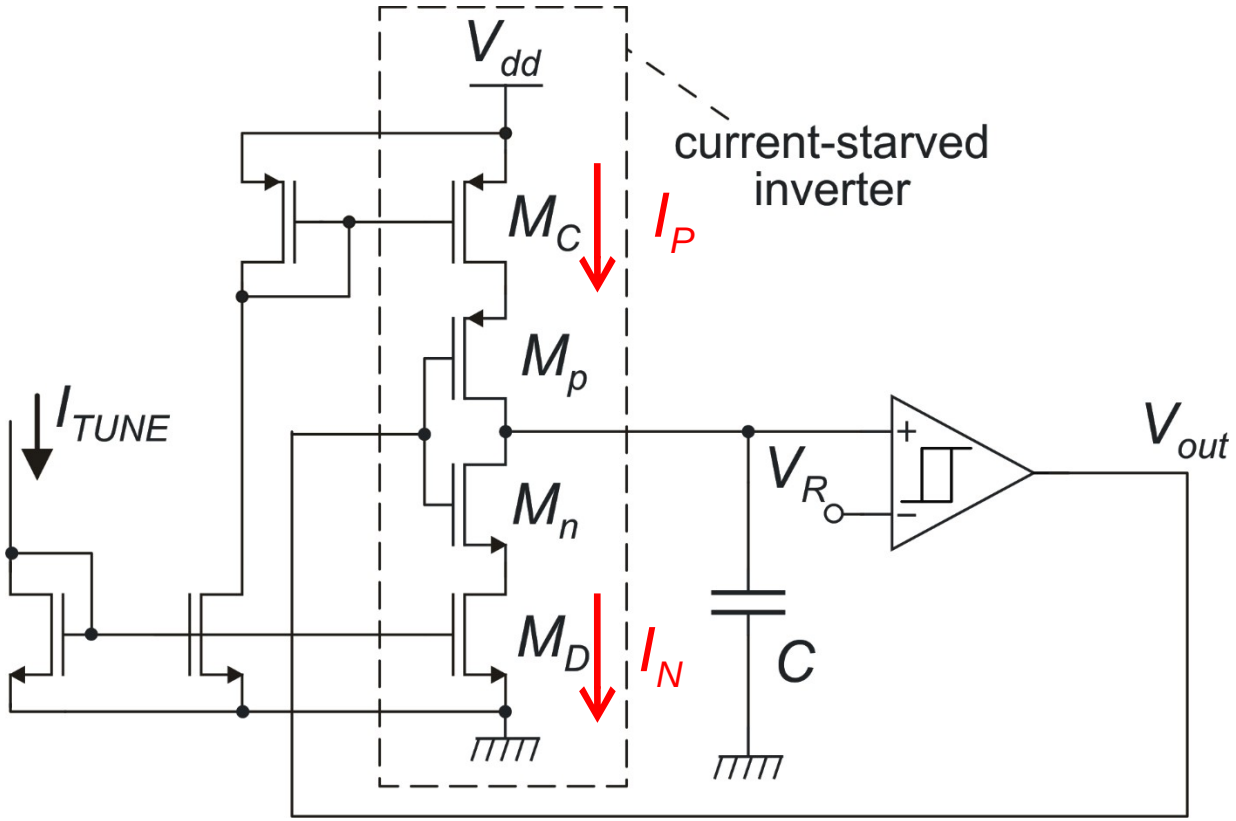




rise time = $T_R = \frac{\Delta V_H}{I_P / C} = C\frac{\Delta V_H}{I_P}$

fall time = $T_F = \frac{\Delta V_H}{I_N / C} = C\frac{\Delta V_H}{I_N}$

period = $T = T_R + T_F = C\Delta V_H\left(\frac{1}{I_p} + \frac{1}{I_N}\right)$

# A simple low-frequency VCO: Implementation with "current starved" inverter



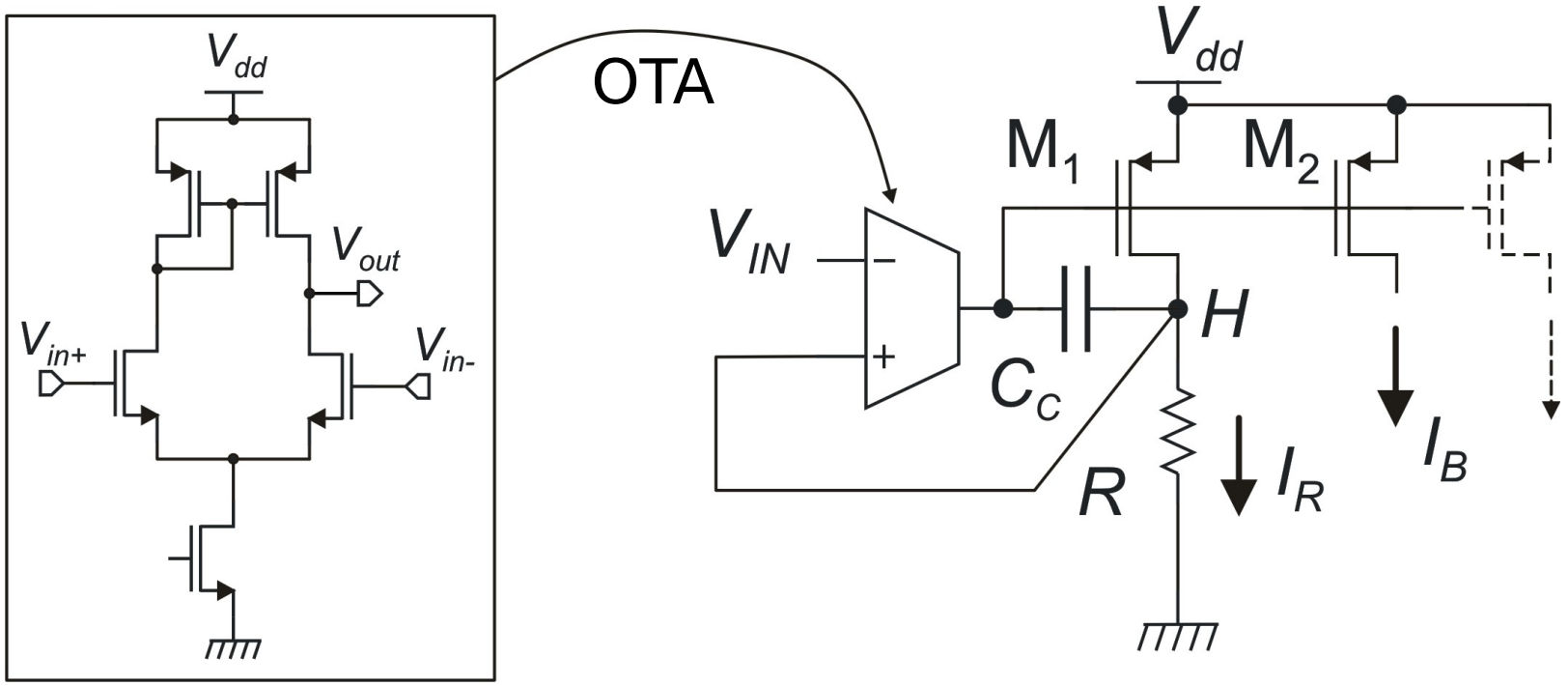

If $I_P = I_N = I_{tune}$:

$$T = 2\frac{C\Delta V_H}{I_{tune}} \qquad f = \frac{I_{tune}}{2C\Delta V_H}$$

The frequency is proportional to the tuning current (**CCO**)

Using a linear voltage to current converter it is possible to make $I_{tune}$ to be proportional to a voltage, transforming the CCO into a VCO

# A simple voltage-to-current converter



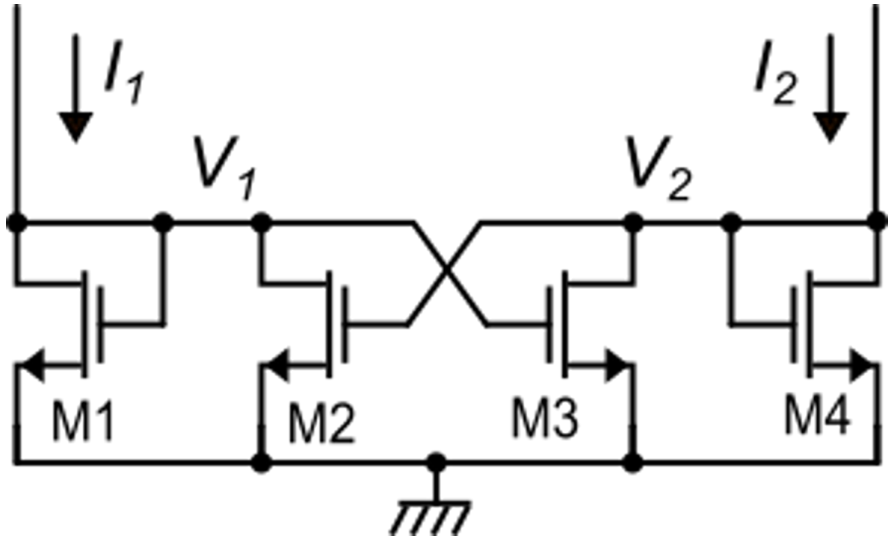

This circuit can be used also to produce constant currents from a single reference voltage

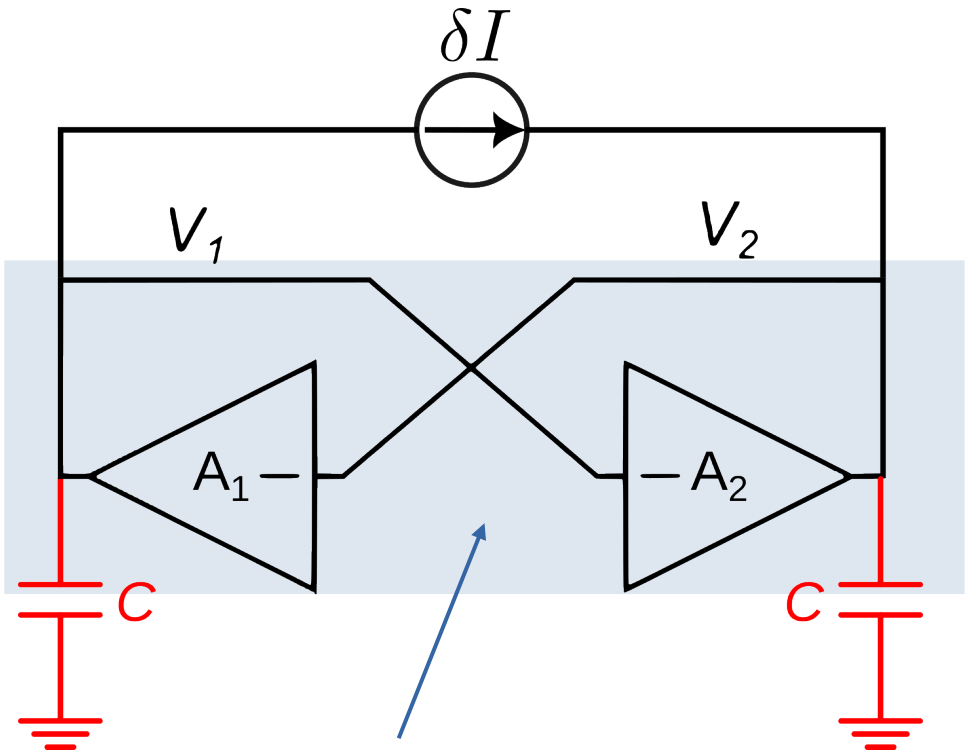
The OTA, and M1 form a two-stage op-amp with output on node H, stabilized by $C_c$ (Miller compensation).

The op-amp is closed as a buffer: $V_H = V_{IN} \Rightarrow I_R = I_{D1} = \frac{V_{in}}{R} \Rightarrow I_B = \frac{\beta_2}{\beta_1} I_{D1} = \frac{\beta_2}{\beta_1} \frac{V_{IN}}{R}$

# Speed and metastability issues

**Metastability**: the comparator does not provide a clear logical output level in a given amount of time

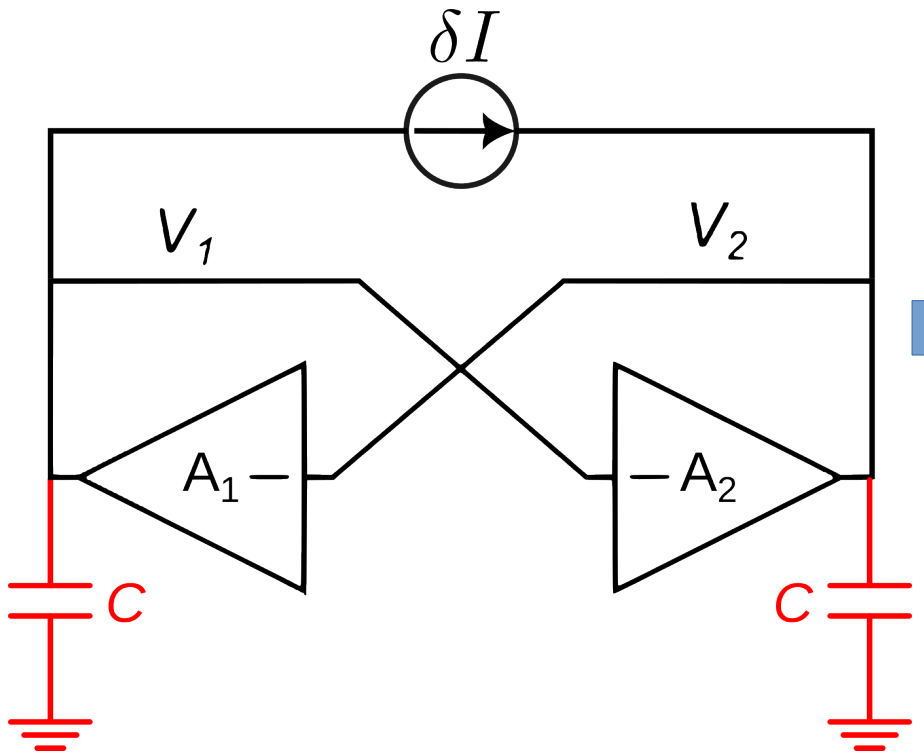


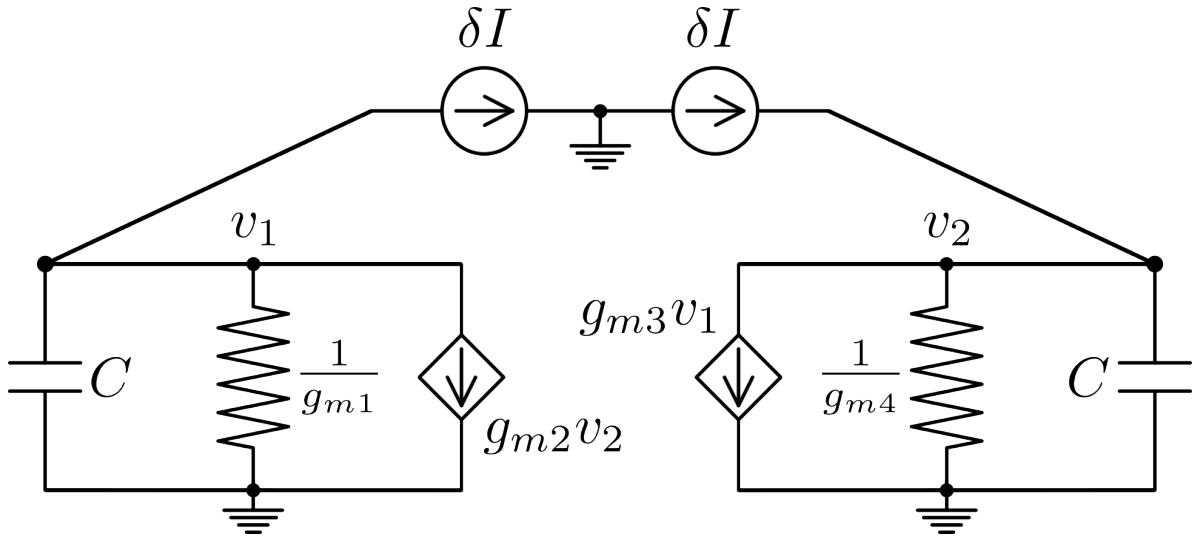




Small signal equivalent circuit of half cell: **+ inertial component (*C*)**

$R_V$: negative signed for regenerative positive feedback

# Speed and metastability issues



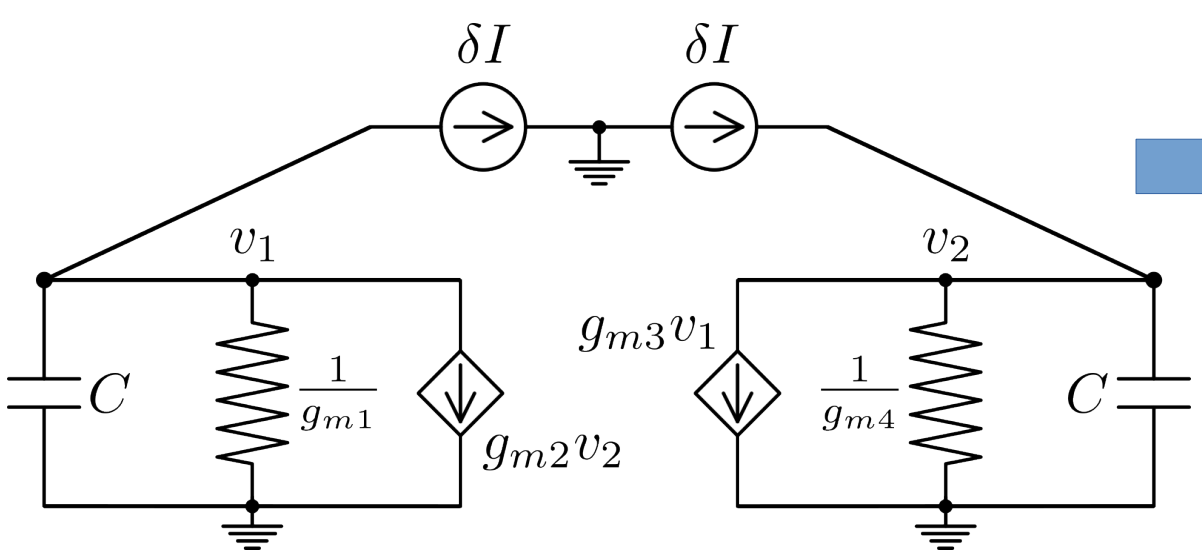

Approximations around the “click” points:

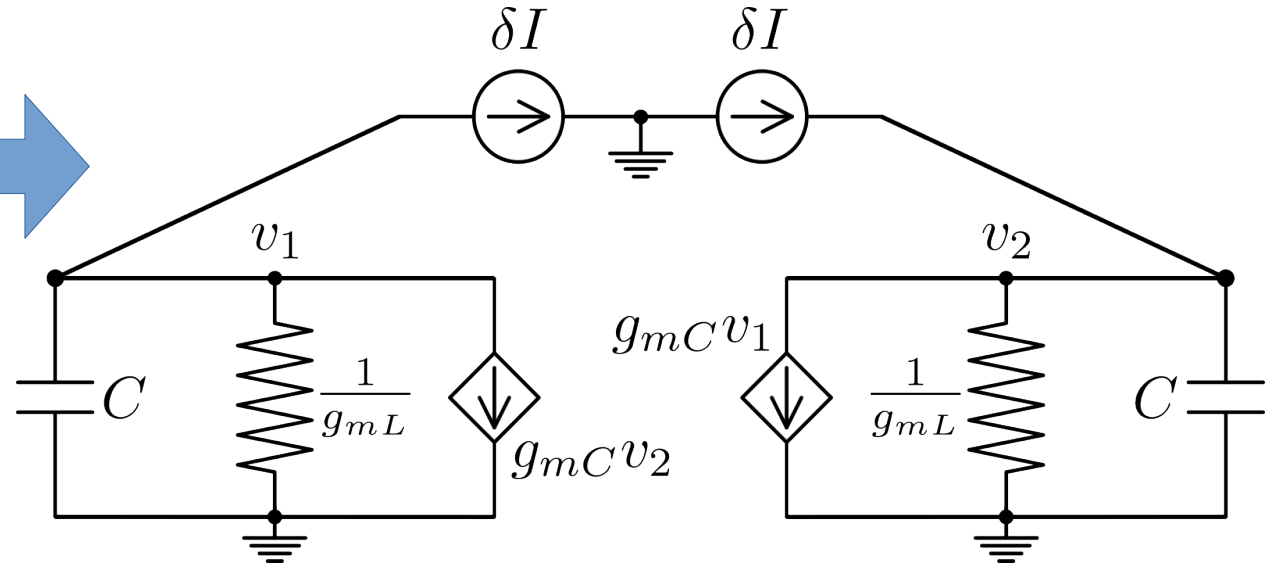
$$g_{m1} \approx g_{m4} \approx g_{mL}$$

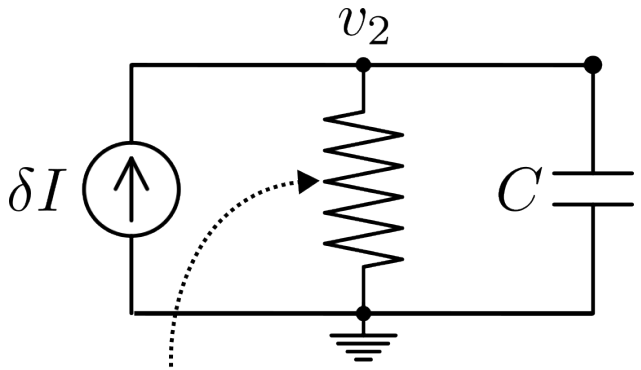
$$g_{m2} \approx g_{m3} \approx g_{mC}$$

Not rigorous but useful for understanding purposes: the circuit is non-linear anyway.
Accurate results only through electrical simulations

# Speed and metastability issues



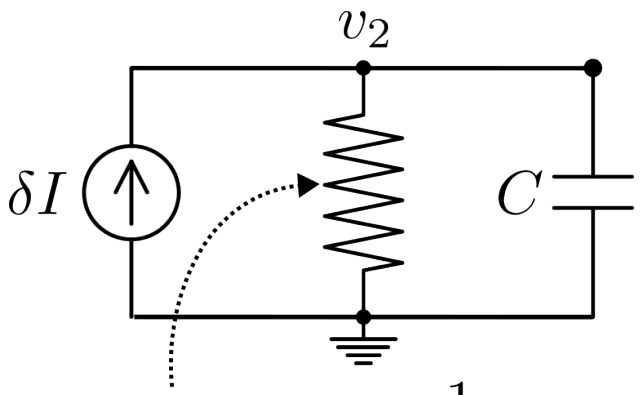

$$R_V = \frac{1}{g_{mL} - g_{mC}}$$

Under this approximation, the circuit is completely symmetric:

$v_1 \approx -v_2$

We can study only half circuit, for simplicity

# Speed and metastability issues




$$R_V = \frac{1}{g_{mL} - g_{mC}}$$

Transient response characterized by growing exponential response: $e^{at}$

$$a = \frac{1}{|R_V|C} = \frac{g_{mL}}{C}\left|1 - \frac{g_{mC}}{g_{mL}}\right| \approx \frac{g_{mL}}{C}|1 - \sqrt{\beta A}|$$

Hence, the higher βA, the faster is the response (as mentioned previously).

Designing low-hysteresis comparator by pushing βA close to 1 is a **BAD IDEA**: not only process sensitivity may lead to lack of hysteresis, but also the comparator would result very slow:

The pre-amp solution with is always used in such cases

# Syllabus

Design of integrated comparators

**Done (today's class):**

1) Ideal behaviour
2) Applications
3) Taxonomy
4) The 4T-hysteretic cell for SoC
5) Simple comparator based on the 4T-hysteretic cell
6) Low-frequency relaxation oscillator based on simple VCO
7) Notes on speed and metastability (*optional material*)

**To do (next class):**

8) Dynamic comparator example: the StrongARM case
9) Other comparator structures from literature (*optional material*)