ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

Materials Views
www.MaterialsViews.com

Electrochemical Micromachining as an Enabling Technology for Advanced Silicon Microstructuring

*Margherita Bassu, Salvatore Surdo, Lucanos Marsilio Strambini, and Giuseppe Barillaro**

Based on previous theoretical and experimental results on the electrochemical etching of silicon in HF-based aqueous electrolytes, it is shown for the first time that silicon microstructures of various shapes and silicon microsystems of high complexity can be effectively fabricated in any research lab with sub-micrometer accuracy and high aspect ratio values (about 100). This is well beyond any up-to-date wet or dry microstructuring approach and is achieved using a wet etching, low-cost technology: silicon electrochemical micromachining (ECM). Dynamic control of the etching anisotropy (from 1 to 0) as the electrochemical etching progresses allows the silicon dissolution to be switched in real-time from the anisotropic to the isotropic regime and enables advanced silicon microstructuring to be achieved through the use of high-aspect-ratio functional and sacrificial structures, the former being functional to the microsystem operation and the latter being sacrificed for accurate microsystem fabrication. World-wide dissemination of the ECM technology for silicon microstructuring is envisaged in the near future, due to its low cost and high flexibility, with high-potential impact on, though not limited to, the broad field of microelectronics and microfabrication.

1. Introduction

The fabrication of very high aspect ratio silicon microstructures (e.g., pillars, trenches, etc.) and microsystems (e.g., micro-(opto-)electromechanical systems (M(O)EMS), grippers, etc.) with an arbitrary shape at low cost is of relevance for a multitude of hot research topics and commercial applications, such as energy harvesting,[1] lab-on-a-chip fabrication[2] and 3D microchip stacking.[3] Despite the different silicon microstructuring technologies[4] (or even those based on other materials[5,6]) that have been developed so far, none of the state-of-the-art (e.g., cryogenic reactive ion etching) and commercial (e.g., wet and dry etching) micromachining approaches allows the etching of microstructures and microsystems with different shapes and micrometer-sized features to be finely controlled up to very high aspect ratios (ARs), thus enabling the actual exploitation of the room available in the third (out-of-plane) wafer direction.

Here, on the basis of previous theoretical and experimental results reported in the literature on the electrochemical dissolution of silicon in HF-based aqueous electrolytes,[7–14] we show for the first time that both silicon microstructures of various shapes and silicon microsystems of high complexity can be fabricated effectively in any research lab with sub-micrometer accuracy at high aspect-ratio values (about 100), well beyond any up-to-date wet and dry microstructuring approach, by using a wet etching low-cost technology, namely silicon electrochemical micromachining (ECM). ECM technology overcomes the limitations of up-to-date microstructuring technologies in the out-of-plane wafer direction, mainly concerning the reduced accuracy in fabrication when the aspect ratio increases over a value of about 30, as well as lag-etching problems of structures with fairly different aspect ratio values. World-wide dissemination of ECM technology for silicon microstructuring is envisaged in the near future, with high potential impact on, though not limited to, the broad field of microelectronics and microfabrication.

Micromachining tools have been developed for half a century with the aim of structuring silicon at the microscale, always breaking new research/market grounds. Since the 1960s, wet etching technology, both isotropic and anisotropic, has driven micromachining research/industry (e.g., inkjet cartridges, chromatographic columns, microtip arrays, etc.), thanks to its straightforward and low-cost approach, though it is characterized by a limited flexibility in fabrication and low integration density.[15] In the 1980s, the demand for increased flexibility in fabrication and higher integration density, driven by novel challenging applications (e.g., MEMS, lab-on-a-chip, "through-silicon-via" (TSV), etc.), pushed micromachining research/industry towards the development of dry etching technology with higher performances, although higher cost too.[15] Both wet and dry technologies are still under development, with wet technology being used nowadays for the fabrication of undemanding microstructures with a low density at lower cost, and dry technology exploited for the fabrication of complex microsystems with increased density at a higher cost.

Electrochemical etching of n-type silicon under back-side illumination in acidic (HF-based) electrolytes (back-side-illumination electrochemical etching (BIEE)) has recently been demonstrated as a unique case of microstructuring technology, having a high

Dr. M. Bassu, S. Surdo, Dr. L. M. Strambini, Prof. G. Barillaro
Dipartimento di Ingegneria dell'Informazione:
Elettronica, Informatica
Telecomunicazioni - Università di Pisa
via G. Caruso 16, 56122 Pisa, Italy
E-mail: g.barillaro@iet.unipi.it

DOI: 10.1002/adfm.201102124

 © 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

flexibility, typical of dry etching tools, and a low cost, typical of wet etching tools. BIEE was pioneered by Lehman and Föll for the controlled etching of high-aspect-ratio macropores,[8,9] and later pushed by a number of scientists to the fabrication of a multitude of high-aspect-ratio microstructures[10–14] for different applications.[16–18] ECM technology capitalizes on the experimental and theoretical results reported in the literature over the last two decades on BIEE, to enable the low-cost fabrication of both microstructures of various shapes and microsystems of high complexity with a sub-micrometer accuracy at aspect-ratio values (about 100) that are not attainable from up-to-date, bulk silicon micromachining technologies. ECM technology pushes silicon micromachining beyond the limitations of dry etching technologies, in a similar way to that which occurred nearly two decades ago, when dry etching technologies provided a means of moving beyond the limitations of wet micromachining techniques, but with a chief difference: the low cost of ECM technology with respect to dry etching technologies should make advanced silicon microstructuring available in any lab.

2. Advanced Silicon Microstructuring by ECM

As an example of the potential of ECM technology, a few experimental results concerning the fabrication of silicon microstructures and microsystems are shown in **Figure 1** (see Figure S1, Supporting Information for images of further microstructures and microsystems). Figure 1a shows a scanning electron microscopy (SEM) image of a MEMS structure consisting of an inertial, free-standing mass (340 μm × 340 μm × 130 μm) equipped with high-aspect-ratio comb-fingers and suspended by high-aspect-ratio folded springs (AR of about 100 for both the fingers and the springs) that are fixed to an anchor structure composed of a 2D array of square holes. Figure 1b,c shows details, at two different magnifications, of the MEMS structure in Figure 1a. Figure 1c, which shows one of the folded springs of the structure in Figure 1a, clearly highlights the remarkable accuracy in the microfabrication of ECM at such high-aspect-ratio values. Figure 1d shows a mechanical microgripper, designed according to work by Volland et al.[19] The proposed microgripper consists of two fingers (length of about 1 mm and thickness of 70 μm) that are electrically actuable by means of comb-finger batteries driving a spring system (Figure 1e), which allows rotation of the two fingers to be performed symmetrically. Figure 1f shows the detail of the tip of one of the microgripper fingers, which is provided with a sub-micrometer artificial surface ripple with the aim of increasing the grasping capability of the gripper. The complexity of the microstructures and microsystems reported in this work is orders of magnitude higher than that achievable by any wet etching (both chemical

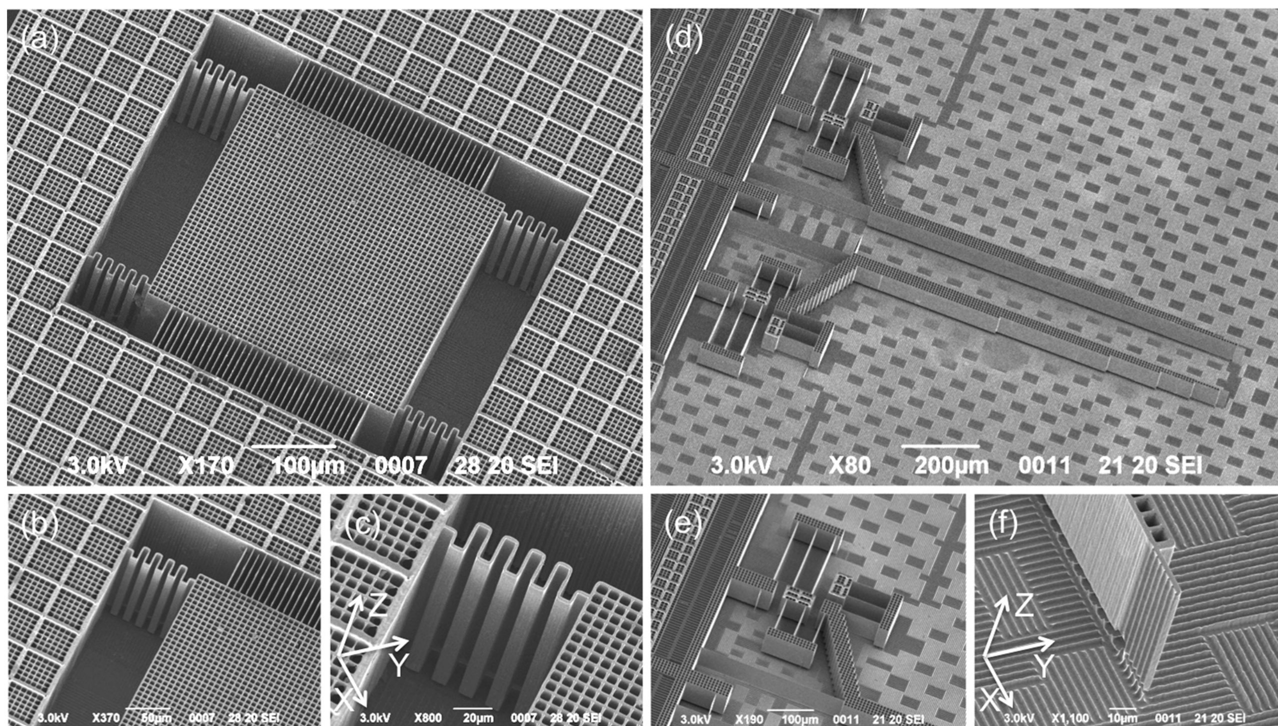

Figure 1. a–f) ECM-fabricated microstructures and microsystems: SEM image of a MEMS structure consisting of an inertial, free-standing mass (340 μm × 340 μm × 130 μm) equipped with high-aspect-ratio comb-fingers and suspended by high-aspect-ratio folded springs (*AR* about 100 for both fingers and springs) that are fixed to an anchor structure composed of a 2D array of square holes (a); details at two different magnifications of the MEMS structure in panel (a) are shown in (b–c); one of the folded springs of the structure in panel (a), which clearly highlights the remarkable accuracy in microfabrication by ECM at such high aspect-ratio values (c); SEM image of a mechanical microgripper consisting of two fingers (length of 1 mm and thickness of 70 μm), electrically actuable by means of comb-finger batteries driving a spring system, which allows rotation of the two fingers to be performed symmetrically (d); detail of the spring system exploited to allow symmetric rotation of the two microgripper fingers (e); and detail of one of the microgripper finger's tip provided with a sub-micrometer artificial surface ripple with the aim of increasing the grasping capability of the gripper (f).

© 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

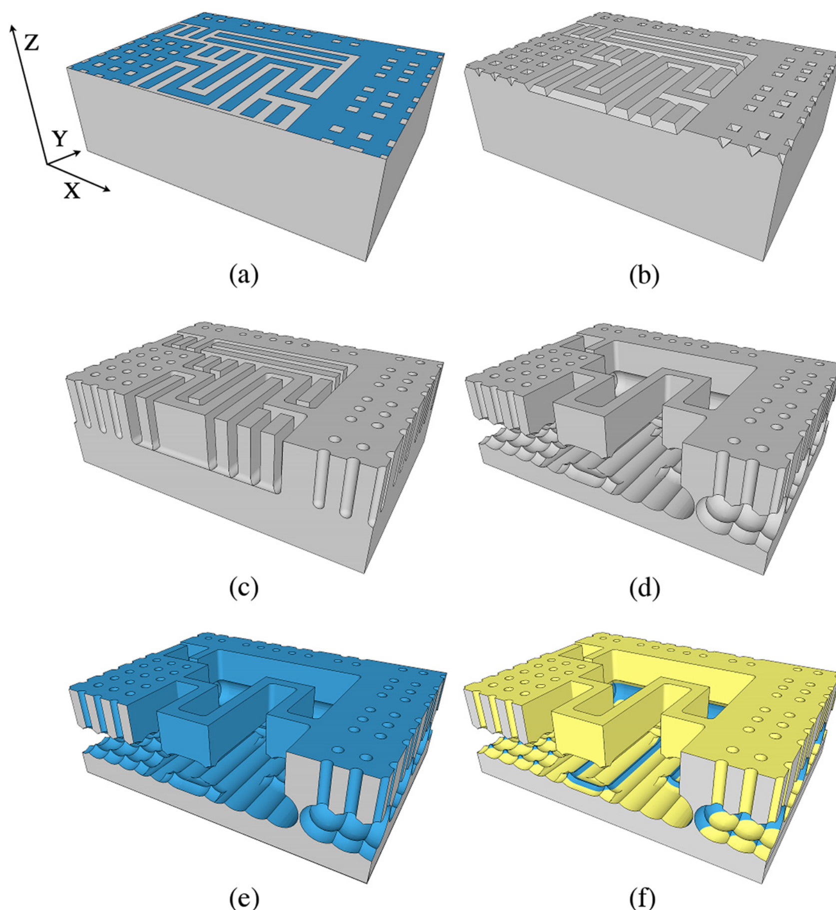

Figure 2. a–f) The main technological steps for the fabrication of microstructures and microsystems by ECM technology: definition of the microstructure layout on the silicon dioxide layer, which is on top of the n -doped silicon substrate, by BHF etching (a); replication of the microstructure layout into the silicon surface by KOH etching (seed-point formation) (b); anisotropic phase of the electrochemical etching step, used to etch the microstructure layout deep into the silicon substrate and create high-aspect-ratio microstructures (c); isotropic phase of the electrochemical etching step, used to release part of the etched microstructures from the substrate and, eventually, yield them to be free-standing (d); conformal growth by thermal oxidation of a silicon dioxide film to be used as an insulation layer (e); and quasi-conformal deposition by sputtering of a metal film for electrical actuation and/or sensing (f). The last two technological steps (e,f) outline a feasible option for providing ECM microfabricated structures with electrical actuation/sensing, according to the SCREAM approach.[20]

and electrochemical) technology reported so far, and certainly comparable with state-of-the-art dry etching technologies. In spite of such high complexity, the uniformity over large areas, the accuracy at the microscale and the surface finishing (roughness estimated by optical measurements of the order of 20 nm) of structures microfabricated by ECM technology are superior to dry etching tools at such high-aspect-ratio values.

Fabrication of microstructures and microsystems by ECM technology is carried out according to the following main technological steps, which are sketched in **Figure 2** with specific reference to the microstructure in Figure 1a–c. The starting material is n-type silicon, of orientation (100), with a thin silicon dioxide layer on top. The pattern of the microstructure to be fabricated is defined on a photoresist layer by standard lithography, transferred to the silicon dioxide layer by buffered HF (BHF) etching through the photoresist mask (Figure 2a), replicated (seed-point formation) into the silicon surface by potassium hydroxide (KOH) etching through the silicon dioxide mask (Figure 2b), and finally grooved into the bulk material by BIEE. The BIEE consists of a single etching step with an initial anisotropic phase (Figure 2c), used to etch the seed pattern deep into the substrate and create high-aspect-ratio microstructures, and a final isotropic phase (Figure 2d), used to release part of the etched microstructures from the substrate and, eventually, yield them to be free-standing. A further thermal oxidation step can also be performed to grow a 100 nm-thick conformal silicon dioxide layer (Figure 2e), to be used as an insulation layer, on which a metal contact for actuation and/or sensing can be deposited by quasi-conformal metal sputtering (Figure 2f), according to the single-crystal reactive etching and metallization (SCREAM) process.[20] The last two technological steps (Figure 2e,f) outline a feasible option for providing the microfabricated structures with electrical actuation/sensing, as already demonstrated in the literature for other bulk technologies;[20] this option will be not further discussed in this paper, which is focused on advanced silicon microstructuring by ECM. In Figure S2, Supporting Information, thermal oxidation is exploited to grow a silicon dioxide layer thick enough to produce stress-induced displacement of several fabricated MEMS structures, similar to that reported in Figure 1a–c, from their rest position, thus giving a perceptive proof-of-concept of their actuation.

As schematically shown in Figure 2, ECM makes use of both functional and sacrificial structures for the fabrication of advanced silicon microstructures and microsystems. Functional structures are, by definition, the parts of the microsystem that are anchored (partially, at least) to the silicon substrate after the isotropic phase of the electrochemical etching step; sacrificial structures are, by definition, the parts that are not anchored to the silicon substrate after the isotropic phase of the electrochemical etching step and that are, hence, removed. The former are indeed functional to the microsystem operation, while the latter are sacrificed for accurate microsystem fabrication. All of the microsystem parts visible in the SEM images of Figure 1 are functional structures, still connected to the substrate through anchor structures that were properly designed to withstand the isotropic phase of the etching; there are no sacrificial structures visible in Figure 1, as they were designed to be effectively removed during the isotropic phase of the electrochemical etching step. Figure 1f clearly shows the effect of the isotropic phase of the electrochemical etching step on both the functional and the sacrificial structures: the

© 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

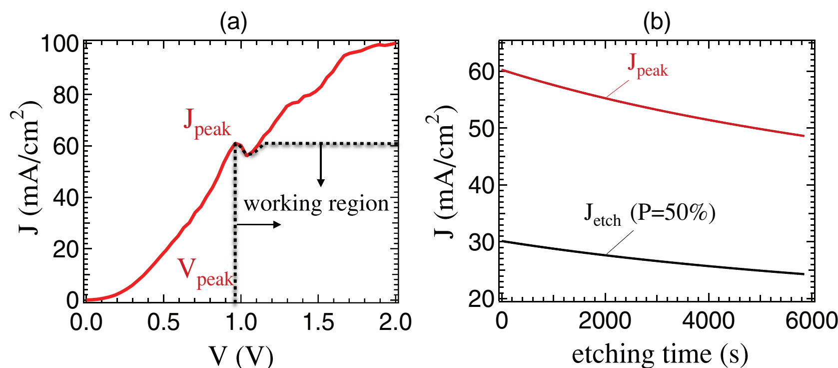

Figure 3. a–b) ECM working conditions: typical J–V anodic curve, for a flat silicon electrode in contact with an aqueous electrolyte containing 5 vol% HF under high-intensity illumination of the silicon back-side, highlighting the ECM working region: $J_{etch} < J_{peak}$ and $V_{etch} > V_{peak}$ (a); and the theoretical, non-linear decrease of the current density peak value, J_{peak}, with time for the microstructured electrodes and the etching current density value, J_{etch}, versus etching time needed to maintain the J_{etch}/J_{peak} ratio at a constant value of $P = 0.5$ over time, thus allowing the etching process to be perfectly anisotropic (b).

finger tip becomes free-standing after the isotropic phase, though anchored to the substrate through the gripper structure (Figure 1e), while the sacrificial structures around the finger tip are removed after the isotropic phase, leaving a characteristic ripple on the bottom surface. The use of sacrificial structures allows the simultaneous etching of both small (features of a few micrometers in size) and large (length of several millimeters) areas to be performed at the same rate and with the same accuracy, thus eliminating lag-effect problems of silicon areas with different aspect-ratios, which is a major problem of dry etching technologies.

3. ECM Anisotropy/Isotropy Tunability

The key role in ECM technology is played by the BIEE, which allows the silicon dissolution to be finely controlled at the submicrometer scale in the X–Y plane up to etching depths of hundreds of micrometers in the Z-direction. In particular, BIEE makes use of n-type substrates and back-side illumination to enable silicon dissolution in HF-aqueous electrolytes, a hole-activated process under anodic polarization of silicon, only where the seed points on the silicon surface are defined by KOH replication of the layout pattern.[8,13] Sub-micrometer control of the silicon dissolution at the seed sites, in the X-Y plane and along the Z-direction, is obtained by properly modulating both the etching current density, J_{etch}, and the etching voltage, V_{etch}, as the etch progresses. The J_{etch} and V_{etch} values are kept within the working region: $J_{etch} < J_{peak}$ and $V_{etch} > V_{peak}$; J_{peak} and V_{peak} represent the values of the current density and voltage of the electropolishing peak of the electrochemical system under investigation.[8,21] **Figure 3**a shows a part of the typical J–V anodic curve of a flat n-type silicon electrode in contact with an aqueous electrolyte containing 5 vol% HF, under back-side, high-intensity illumination. The J–V curve of Figure 3a represents the maximum value of the photogenerated current density as a function of the anodic voltage value, from which J_{peak} and V_{peak} are univocally defined for the electrochemical system under investigation. All of the current density–voltage pairs (J_{etch}, V_{etch}) in the area under the J–V curve of Figure 3a are addressed by properly tuning the illumination intensity of the silicon electrode, which allows the J_{etch} value to be set independently of the V_{etch} value in the working region. The J_{peak} value is proportional to $C_{HF}^{1.5}$, where C_{HF} is the HF concentration at the active silicon/electrolyte interface. C_{HF}, which represents the bulk electrolyte concentration for the flat electrodes, decreases non-linearly with etching depth and, in turn, with the etching time for microstructured electrodes. As a consequence, the J_{peak} value also decreases non-linearly with etching depth and time for microstructured silicon electrodes (Figure 3b).[22] In the working region, the silicon mass dissolved per unit time around a given X-Y position is proportional to the ratio J_{etch}/J_{peak} (also known as the porosity P), for any etching depth; the J_{peak} value also determines the etching rate in the Z-direction, which is, indeed, proportional to J_{peak}.[8,22]

The silicon dissolution (in terms of both volume and isotropy versus time) is finely tuned as the etching progresses by properly controlling the J_{etch} value over time. On the one hand, if the J_{etch} value is slowly reduced over time according to HF-diffusion kinetics, it is possible to compensate for the slight reduction of the J_{peak} value with etching depth, so that by maintaining the J_{etch}/J_{peak} ratio constant over time (Figure 3b), the etching results to be perfectly anisotropic and, in turn, micromachined structures with excellent straight walls are achieved. The reduction of J_{peak} with etching depth is caused by a reduction in C_{HF} inside the etched trenches, due to stationary diffusion of HF molecules from the top to the bottom of the etched structures. On the other hand, if the J_{etch} value is suddenly increased over time with respect to the HF diffusion kinetics, a dramatic decrease of the J_{peak} value occurs, which dynamically increases the J_{etch}/J_{peak} ratio, and, in turn, the silicon mass dissolved per unit time. A higher number of HF molecules per unit time, with respect to that supplied by stationary diffusion, is consumed at the bottom of the etched trenches as a consequence of the sudden increase of the J_{etch} value. The excess of HF molecule consumption leads to a dynamic reduction of the C_{HF} value and, in turn, of the J_{peak} value at the bottom of the etched trenches. The etching rate in the Z-direction, being proportional to J_{peak}, is therefore reduced, and the increased mass of silicon removed per unit time, J_{etch}/J_{peak}, mainly occurs in the X and Y directions, thus switching the etching from anisotropic to isotropic.

Figure 4a shows the typical experimental etching current density, J_{etch}, (left axis) and etching voltage, V_{etch}, (right axis) versus time, used for fabricating the microstructures of Figure 1a–c, for both the anisotropic and isotropic phases of the electrochemical etching step. During the anisotropic phase, the J_{etch} value is non-linearly reduced to compensate for the reduction of the C_{HF} value with etching depth. The etching voltage, V_{etch}, is linearly decreased over time in

© 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

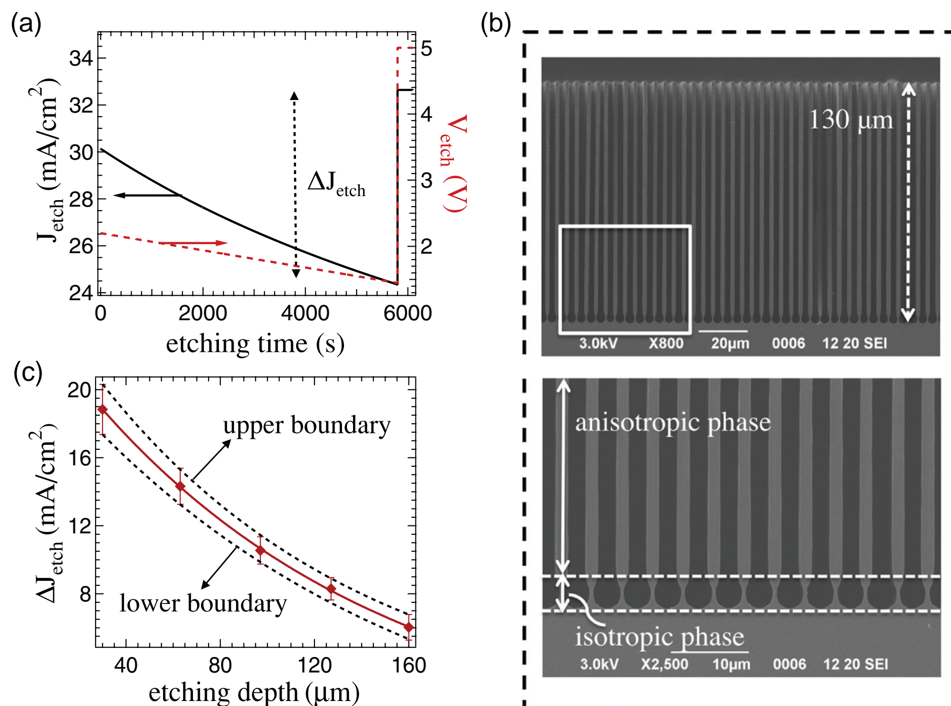

Figure 4. a–c) ECM anisotropy/isotropy tunability: typical experimental etching current density, J_{etch}, (left axis) and etching voltage, V_{etch}, (right axis) versus time, used for fabricating the microstructures of Figure 1a–c, both for the anisotropic and isotropic phases of the electrochemical etching step (a); SEM images, at different magnifications, of the sacrificial structures after the electrochemical etching step, highlighting the effect of both the anisotropic and isotropic phases (b); and optimum values for the current density step, ΔJ_{etch}, that allow the isotropic dissolution of silicon to be controlled carefully at the bottom of the etched trenches, as a function of the etching depth (c). The bars around the optimum ΔJ_{etch} values in panel (c) indicate the current density variation range (minimum and maximum ΔJ_{etch} values) for which isotropic etching can be successfully controlled for the detachment from the silicon substrate of both functional (free-standing) and sacrificial structures.

order to perform a first-order compensation of the voltage drop V_j at the silicon/electrolyte junction, which tends to increase due to the reduction of the etching current density ($V_j = V_{etch} - ARJ_{etch}$, with A being the area of the silicon surface in contact with the electrolyte and R the total resistance in series to the silicon/electrolyte junction). The etching anisotropy is nearly ideal in this phase, with an anisotropy percentage error over a depth of 100 μm of about 0.04%, measured from SEM observations. When the chosen depth is reached (130 μm in this specific case), both J_{etch} and V_{etch} are instantly switched to a higher value, $V_{etch} + \Delta V_{etch}$ and $J_{etch} + \Delta J_{etch}$ respectively, in order to quickly consume most of the HF molecules at the bottom of the etched trenches and, in turn, decrease the etching rate in the Z-direction, thus enhancing the silicon dissolution rate in the X and Y directions. The etching voltage step, ΔV_{etch}, gives rise to a current burst, thanks to dynamic capacitive effects at the silicon/electrolyte interface, whose amplitude is roughly equal to $\Delta V_{etch}/R$ right after the step application, and which decreases exponentially towards zero with time. On the other hand, the photogenerated current variation, due to the low-pass filtering effect of the photo-electrochemical system, is zero right after the current-step application and exponentially increases with time up to its novel, steady-state value, ΔJ_{etch}. The capacitive current burst, $\Delta V_{etch}/R$, initially sustains the current density step, ΔJ_{etch}, needed for the dynamic isotropic etching of the silicon, thus limiting low pass filtering effects.

As an example, Figure 4b shows two SEM images, at different magnifications, of sacrificial structures after the electrochemical etching step, highlighting the effect of both the anisotropic and isotropic phases. In particular, in this example, the anisotropic phase was exploited to etch 130 μm-deep, straight trenches; the isotropic phase was stopped a few seconds before complete dissolution of the silicon stem between adjacent trenches in order to better highlight the effect of isotropic etching at the bottom of the etched structures. Figure 4c shows the optimum value of the current density variation, ΔJ_{etch}, which allows the isotropic dissolution of silicon to be carefully controlled at the bottom of the etched trenches, as a function of the etching depth. The data of Figure 4c, which were obtained from a large set of experiments, highlight that the current density step, ΔJ_{etch}, required to enable isotropic etching, decreases non-linearly with etching depth, in agreement with the non-linear reduction of C_{HF} with etching depth. The silicon mass per unit section that is isotropically dissolved at the bottom of the etched trenches depends on the actual etching density value multiplied by the duration of this phase (300 s in Figure 4a). For a given depth, the time duration of the isotropic phase is tuned to fully dissolve the silicon stem at the bottom of both the sacrificial structures and the free-standing functional structures, while only partially dissolving the silicon stem of the anchoring structures, which is, by design, sufficiently thick to withstand the isotropic phase of the etching

© 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

properly. The bars around the optimum ΔJ_{etch} values denote the current density variation range (minimum and maximum ΔJ_{etch} values) for which the isotropic etching can be successfully controlled for the detachment of both the functional (free-standing) and sacrificial structures from the silicon substrate. ΔJ_{etch} values below the lower boundary in Figure 4c give rise to an incomplete detachment of the etched structures, which is independent of the time duration of the isotropic phase; ΔJ_{etch} values above the upper boundary in Figure 4c produce a non-homogeneous detachment, also associated with a partial erosion of the fabricated microstructures.

4. Conclusions

In this work, for the first time, the fabrication of high-complexity silicon microstructures and microsystems with sub-micrometer accuracy at aspect-ratio values (about 100) well beyond any up-to-date, both wet and dry technologies has been demonstrated by using a low-cost electrochemical micromachining technology, namely ECM. Among its main features, ECM technology encompasses: i) feasible structures with a high aspect ratio, which can easily be at least 100, three times higher than the better, deep etching techniques used so far for microsystem fabrication; ii) the possibility of changing the etching anisotropy (from zero to one) as the etching progresses, which enables 3D free-standing microstructure fabrication by one-step etching; iii) the possibility of finely controlling the etching features at the sub-micrometer scale, for both small (features down to 1 micrometer in size) and large (length over 1 mm) areas; iv) a high quality of etched structures in terms of anisotropy (percentage error over a depth of 100 μm of about 0.04%) and surface roughness (about 20 nm). World-wide dissemination of ECM technology at the lab-scale for silicon microstructuring can be easily envisaged in the near future, with a high-potential impact on, though not limited to, the broad field of microelectronics and microfabrication.

5. Experimental Section

Design Rules: The layout design of the microstructures and microsystems fabricated by ECM technology was carried out according to the following main rules: 1) the porosity of the whole patterned silicon area was maintained around an average value of 0.5; 2) after the functional structures had been properly designed, the remaining silicon area was partitioned with sacrificial structures; 3) two layout elements, both for the structural and the sacrificial structures, were separated, by design, by a distance of a minimum dimension of 2 μm and a maximum dimension of 10 μm; 4) each layout element, both for the structural and sacrificial structures, by design, had a minimum width of 1 μm and a maximum width of 10 μm; 5) anchor structures were designed to include parts sufficiently larger than the sacrificial structures, in order to withstand the isotropic phase of the electrochemical etching step effectively; 6) the free-standing functional structures were designed to include parts no larger than the sacrificial structures, in order to become actually free-standing during the isotropic phase of the etching; 7) the sacrificial structures consisted of basic elements (i.e., a straight line with a suitable length and width), designed to become free-standing and, hence, to be removed during the isotropic phase of the electrochemical etching, which were arranged as 1D arrays of parallel lines, with the number of elements and the array orientation chosen to comply with issues 1 and 2.

For the sake of clarity, the design values of the structural and sacrificial structures used for the fabrication of the microstructures and microsystems in both Figure 1 and Figure S1 (Supporting Information) are provided below. As to the MEMS devices, the anchor structures consisted of a 2D repetition of a 6 × 6 square lattice of holes, having a side of 5.3 μm and a pitch of 6.8 μm, enclosed by a silicon frame with width of 8 μm. The inertial masses consisted of square lattices of holes of side 5.3 μm and pitch 6.8 μm. The straight and folded springs consisted of long and straight (up to 300 μm), or folded lines with a width of 2 μm. The comb fingers consisted of interdigitated silicon fingers of different lengths, with a width of 2 μm and a pitch from 4 μm up to 6 μm. The sacrificial structure basic elements had a width of 2 μm and were arranged with a pitch of 4 μm. Regarding the microgripper devices, the anchor structures consisted of a 2D repetition of a 3 × 3 square lattice, with holes having a side of 6 μm and a pitch of 8 μm that were enclosed by a silicon frame with a width of 10 μm; the movable, rigid parts of the microgrippers (e.g., the gripper fingers) consisted of an array of holes with a side of 6 μm and a pitch of 8 μm. The beam springs consisted of long (up to 500 μm), straight lines with a width of 2 μm. The comb-fingers consisted of interdigitated silicon fingers with a length of 40 μm, a width of 2 μm and a pitch of 4 μm. The sacrificial structure basic elements had a width of 2 μm and were arranged with a pitch of 4 μm.

Silicon Wafers: All of the experiments were carried out on n-type, CZ-grown silicon, of orientation (100), with a resistivity of 2.5–8.5 Ω cm (from MEMC). A 200 nm-thick layer of silicon dioxide was grown on the substrates by dry thermal oxidation in a pure-O_2 atmosphere at 1050 °C for 4h in a ThermoLyne 21100 tube furnace.

Pattern Definition: A Microposit S-1818 photoresist film (from Shipley) was deposited on the silicon wafer by spin-coating at 4000 rpm for 60 s and subsequently subject to soft-baking on a hot-plate at 115 °C for 90 s. A UV contact-lithography system (MJB3 Karl–Suss mask aligner) was used for the layout-pattern definition. The photoresist development and post-baking were carried out using 1:5 (by volume) Microposit developer 351:H_2O solution and a hot-plate at 115 °C for 90 s, respectively. Once the lithographic step was ended, the layout pattern was transferred to the silicon dioxide layer by wet etching in BHF solution for 120 s.

KOH Etching: The pattern was transferred to the silicon substrate by wet etching in a 25 wt% KOH solution, saturated with isopropyl alcohol to increase the etching uniformity, at 50 °C. The etching time was chosen as being long enough to obtain the formation of full-V grooves for all of the patterned geometries. The silicon dioxide layer, which was used as a masking layer during the alkaline etching, was removed afterwards by a wet etch in a 1:1 (by volume) HF (48%):ethanol (99.9%) solution.

Electrochemical Etching (BIEE): The experimental setup used for the electrochemical etching consisted of a polytetrafluoroethylene (PTFE) electrochemical cell with a volume of 400 cm^3. The front side of the silicon sample was in contact with the solution. The area of the sample exposed to the electrolyte was about 1.3 cm^2 and had a circular shape. The electrolyte composition was 5 vol% HF:95 vol% H_2O, with 1000 ppm of sodium lauryl sulfate (SLS) as a wetting agent. The surfactant was added to reduce the formation of hydrogen bubbles at the sample surface, thus enhancing etching uniformity. For the same reason, the solution was stirred during the anodization process. Back-side illumination of the silicon sample was performed using a 250 W halogen lamp that was positioned about 6 cm away from the sample, through a circular window (1.3 cm^2) in the metal electrode that was used to provide the electrical contact to the sample itself. A feedback loop, performed using a proportional-integral-derivative (PID) controller (Eurotherm 2604), allowed the lamp power, and thus the illumination intensity, to be changed in order to set the etching current density value properly as the etching progressed. An IR filter with a cut-off wavelength of 750 nm was placed between the lamp and the silicon sample in order to avoid carrier generation close to the silicon surface in contact with the electrolyte. A second feedback loop, also obtained using the same PID controller, allowed the working temperature to be maintained at 22 °C for the entire etching time. The cathode consisted of a platinum disk

© 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

in front of the silicon anode at a distance of 1 cm, whereas a platinum wire close to the silicon electrode, at a distance of about 2 mm, was used as a pseudoreference electrode. A Source Measure Unit (Keithley 2410 Source Meter) was used to apply the anodization voltage between the silicon sample and the reference electrode, and to monitor the etching current.

J–V curves of the electrochemical system under investigation were recorded under back-side, high-intensity illumination of the silicon electrode by driving the halogen lamp at its maximum power value (250 W).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Received: September 7, 2011
Revised: October 18, 2011
Published online: January 30, 2012

[1] Z. Fan, H. Razavi, J.-W. Do, A. Moriwaki, O. Ergen, Y.-L. Chueh, P. W. Leu, J. C. Ho, T. Takahashi, L. A. Reichertz, S. Neale, K. Yu, M. Wu, J. W. Ager, A. Javey, *Nat. Mater.* **2009**, *8*, 648.
[2] G. M. Whitesides, *Nature* **2006**, *442*, 368.
[3] K. Sakuma, P. S. Andry, C. K. Tsang, S. L. Wright, B. Dang, C. S. Patel, B. C. Webb, J. Maria, E. J. Sprogis, S. K. Kang, R. J. Polastre, R. R. Horton, J. U. Knickerbocker, *IBM J. Res. Dev.* **2008**, *52*, 611.
[4] B. Wu, A. Kumar, S. Pamarthy, *J. Appl. Phys.* **2010**, *108*, 051101.
[5] M. F. Aimi, M. P. Rao, N. C. MacDonald, A. S. Zuruzi, D. P. Bothman, *Nat. Mater.* **2004**, *3*, 103.
[6] D. Copic, S. J. Park, S. Tawfick, M. F. L. De Volder, J. A. Hart, *Lab Chip* **2011**, *11*, 1831.
[7] R. L. Smith, S. D. Collins, *J. Appl. Phys.* **1992**, *71*, R1.
[8] V. Lehmann, H. Föll, *J. Electrochem. Soc.* **1990**, *137*, 653.
[9] V. Lehmann, *J. Electrochem. Soc.* **1993**, *140*, 2836.
[10] H. Ohji, P. J. Trimp, P. J. French, *Sens. Actuators A* **1999**, *73*, 95.
[11] J. Carstensen, M. Christophersen, H. Föll, *Mater. Sci. Eng. B* **2000**, *69–70*, 23.
[12] G. Barillaro, A. Nannini, F. Pieri, *J. Electrochem. Soc.* **2002**, *149*, C180.
[13] G. Barillaro, A. Nannini, M. Piotto, *Sens. Actuators A* **2002**, *102*, 195.
[14] S. Matthias, F. Müller, J. Schilling, U. Gösele, *Appl. Phys. A* **2005**, *80*, 1391.
[15] M. Köhler, *Etching in Microsystem Technology*, Wiley-VCH, Weinheim-Germany **1999**, Ch. 3.
[16] S. Matthias, F. Müller, *Nature* **2003**, 424, 53.
[17] G. Barillaro, A. Diligenti, M. Benedetti, S. Merlo, *Appl. Phys. Lett.* **2006**, *89*, 151110.
[18] S. Ottow, V. Lehmann, H. Föll, *J. Electrochem. Soc.* **1996**, *143*, 385.
[19] B. E. Volland, H. Heerlein, I. W. Rangelow, *Microelectron. Eng.* **2002**, *61–62*, 1015.
[20] N. C. MacDonald, *Microelectron. Eng.* **1996**, *32*, 49.
[21] G. Barillaro, L. M. Strambini, *Electrochem. Commun.* **2010**, *12*, 1314.
[22] G. Barillaro, F. Pieri, *J. Appl. Phys.* **2005**, *97*, 116105.

© 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim