SISTEMI EMBEDDED

Course Presentation – Spring 2018

Federico Baronti

Dip. Ing. Informazione

Via G. Caruso, 16 – Stanza B-1-09

050 2217581 – federico.baronti@unipi.it

http://www.iet.unipi.it/f.baronti/

Office hours:

Friday 15-18. Please, contact me in advance before showing up.

Class Schedule

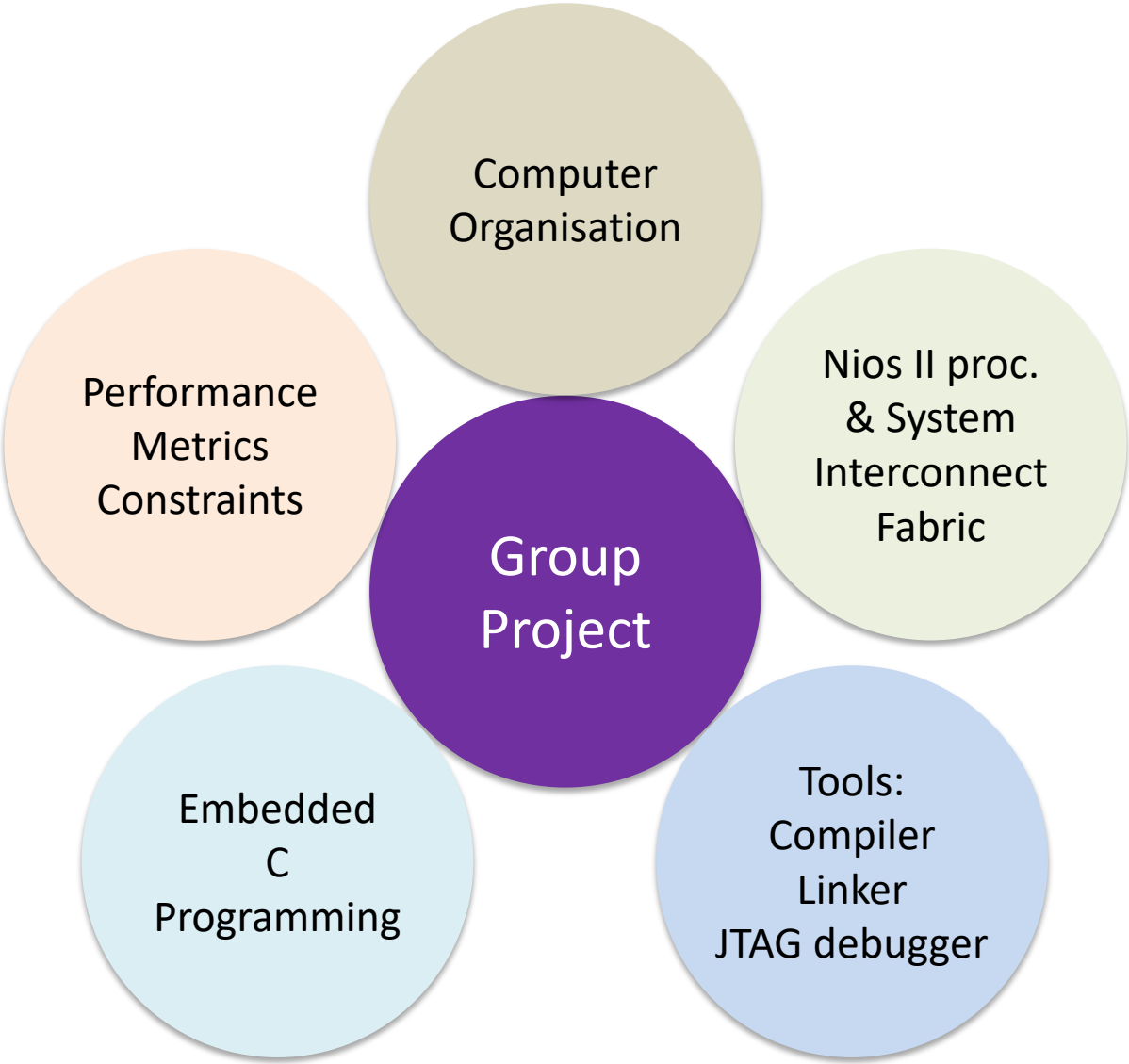
2M Elettronica						
	Lu	Ma	Me	Gi	Ve	Sa
8:30/9:30						
9:30/10:30	Nanoelettronica C33		Nanoelettronica C22			
10:30/11:30	Nanoelettronica C33		Nanoelettronica C22			
11:30/12:30	Nanoelettronica C33	Sistemi embedded B24	Sistemi di elaborazione SI 7			
12:30/13:30		Sistemi embedded B24	Sistemi di elaborazione SI 7			
13:30/14:30	Sistemi di elaborazione ADI1		Sistemi di elaborazione SI 7			
14:30/15:30	Sistemi di elaborazione ADI1	Nanoelettronica C41	Optional Lab			
15:30/16:30	Sistemi embedded ADI3 ex B26	Nanoelettronica C41	Sistemi embedded ADI3 ex B26			
16:30/17:30	Sistemi embedded ADI3 ex B26	Nanoelettronica C41	Sistemi embedded ADI3 ex B26			
17:30/18:30	Sistemi embedded ADI3 ex B26		Sistemi embedded ADI3 ex B26			

Course Objectives

Learn expertise and methodologies to design and program an embedded system

We'll use as a reference a **System on Programmable Chip (SoPC)** platform based on an Intel (formerly Altera) FPGA

Course Organization



Course Requirements

- Digital Electronics
- Digital Logic Design
  - HDL Coding
- Software Programming
  - Basic knowledge of C or C^{++} Language

Group Project

- Design an SoPC on an Intel Max 10 FPGA hosted on the Terasic DE10-Lite board
  - Computer implementation
    - May require the design of one or more custom peripherals
  - Software programming
- Project assignment during the 5th week
- See Projects of previous years to gather an idea

Course Material (1)

- Available at the course web page:

  http://http://www.iet.unipi.it/f.baronti/didattica/SE/2018/Sistemi Embedded.html
- Slides used during lectures
- Project templates/examples
- Text book:
  - C. Hamacher, Z. Vranesic, S. Zaky, N. Manjikian "Computer Organization and Embedded Systems," *McGraw-Hill International Edition*
- Documentation from Intel FPGA (Altera)

Course Material (2)

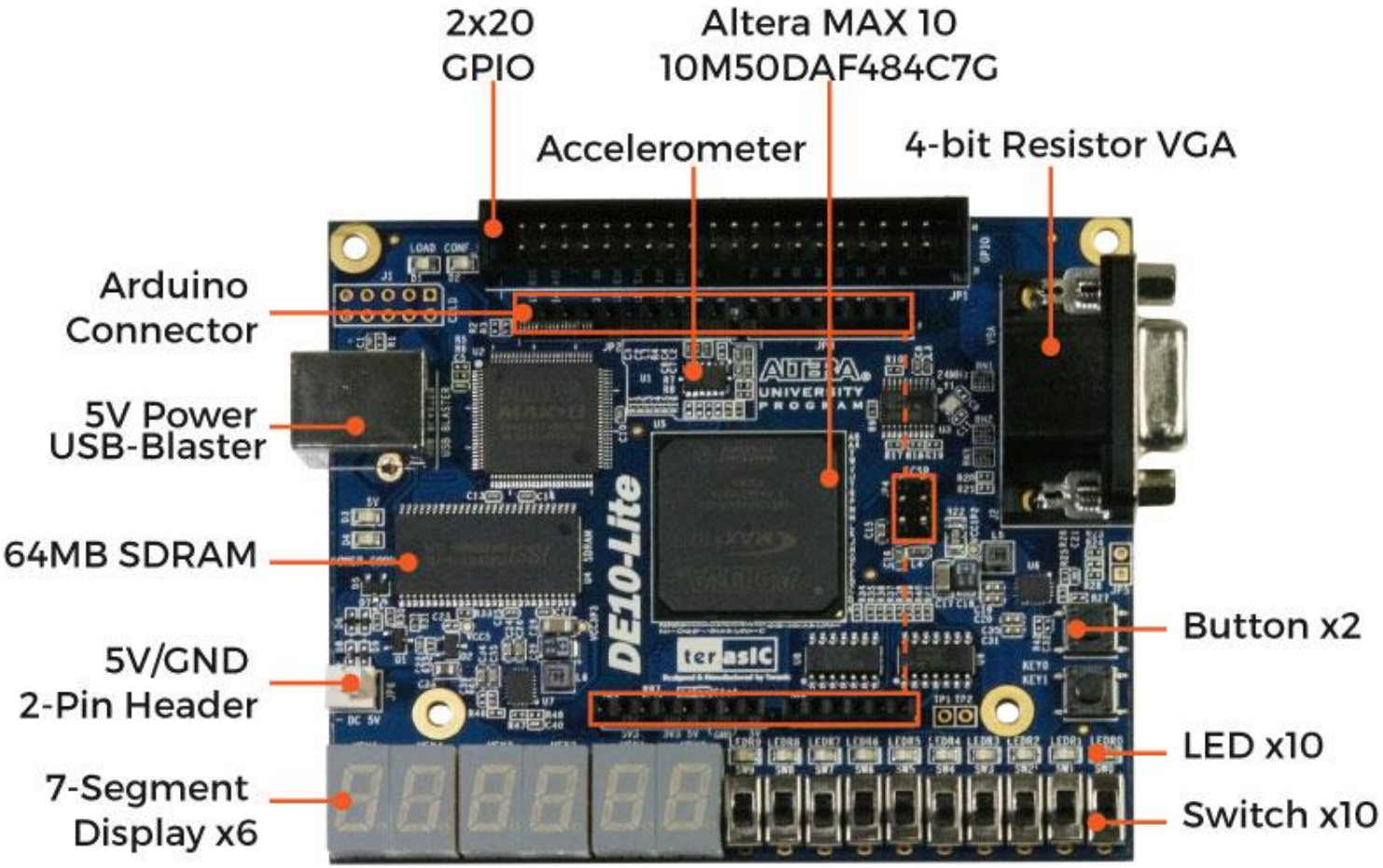
- Quartus Prime Lite Edition (16.1 update 2), with Max 10 Device Support
- University Program Installer (16.1)
- Nios II Documentation

Course Material (3)

- **14x** DE10-Lite: Development & Education board

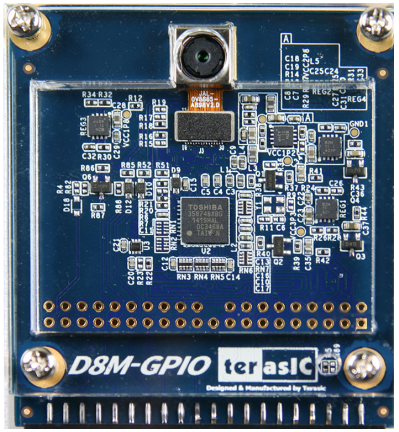
NEW

  - Intel Max 10 10M50DAF484C7G (50k LE; 1,638 Kb in M9K blocks)



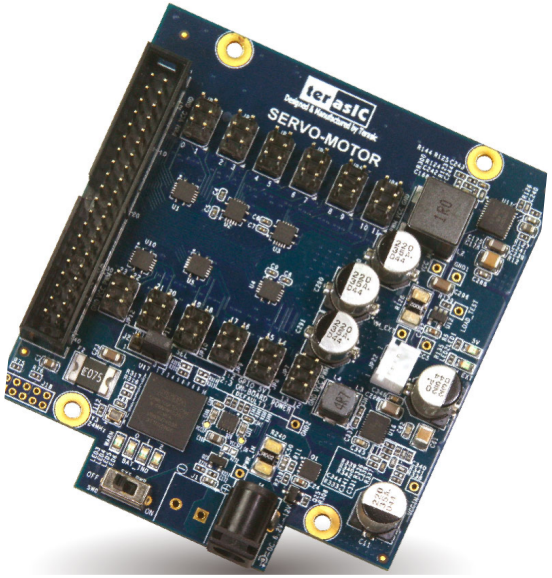
Course Material (4)

- 2x Touch display (LT24), 6x 8M Pixel Camera (D8M-GPIO), Multi-touch LCD Module Second Edition (MTL2), Servo Motor Kit (SVK)



MTL2

NEW



Exam Evaluation

- Project Evaluation (~40 %): the same marking for all the group members
  - Presentation and Demo (~30 %) - Due on last class
  - Project report (~70 %) – Due a “week” before the selected exam date
- Oral Test (~60 %)
  - Project discussion (~50 %)
  - Assessment of understanding and mastering the course contents (~50 %)