Power Amplifier Design for IEEE 802.11a Standard Using AMS 0.35 SiGe BiCMOS Technology

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***Abstract*—In this paper, different class power amplifiers (PA) are designed using different transistors available in the (AMS) 0.35µm SiGe BiCMOS HBT technology. These designs and evaluations will be based on first a basic DC simulation followed by a load-pull simulation.**

***Index Terms*—Class-A, Class-B, Power amplifier, SiGe.**

I. Introduction

Data communication using wireless networks such as IEEE 802.11 has found widespread use for the last few years. One of the critical components which allowed such common use of the technology can be attributed to the efficient and linear power amplifiers in the transmitter chain of the 802.11 transceivers. State-of-art power amplifier design has to be a highly efficient, high gain, ultra-linear, desired power output device while the device technology choice has also a crucial role [1]. In this study, a power amplifier design approach will be specified for IEEE 802.11a WLAN standard, and performance of different class PA will be specified in terms of power gain, PAE (power added efficiency), linearity, gain, output power.

IEEE 802.11a standard specifies the maximum power that can be transmitted in the Unlicensed National Information Infrastructure (UNII) band. These specifications are also the output power of the amplifier for frequency band of 5.18-5.8 GHz and specified as follows: 40mW (5.18-5.24GHz), 200mW (5.26-5.32GHz) and 800mW (5.74-5.8GHz).

II. Technology

The amplifier designs are based on AustriaMicroSystems (AMS) 0.35µm SiGe BiCMOS HBT technology which has an f_t of 40 GHz. In this work, seven different types of npn transistors are simulated. These transistors are symbolized as npn<c><b><e>h5 HBT which is suitable for high output voltage and power. The numbers in the symbol of the transistor <c>, <b>, and <e> refers to the number of contacts of collector, base and emitter, respectively. The typical breakdown voltages of collector-emitter and collector-base are 5.5V and 13V respectively. The capacitors and the inductors are the ideal devices defined by the process.

III. Circuit Design

We have evaluated PA as class A and B using different transistors in the AMS 0.35 um technology using Agilent Advanced Design System (ADS) environment.

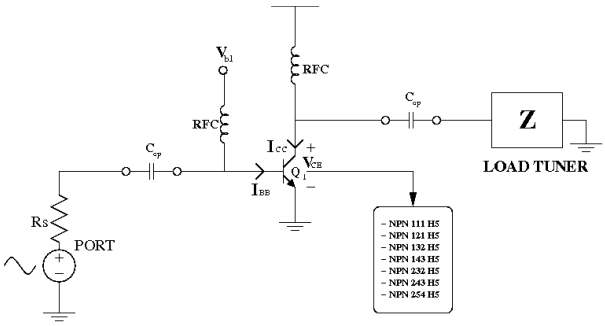

Figure 1- Schematic of the circuit for PAE and P_{out}

Figure 1 shows a generic PA circuit for optimum transistor analysis for each class/specifications [2]. Firstly, to obtain an initial design for the load impedance, transistors are DC simulated for optimum bias values for Class-A and B operation. The DC simulation results are shown in Figure 2, where V_{CE}-I_C curves for I_B values from 20µA to 200µA are plotted. For Class-A biasing, V_{CE} should be chosen at the midpoint of the voltage swing (marker m1). This point shows V_{CE} = 2.5V and I_C = 16.34mA. For Class-B biasing, V_{CE} = 2V and I_C = 20mA are chosen.

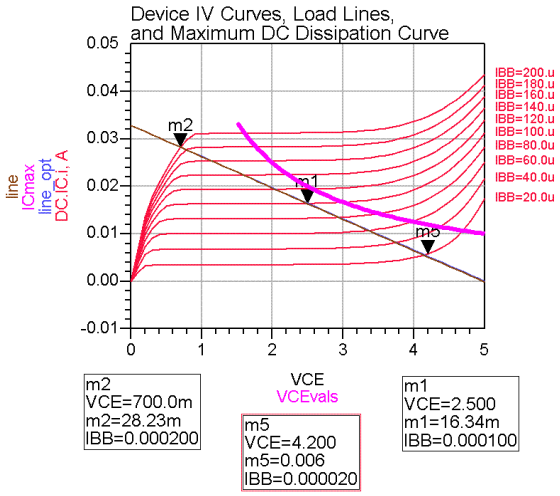

Figure 2- I-V curves for optimum biasing

There are seven different HBT transistors in this technology, classified based on their conductivity (power rating) and/or number of contacts at each terminals, as listed in Figure 1. To obtain the optimum load value for Class-A and Class-B,

simulations are done with the circuit shown in Figure 1. The capacitors on the base and collector are the by-pass capacitors and RF chokes are used for biasing. The output is terminated with variable load impedance for load-pull setup. These curves are obtained with seven different types of high-voltage HBT's in AMS technology. Due to different number of contacts at collector, base and emitters, series resistances and contact capacitances are different for each of these transistors. For Class-A bias values, $P_{out} = \frac{V_{CE}^{2}}{2R_{opt}}$. After the DC simulations, optimization of the load impedance is achieved through load-pull setup.

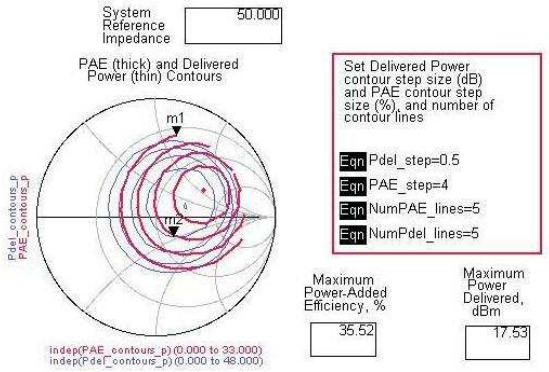

Figure 3- Max PAE and Pout circles

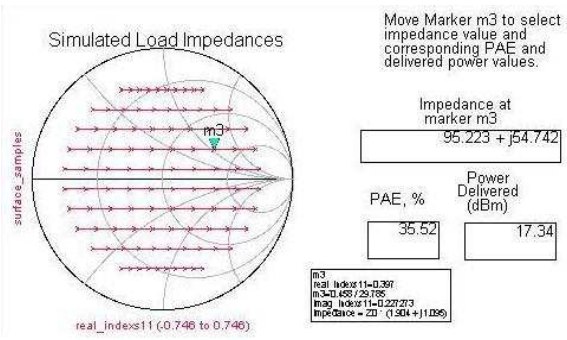

Figure 4- Load impedance for max PAE and Pout

In Figure 3, power and efficiency circles are shown on the smith chart and maximum PAE and P_{out} that can be obtained from this circuit are calculated. The simulated load impedances can be seen on the Smith Chart in Figure 4, where the optimum load impedance is shown which gives the maximum PAE and P_{out}. The load impedance of 95,223 + j54,742 Ohms gives 35.52% PAE and 17.34dBm output power. According to these results, output matching is done between this optimum impedance and 50Ω fix load.

These values are 35.52% and 17.53 dBm (56.62mW) respectively. This shows that the single stage amplifier is not sufficient for all frequency bands and for the output power and the gain, multi-stage amplifier design will be considered [3].

Finally, after deciding the optimum load impedance, output matching circuit is inserted into the circuit. Also, for input matching, the input resistance of the transistor is simulated and another matching is designed for input. The input and output ports' impedances are taken as 50Ω as shown in Figure 5. To decrease the number of components used and as a result of parasitics, the RF chokes are used as matching device which means their values are designed for matching.

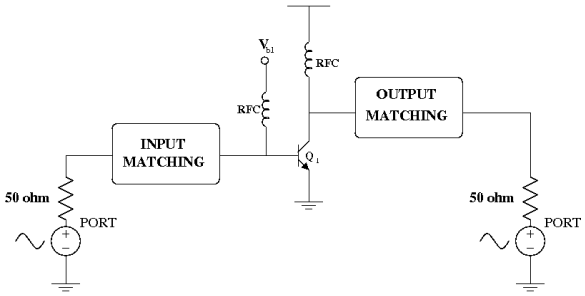

Figure 5- Power amplifier with matching circuits

IV. SIMULATION RESULTS

Figure 6 shows the transducer gain and Figure 7 shows PAE values for npn254h5 transistor which is simulated as class-A amplifier. The low-frequency gain for Class-A amplifier is about 17dB. As expected, gain decreases as output power increases. At 1dB compression point, gain is about 16dB at 10.07dBm output power. Conversely, PAE is directly proportional with output power and it takes its maximum value 20.04% at 15.3dBm output power. Also, P_{in}-P_{out} graphics can be seen in Figure 8. RF power means input power and at 20dBm, P_{out} becomes 17.24dBm. The other six different transistors are also simulated for Class-A amplifier, but the gain and PAE values are all lower than these shown in figures.

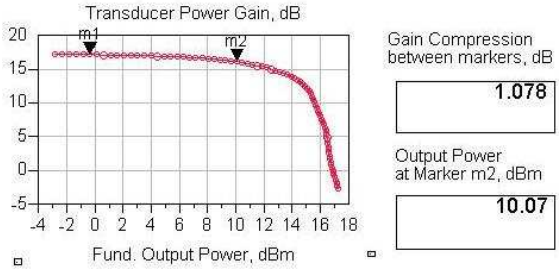

Figure 6- Class-A Power Gain

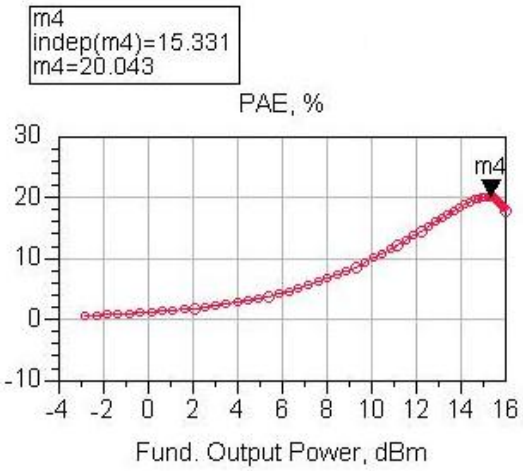

Figure 7- Class-A PAE

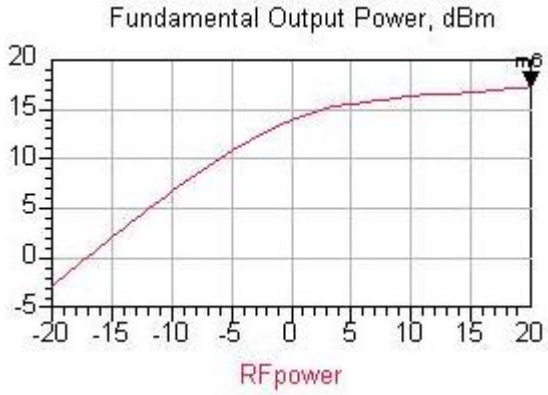

Figure 8- Class-A P_{in} vs. P_{out}

Class-B biasing is also simulated for all types of transistors. The best results are obtained with npn254h5 again. These results are shown in Figure 8, 9, and 10 which show power gain, PAE and P_{in}-P_{out} respectively. In Figure 9, maximum power gain is about 10dB at output power of 13.36dBm. The gain is not constant because of input matching. PAE has increased according to Class-A circuit which is shown in Figure 10. It takes the maximum value 27.16% at 14.81dBm output power. The linear region for P_{in}-P_{out} curve becomes narrower which can be seen in Figure 11. In the other hand, the maximum output power value 17.26dBm is nearly same as Class-A.

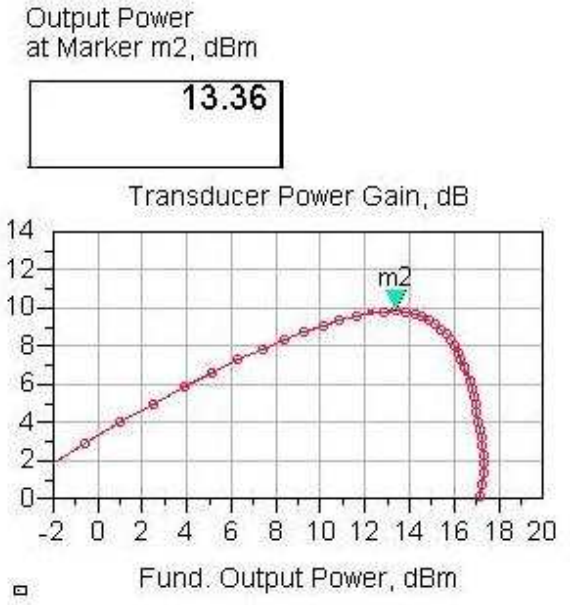

Figure 9- Class-B Power Gain

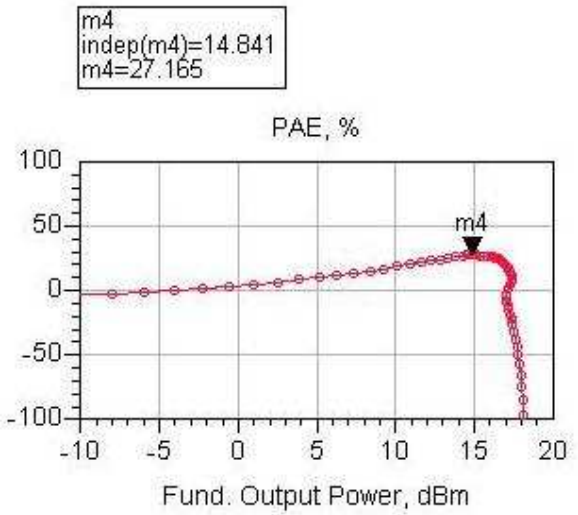

Figure 10- Class-B PAE

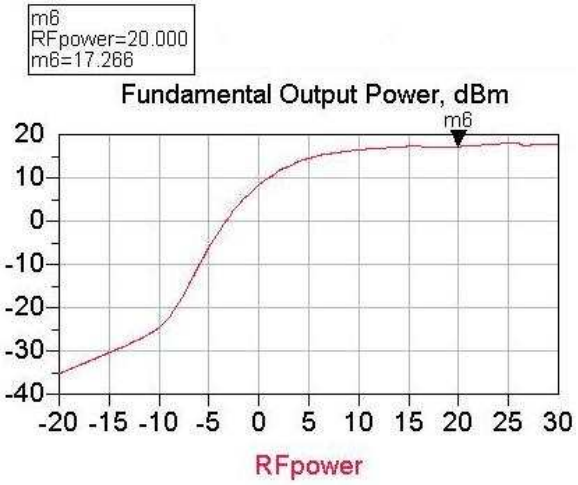

Figure 11- Class-B P_{in} vs. P_{out}

V. CONCLUSION

Class-A and Class-B power amplifiers are simulated at 5GHz using AMS 0.35µm SiGe HBT's to compare the performances of these transistors. Supply voltage is set to 3.3V which will be compatible to the other components of transceiver structure. Maximum performance is achieved with npn254h5 transistor for both classes.

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