Design of a LNA for 5.25 GHz in ams S35 CMOS Technology

Elettronica dei Sistemi Wireless report

Gabriele Ciarpi

Marc Marì

Introduction

The aim of this work is to design and compare a two-stage Low Noise Amplifier (LNA) for 5.25 GHz in 0.35 µm technology with two single-stage LNAs. The design of the LNA is made using ADS (Advanced Design System) CAD and the performances comparison are extracted by an 8-PSK communication system modelled in Matlab-Simulink.

1. LNA design

1.1. Single Stage LNA

This LNA is a cascode amplifier designed to obtain the lowest noise figure keeping the power consumption below 15 mW and 30 mW (5 mA and 10 mA supply currents). The mosfets size are project constraints and are 140 µm for MN1-MN2 and 10 µm for MN3.

The steps to design this amplifier are:

1. Choice Rref value to meet the power consumption constraint.
2. Sizing Ls and Lg to realize the integrated matching (Zin = 50 Ω). A first choice of the value is made using the Eq. (1) (f_t = 24 GHz, C_{gs} = 1.15 pF/mm) then the results are optimized with parametric simulations.

$$Z_{in} = L_s\omega_t + j\omega(L_s + L_g - \frac{1}{\omega^2 C_{gs}}) \quad (1)$$

3. Choice of Ld and Cd value to realize the output power matching.
4. Parameters extraction

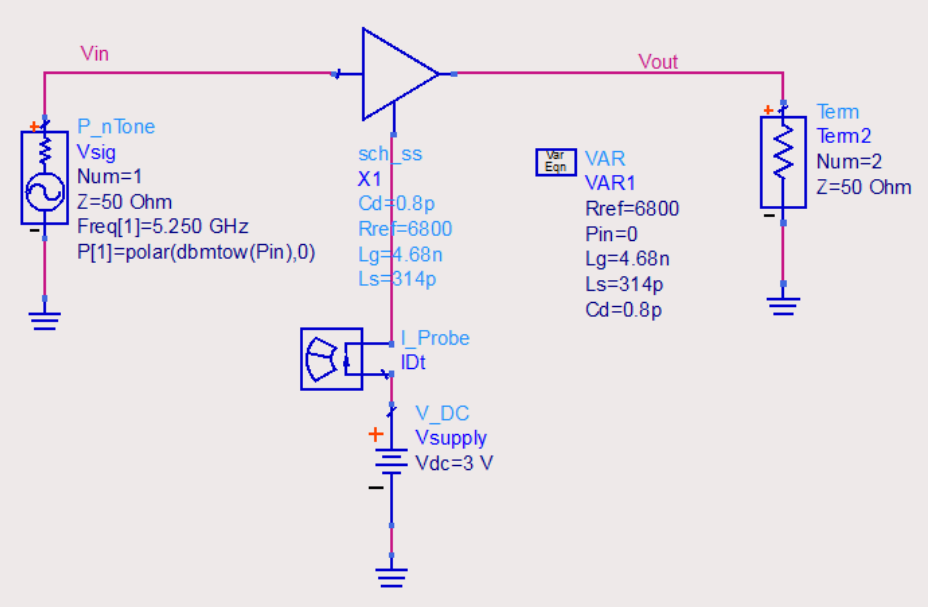

Fig. 1: Top level schematic

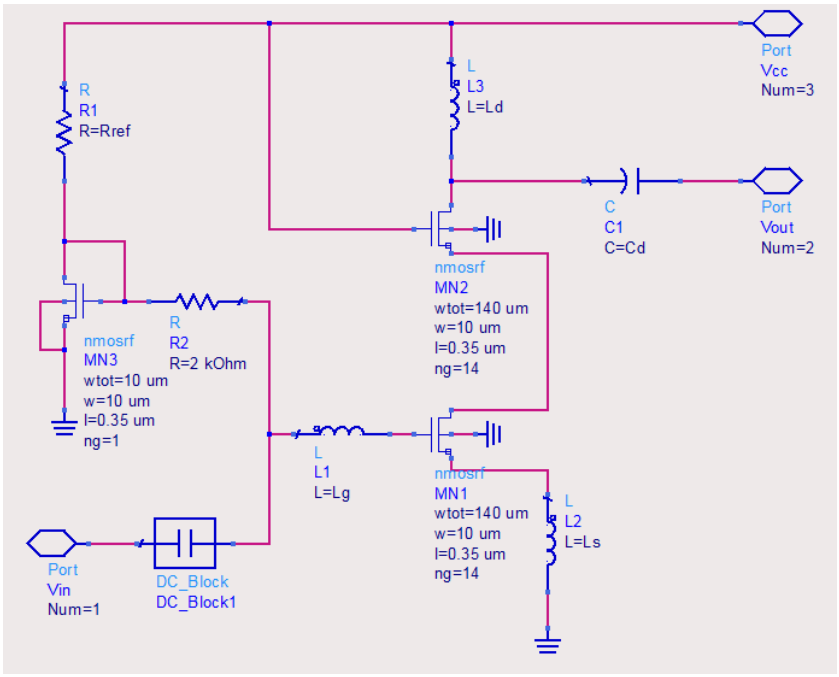

Fig. 2: Single stage LNA schematic

The features of this designed single stage LNA are listed in Table 1 for the two supply current constraints.

	Isupply = 5 mA	Isupply = 10 mA	Unity
MN1 & MN2 size	140	140	µm
MN3 size	10	10	µm
Rref	6800	2914	Ω
Ls	316	293	pH
Lg	4.5	4.39	nH
Ld	3.6	3.5	nH
Cd	0.144	0.147	pF

Zin	49.97 + j0.13	50.01 + j0.05	Ω
Zout	49.74 + i0.95	49.55 – j0.3	Ω
Zon	95.19 + j11.56	100.58 + j12.53	Ω
Gt	15.517	16.628	dB
NFmin	2.064	1.888	dB
NF	2.337	2.194	dB
iCP1dB	-15.13	-15.58	dBm
oCP1dB	-0.61	0.045	dBm
iIP3	0.861	0.197	dBm
oIP3	10.52	9.857	dBm
Saturation Power	10.66	16.374	dBm
Gain compression @ Psat	45.28	46.94	dBm

Table 1: Single stage LNA parameters

The S-parameters and Output power characteristics of the two LNAs are displayed in Fig. 3, Fig. 4, Fig. 5 and Fig. 6. The m1 cursor indicates the 1 dB compression point.

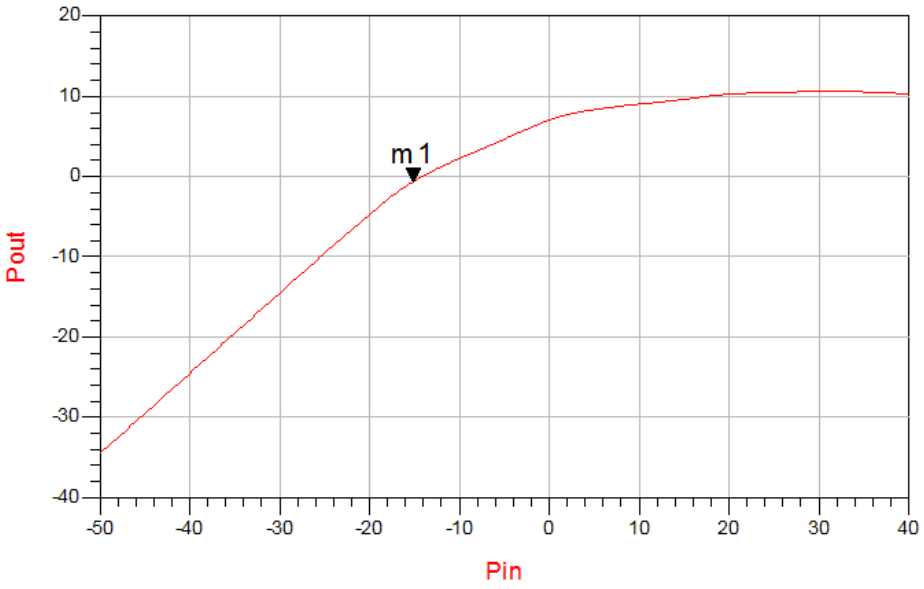

Fig. 3: Output power characteristic of single stage LNA @ 5 mA

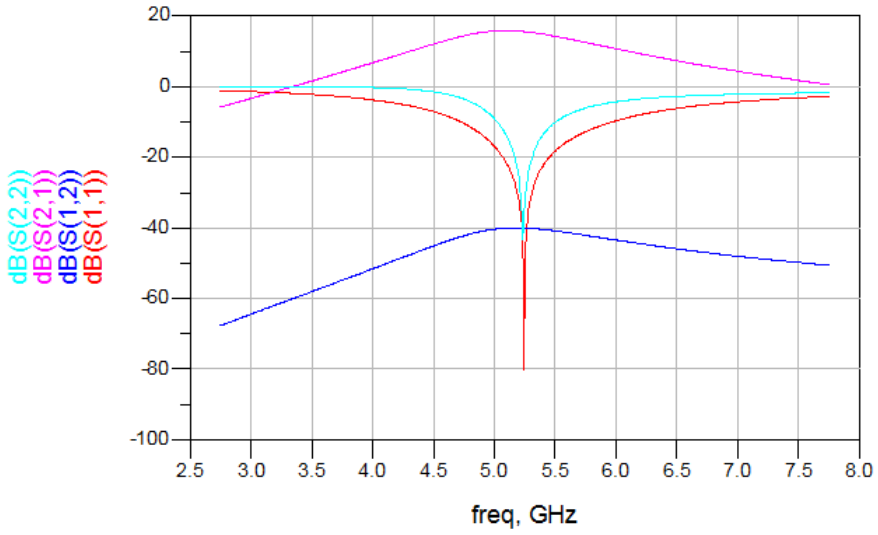

Fig. 4: S-parameters of single stage LNA @5 mA

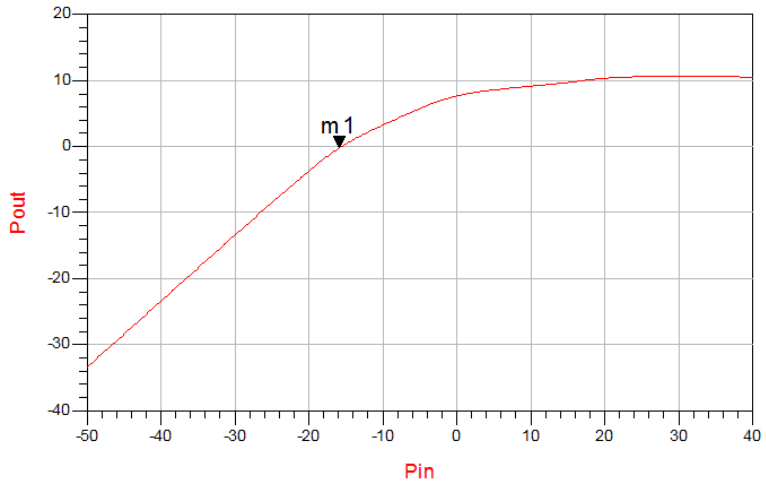

Fig. 5:Output power characteristic of single stage LNA @ 10 mA

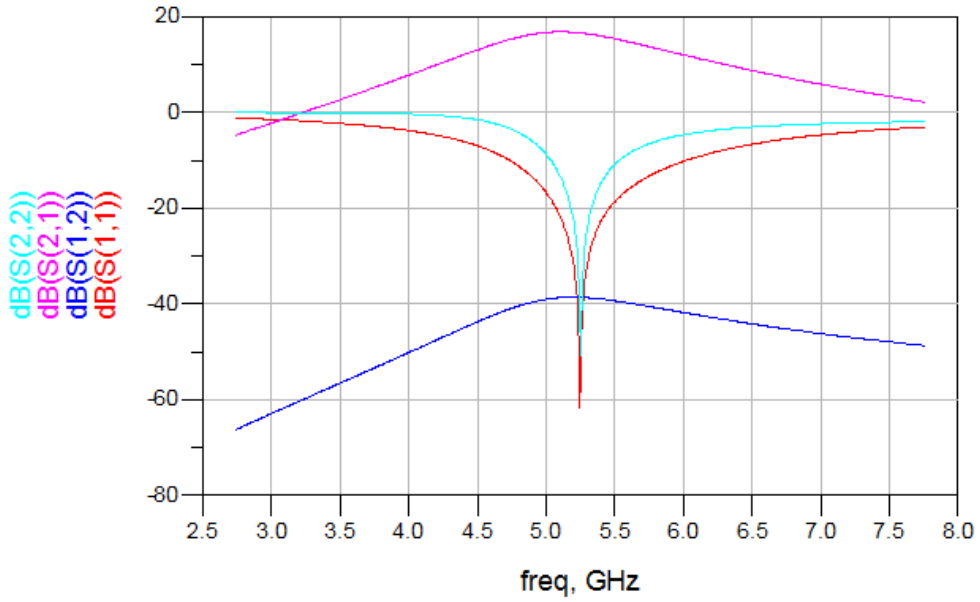

Fig. 6: S-parameters of single stage LNA @10 mA

1.2. Double Stage LNA

The design is focused on low noise figure, input and output impedances matching and high transducer power gain.

1.2.1. Polarization network

The double stage LNA (Fig. 7) is designed adding a second cascode stage at the single stage amplifier keeping the same power consumption constraint (30 mW) to compare this solution with the single stage.

The polarization network (Rref and MN3) fixes the polarization currents of the two amplifiers by a mirror configuration with ratio 1:14. The current used to polarize the amplifier can be calculated by Eq.(2). The two stages are supply with the same currents (5 mA) to compare the results with the single stage LNA at 5 mA.

$$I_{tot} = I_{Rres} + I_{MN2} + I_{MN5} = I_{Rres} + 14I_{Rres} + 14I_{Rres} = 29I_{Rres} \qquad (2)$$

Where the reference current is chosen using the Rref value Eq.(3).

$$I_{ref} = \frac{V_{cc} - V_{gs3}}{R_{ref}} \qquad (3)$$

Using a Vgs3 = 0.8 V the Rref value that meets the constraint is 6380 Ω, and by parametric simulation the value is fixed to 6610 Ω.

1.2.2. Integrated Matching

In CMOS technology the optimum noise and the input power matching conditions are very close together so both matching could be possible. The optimal noise impedance depends on technology parameters and MN1 (see Fig. 7) gain capacitance that is fixed by constraints (mosfet size if a constraint). The noise figure depends also on drain current density, high values of current should be used to obtain the best value. Since power consumption constraints, the current values in the first and second stage are about 5 mA to compare it with the already designed LNA.

Degenerating inductance in the source of the first stage produces a resistive term in the input impedance of MOS transistor that allow to obtain a 50 Ω input impedance keeping acceptable mos size value. The reactive part of the optimum noise impedance is zero and this is also the value wanted to power matching. Therefore the Lg element is added to delete this reactive component due to gate capacitance.

The input impedance can be expressed as Eq. (4) and Ls and Lg value are chosen to obtain the real impedance of 50 Ω.

$$Z_{in} = L_s\omega_t + j\omega\left(L_s + L_g - \frac{1}{\omega^2 C_{gs}}\right) \qquad (4)$$

Considering ω_t = 150.8 GHz and C_{gs} = 1.15 pF/mm the Ls and Lg value are respectively 331.56 pH and 5.38 nH. These values are then optimized with parametrical simulations.

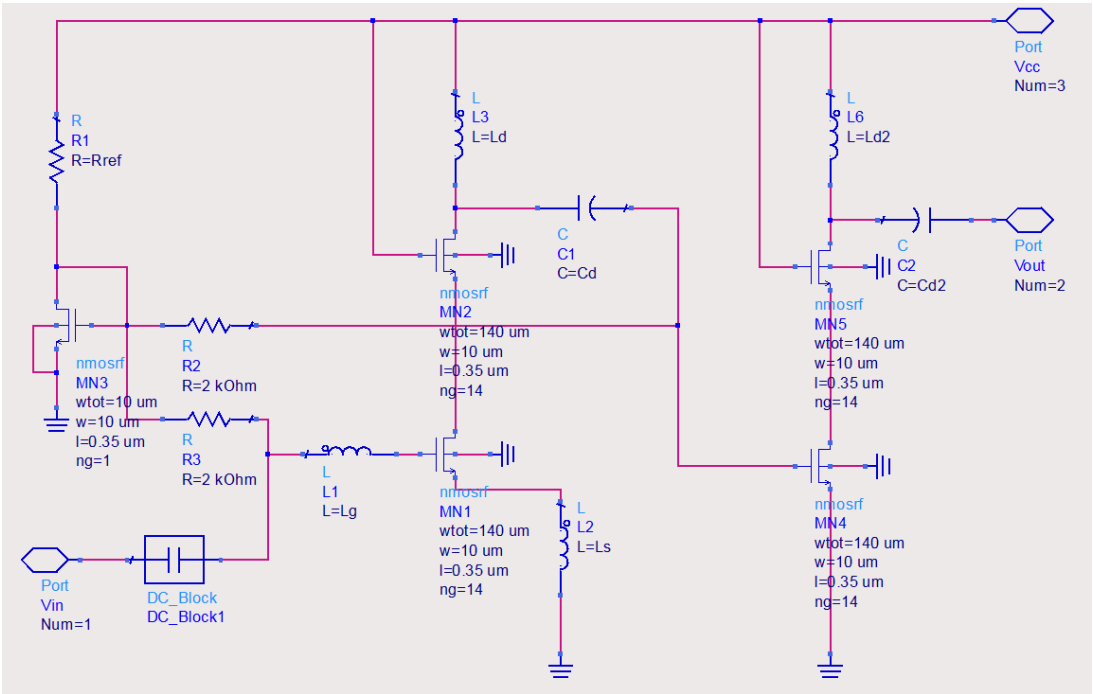

Fig. 7: Double stage LNA schematic

1.2.3. Matching networks

For the output network of the first and second stages we decided using a matching network to improve the transducer power gain (see Fig. 8).

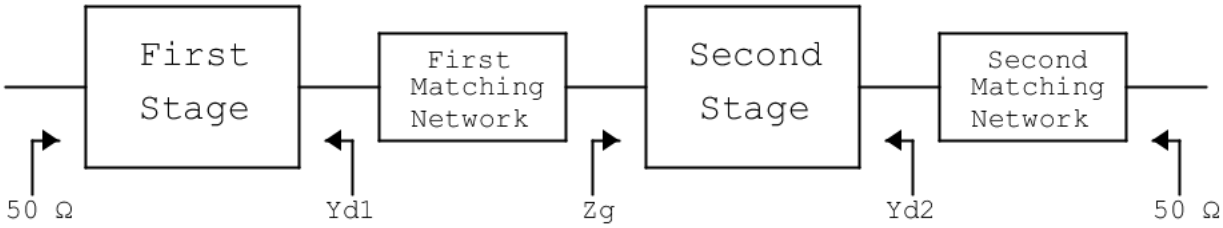

Fig. 8: LNA architetture

The networks are sized considering the admittance shows in the drains (Y_{d1}, Y_{d2}) of the common gate stage mosfets, the complex conjugate impedance shows in input of the second cascode stage (Z_g) and the standard load (50 Ω).

The matching network is a no-dissipative system so can be represented as reactances and susceptances.

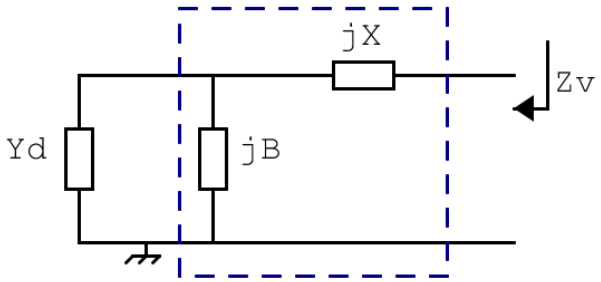

Fig. 9: Matching network

$$Z_v = R_v + jX_v = \frac{G_d}{G_d^2+(B+B_d)^2} - j\frac{B+B_d}{G_d^2+(B+B_d)^2} + jX \qquad (5)$$

The cascode amplifier architecture has a low S12 due to the presence of common gate stage, therefore the input impedance depend weakly on the load impedance. This feature can be used to size the system, therefore the network between the two stages is sized before of the output network.

For the first-stage matching network Zv (input impedance of the second stage) and Yd (admittance shows in the MN2 drain) are:

$$Y_{d1} = G_{d1} + jB_{d1} = 1.049\text{e-}3 + j3.973\text{e-}3\ S \qquad (6)$$

$$Z_g = R_g + jX_g = 44.95 - j267.7\ \Omega \qquad (7)$$

Since this, the matching network is sized as Fig. 7 with values Ld = 3.49 nH and Cd = 0.105 pF.

The second-stage matching network is sized as the previewer using Zv = 50 Ω and Yd is the admittance shows in the MN5 drain.

$$Y_{d2} = G_{d2} + jB_{d2} = 1.056\text{e-}3 + j3.953\text{e-}3\ S \qquad (8)$$

The results of this procedure are Ld2 = 3.6 nH and Cd2 = 0.143 pF (9)

1.2.4. Simulative Results

With parametric simulations the component values are optimized to obtain input and output power matching and to maximize the transducer power gain.

	Isupply = 10 mA	Unity
MN1, MN2, MN4, MN5 size	140	µm
MN3 size	10	µm
Rref	6610	Ω
Ls	258	pH
Lg	4.32	nH
Cd	0.23	pF
Ld	4.23	nH
Cd2	0.143	pF
Ld2	3.60	nH
Zin	50.030 + j0.133	Ω
Zout	50.113 – j0.044	Ω
Zon	92.523 + j16.073	Ω
Gt	32.31	dB
NFmin	2.097	dB
NF	2.367	dB
iCP1dB	-32.07	dBm
oCP1dB	-0.761	dBm
iIP3	0.933	dBm
oIP3	10.593	dBm
Saturation Power	7.63	dBm
Gain compression @ Psat	46.66	dBm

Table 2: two-stage LNA parameters

The IP3 is valued with two tones at 500 kHz from the main frequency with a power of -42 dBm.

Fig. 10 displays the no-linearity of the transducer power gain. The cursor m1 highlights the 1 dB compression point.

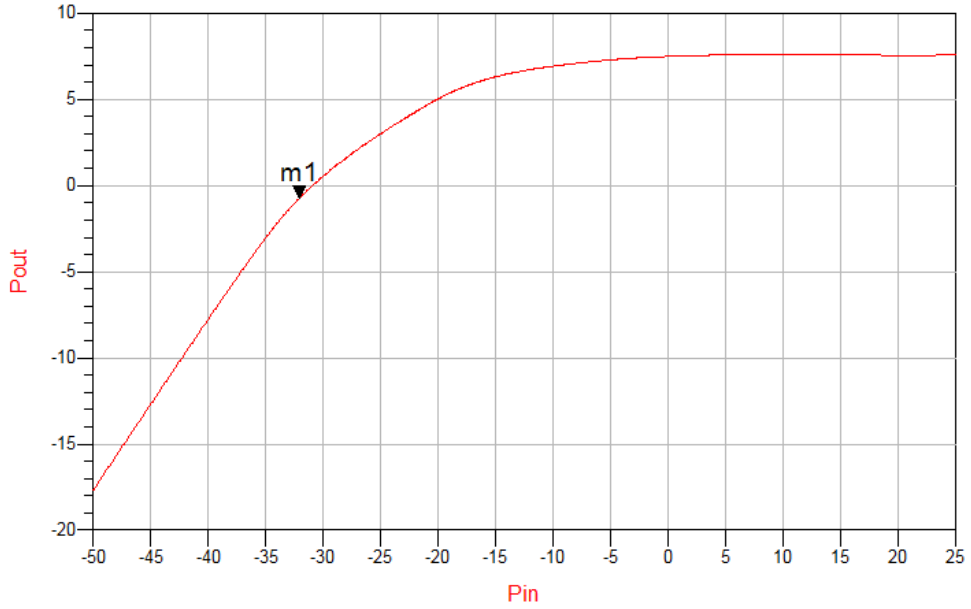

Fig. 10: Output Power characteristic

The frequency variation of the S-parameters of the two-stage LNA is showed in Fig. 11.

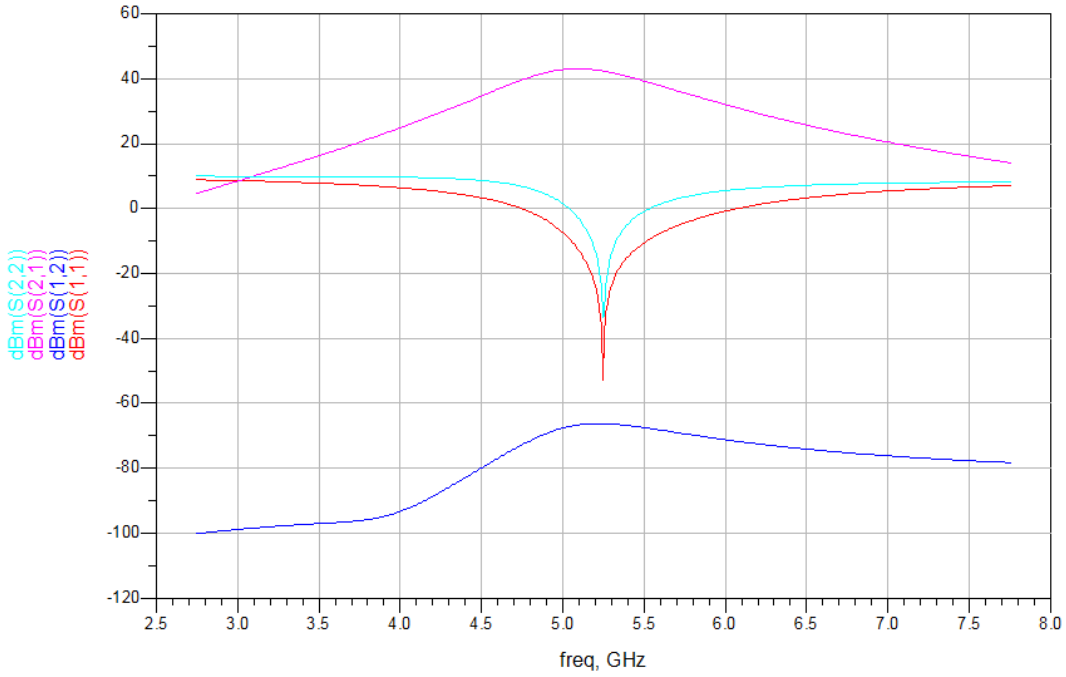

Fig. 11: S-parameters of double stage LNA

2. Transceiver model characterization (Matlab-Simulink)

The three LNAs (two single stage and a two-stage) are compared in a Matlab-model of a 5.25 GHz transceiver for 8-PSK communications.

The transmitter emits the signal at 5.25 GHz in a 1.07 MHz bandwidth with a power of about 5 dBm. The transmitter is placed at a variable distance from the receiver so a variable path loss is considered in the application test. The channel is modeled as a free space system and a thermal noise at 273 K is added at the signal.

A blocker, at 30 MHz from the signal frequency, is added at the received signal. Its power is fixed at -119.7 dBm.

If the receiver is placed at 100 m from the transmitter, the path loss is 87 dB so the power of the signal that arrives at the receiver is about -82 dBm.

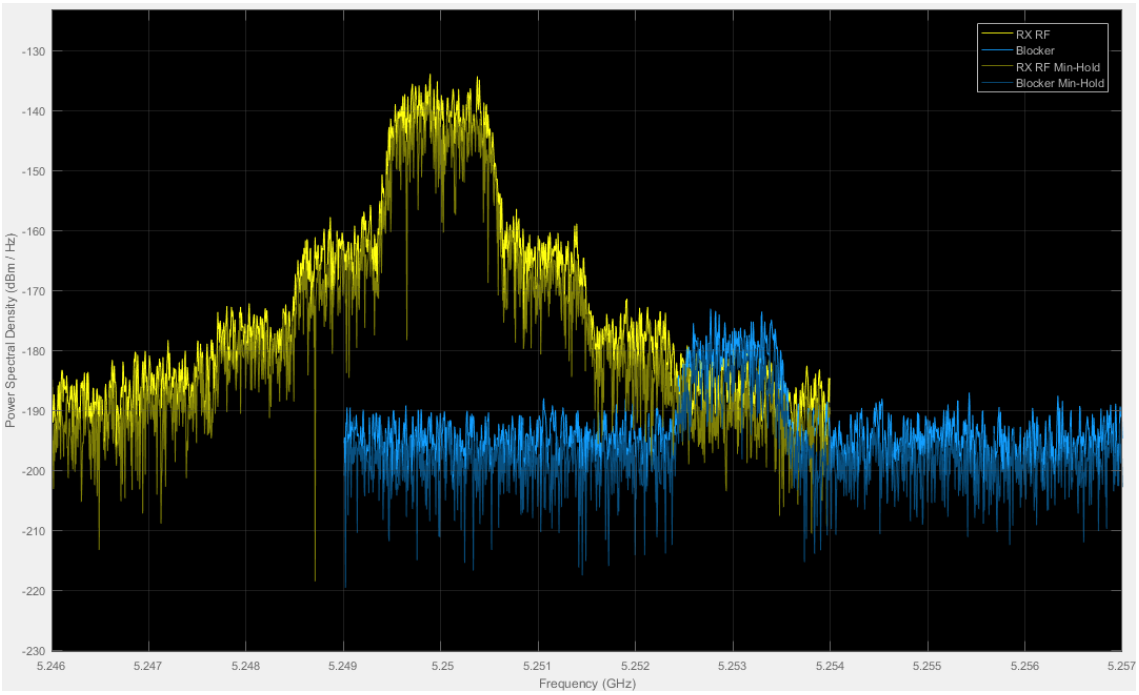

Fig. 12: Signal and noise spectrum @100m

The receiver implements a direct conversion architecture. It is made by antenna (0 dB gain), the designed LNA, I-Q mixers (reference [1]) and I-Q amplifiers (Fig. 13).

The features of the mixers used [1] are:

- Conversion Gain: 10.5 dB
- Noise Figure: 16.02 dB
- IIP3: 14 dBm

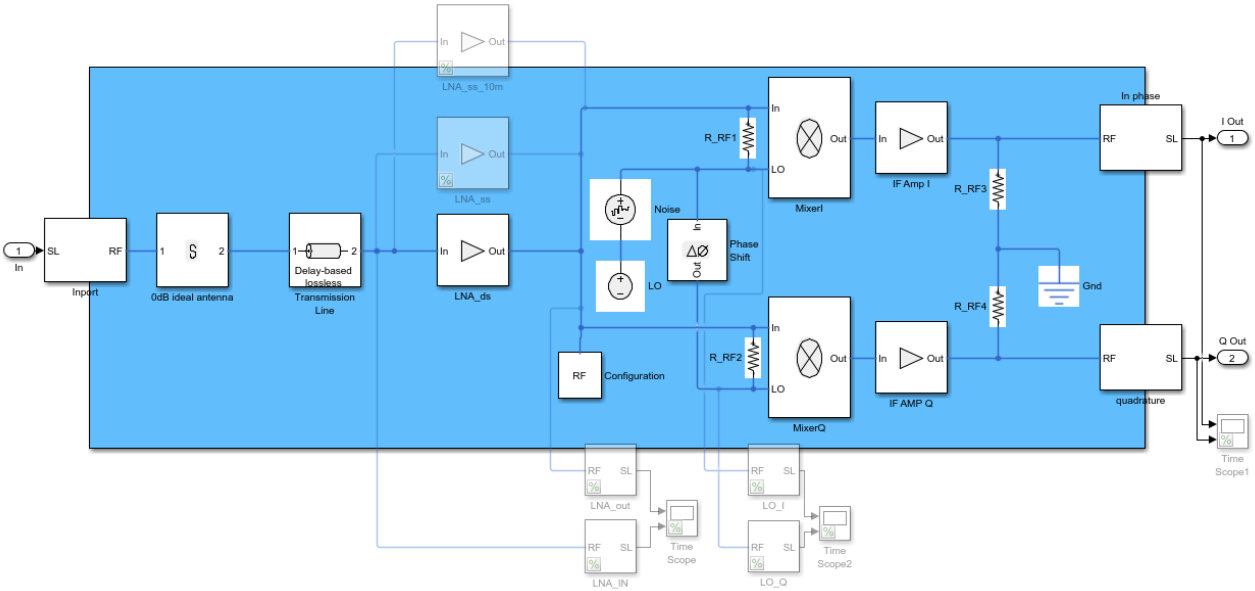

Fig. 13: RF-receiver

In Table 3 are listed the values RMS of real and imaginary parts of the LNA signals, considering a distance of 100 m between transmitter and receiver. With this data we have calculated the Power Gain of the three LNAs and verified with the results obtained in ADS.

Power Gain verification				
	Input signal	Output one-stage 5 mA	Output one-stage 10 mA	Output two-stage 10 mA
Real [V-rms]	4.89e-5	3.02e-4	3.45e-4	2.26e-3
Imaginary [V-rms]	5.25e-5	3.24e-4	3.71e-4	2.42e-3
Power Gain [dB]	-	15.81	16.98	33.28

Table 3: Power Gain verification

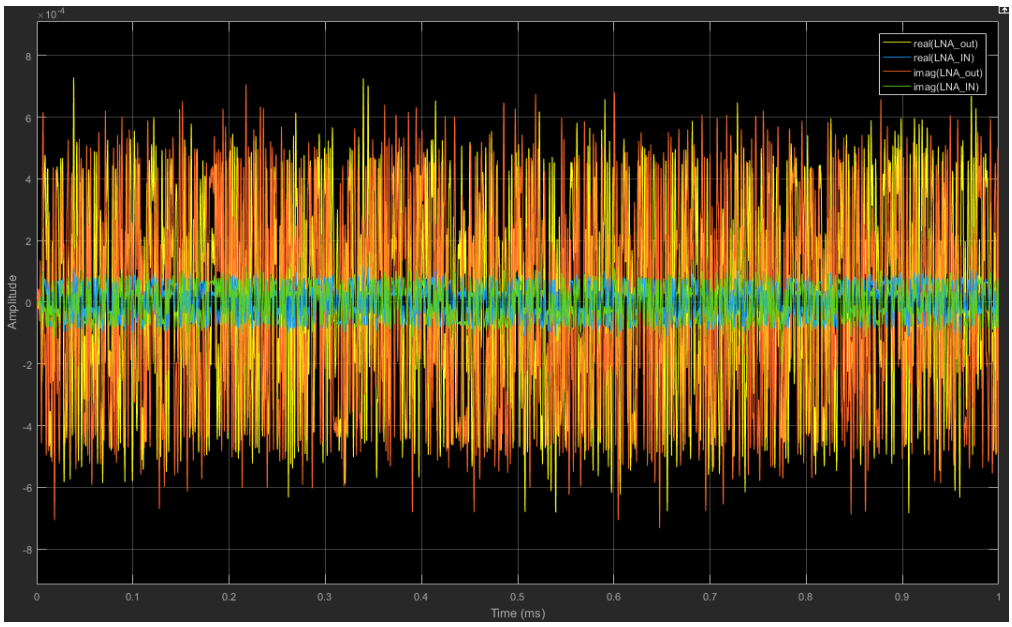

Fig. 14: Signals of one-stage LNA @ 5mA

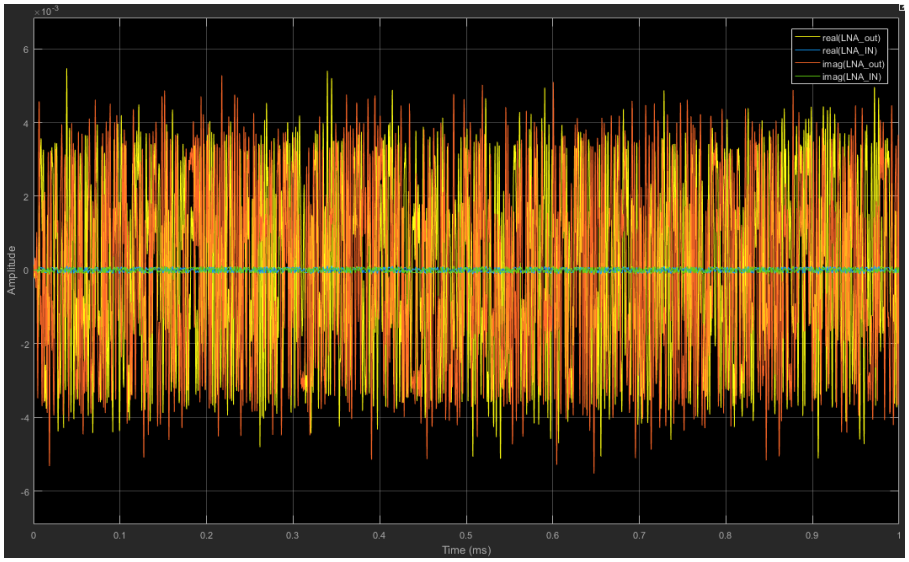

Fig. 15: Signals of two-stage LNA @ 10mA

The digital baseband system is composed by AGC, ADC and demodulator.

In the following tables, some comparisons from the three designed LNAs at various distance are listed.

SER			
Distance [m] / Path Loss [dB]	Single stage 5 mA	Single stage 10 mA	Double stage
0.01 / 27	0	0	0
0.5 / 41	0	0	0
1 / 47	0	0	0
5 / 61	0	0	0
10 / 67	0	0	0
50 / 81	0	0	0
100 / 87	0	0	0
500 / 101	0	0	0
1000 / 107	1.052e-3	0	1.052e-3
2500 / 115	0.2271	0.1756	0.224
5000 / 121	0.5384	0.4879	0.53

Table 4: Symbol error ratio for 951 transmitted symbols

BER			
Distance [m] / Path Loss [dB]	Single stage 5 mA	Single stage 10 mA	Double stage
0.01 / 27	0	0	0
0.5 / 41	0	0	0
1 / 47	0	0	0
5 / 61	0	0	0
10 / 67	0	0	0
50 / 81	0	0	0
100 / 87	0	0	0
500 / 101	0	0	0
1000 / 107	3.505e-4	0	3.505e-4
2500 / 115	7.641e-2	0.05853	7.536e-2
5000 / 121	0.2128	0.1854	0.2082

Table 5: Bit error ratio for 2873 transmitted bits

The Error Vector Magnitude (EVM) is used to quantify the performance of a digital radio communication and it is a measure of how far the points are from the ideal locations. EVM is defined as

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{reference}}} * 100 \qquad (10)$$

Where P_{error} is the RMS power of the error vector (defined as the conjunction vector between the received point and the reference point of the I-Q constellation) and the $P_{reference}$ is the RMS power of the reference vector (defined as the conjunction vector between the center of the I-Q plane and the reference point of the I-Q constellation).

EVM RMS [%]			
Distance [m] / Path Loss [dB]	Single stage 5 mA	Single stage 10 mA	Double stage
0.01 / 27	8.56	4.55	12.99
0.5 / 41	4.18	3.89	10.83
1 / 47	4.12	3.82	5.98
5 / 61	3.95	3.64	3.82
10 / 67	3.9	3.57	3.78
50 / 81	3.97	3.61	3.71
100 / 87	4.26	3.89	3.96
500 / 101	9.48	8.59	9.12
1000 / 107	17.54	15.61	16.97
2500 / 115	33.64	30.91	33.86
5000 / 121	45.22	44.03	45.73

Fig. 16: EVM %

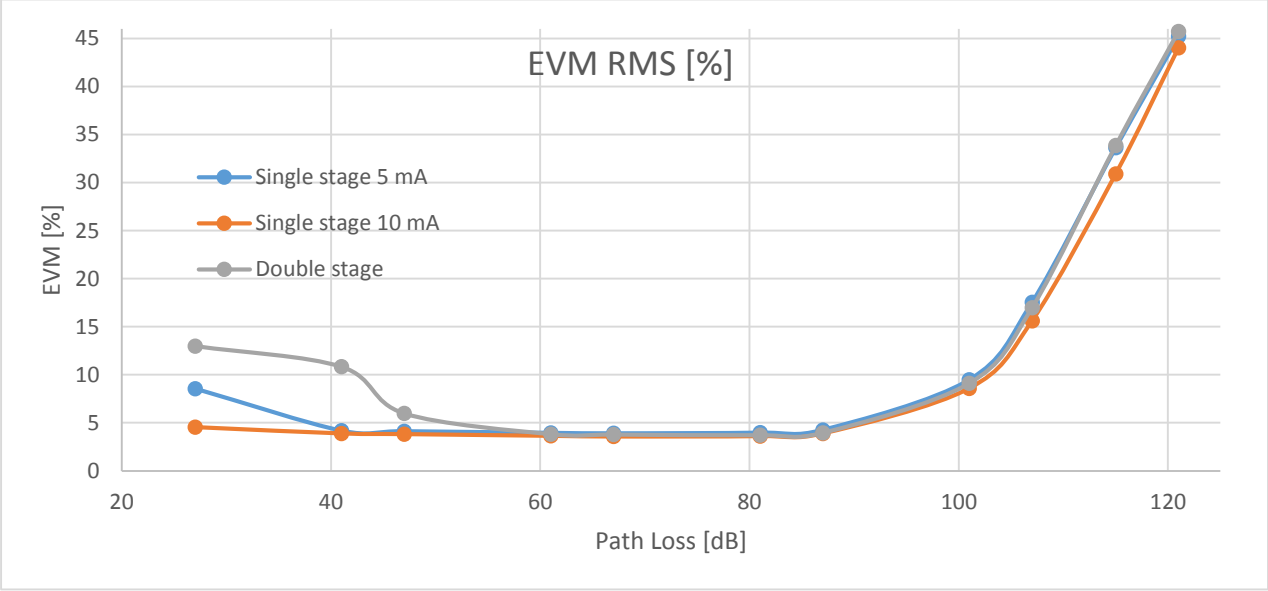

Fig. 17: EVM RMS [%] comparison

EVM Peak [%]			
Distance [m] / Path Loss [dB]	Single stage 5 mA	Single stage 10 mA	Double stage
0.01 / 27	23.73	8.72	33.28
0.5 / 41	8.43	7.25	27.88
1 / 47	8.31	7.21	18.05
5 / 61	8.10	7.00	17.17
10 / 67	7.93	6.78	10.14
50 / 81	8.27	6.80	7.21

100 / 87	9.05	7.58	8.23
500 / 101	19.91	19.43	19.56
1000 / 107	37.78	32.83	36.83
2500 / 115	81.42	72.07	86.92
5000 / 121	116.48	96.49	101.87

Fig. 18: EVM peak

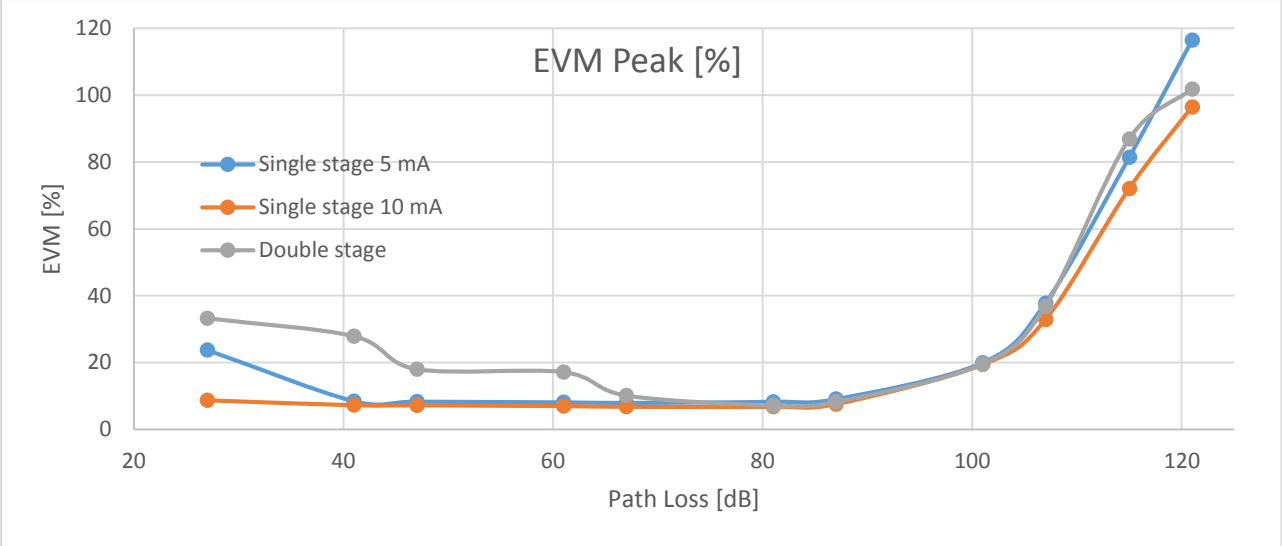

Fig. 19: EVM Peak [%] comparison

The Modulation Error Ratio (MER), as the EVM quantify the performance of a digital communication, it is defined as

$$MER(dB) = 10\log_{10}\frac{P_{signal}}{P_{error}} \qquad (11)$$

It is closely to EVM but is calculated from the average power of the signal.

MER [dB]			
Distance [m] / Path Loss [dB]	Single stage 5 mA	Single stage 10 mA	Double stage
0.01 / 27	21.35	26.84	17.73
0.5 / 41	27.59	28.20	19.31
1 / 47	27.69	28.35	24.46
5 / 61	28.06	28.79	28.35
10 / 67	28.18	28.95	28.45
50 / 81	28.03	28.85	28.61
100 / 87	27.41	28.2	28.04
500 / 101	20.47	21.32	20.8
1000 / 107	15.12	16.13	15.41
2500 / 115	9.46	10.20	9.41
5000 / 121	6.89	7.12	6.80

Fig. 20: MER dB

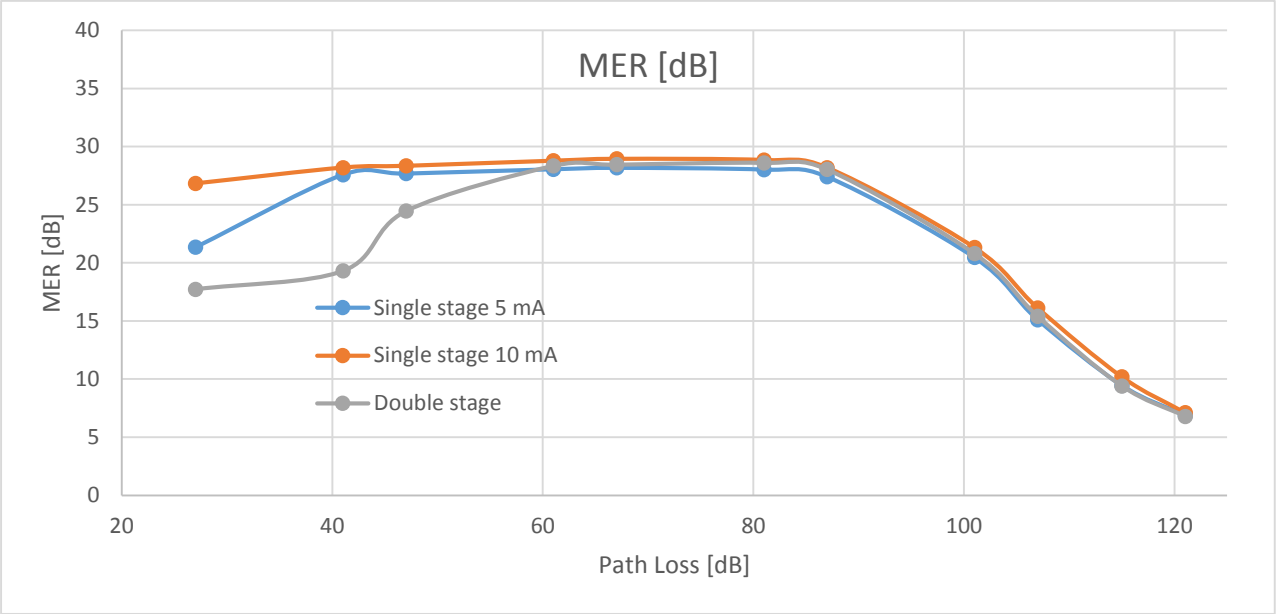

Fig. 21: MER [dB] comparison

At 1 m of distance between transmitter and receiver, the path loss is 47 dB and the receiver input power is about -42 dBm. Which is near at 1 dB Compression Point of the two-stage LNA and this creates non-linearity errors, therefore EVM increases and MER decreases for distance below 1 m.

The data highlight rapid decreases of the performance around 500 m of distance between the transmitter and the receiver (101 dB of path loss). This can be observed in the following pictures.

Fig. 22 and Fig. 23 show the scatter plots of the received data of the double stage LNA at two distance between transmitter and receiver. While Fig. 24 and Fig. 25 display the eye diagrams of the same LNA in the same conditions.

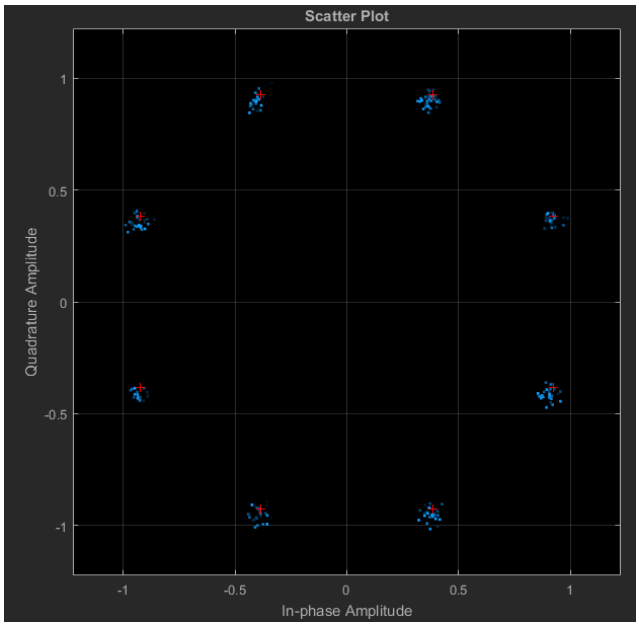

Fig. 22: two-stage 10 mA @ 100m

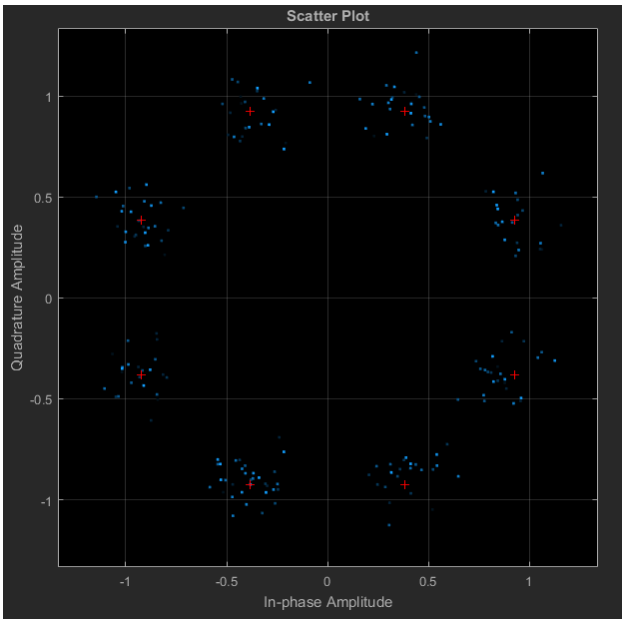

Fig. 23: two-stage 5 mA @ 500m

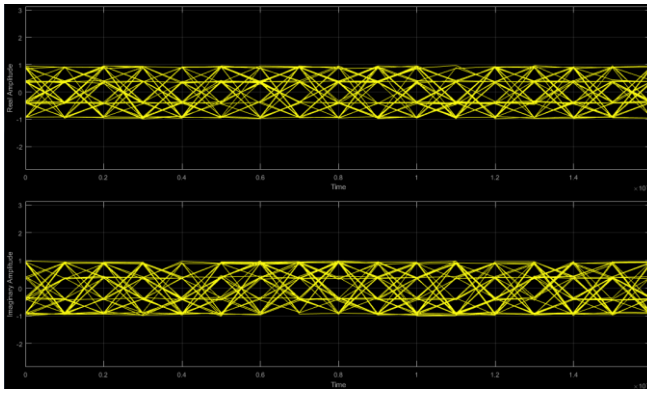

Fig. 24: two-stage @ 100m

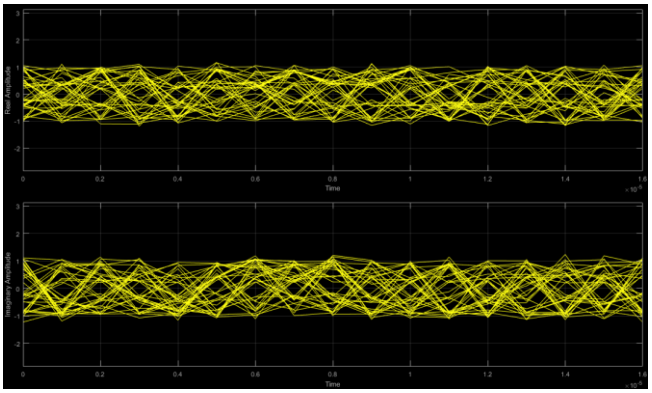

Fig. 25: two-stage @ 500m

5. Conclusions

The two-stage LNA designed in this work, obviously, has a higher power gain than the two single stage LNAs but a worse noise figure due to increased number of elements. This decreases the performance of the transceiver system, as Matlab results highlights. The high power gain of the two-stage LNA (32.31 dB) brings the amplifier to work near to linear condition limit for high input signal value (short distance between the transmitter and receiver) and this decreases its performance.

Since the Friis formula eq. (12)

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \frac{NF_4 - 1}{G_1 G_2 G_3} + \cdots \qquad (12)$$

Considering only the noise of the mixer block NF = 16.02 dB we obtain the total noise figures listed in Table 6. The noise figure calculation of a I-Q receiver is show in [2] . The data show that the best configuration should be the double-stage but the Matlab simulations highlight that its performances are comparable with that of the single stage at 10 mA.

	NF [dB]	**Gt [dB]**	**NFtot [dB]**
One-Stage @ 5 mA	2.337	15.517	4.482
One-Stage @ 10 mA	2.194	16.628	3.988
Two-Stage @ 10 mA	2.367	32.310	2.424

Table 6: Noise Figure comparison

To improve the feature of the two-stage LNA a better evaluation of the power distribution should be done. Currently, the current that flows in the first and second stage is the same but may not be the best solution. Therefore, the increasing of the current in the first stage for a better noise figure and the decreasing that of the second stage to keep the same power consumption could improve its features.

3. Note

3.1. Optimum size

The optimum noise impedance of a common source CMOS configuration can be expressed as eq.(13) [3]

$$Z_{on} = \omega C_{gs} \frac{g_m}{g_{do}} \sqrt{\frac{\delta}{5\gamma}(1-|c|)} - j\omega C_{gs}(1-\alpha|c|\sqrt{\delta\gamma(1-|c|^2)} \qquad (13)$$

if this value is equal to 50 Ω the input power matched is achieved. This can be made with mosfet size about 200 ÷ 300 µm.

The achievement of the Zon allows to obtain the minimum noise figure of this configuration, eq. (14)

$$NF_{min} = 1 + 2\frac{\omega}{\omega_t}\sqrt{\frac{\gamma\delta}{5}(1-|c|)} \qquad (14)$$

This value can be decreased increasing the ω_t, which depends on current density ($J_A = \frac{I_D}{W_{tot}}$). A maximum of ω_t value can be found around 0.2 mA/µm, independently from technology [4 [1]]. Using this and the mosfet value calculated with eq (13) we can obtain a current supply of 40 ÷ 60 mA, to much to be used in an integrated LNA (dissipation power 120 ÷ 180 mW @ power supply 3V).

The common approach used to sizing a LNA with mosfet technology is using the experimental Lee's relation:

Won*fo = 500 ÷ 600 GHz*µm (15)

In this work using a fo = 5.25 GHz the optimum noise size expected is 95 ÷ 115 µm so the LNA is designed again with W = 110 µm, using the same procedure described previous.

In Table 7 are listed the data of the new LNAs and they highlights that the noise figure is surprisingly increased.

	Single stage	Single stage	Double stage	Unity
Isupply	5 mA	10 mA	10 mA	
MN1, MN2, MN4, MN5 size	110	110	110	µm
MN3 size	10	10	10	µm
Rref	5248	2190	5001	Ω
Ls	247	237	184	pH
Lg	5.68	5.46	5.46	nH
Ld	4.14	4.03	4.72	nH
Cd	0.125	0.128	4.72	pF
Cd2	-	-	0.124	pF
Ld2	-	-	4.16	nH
Zin	49.99 - j0.01	50.04 + j0.04	50.09 - j0.11	Ω
Zout	49.83 + i0.213	50.07 - j0.35	50.13 - j0.25	Ω
Zon	112.87 + j16.82	118.01 + j18.34	110.21 + j22	Ω
Gt	17.15	18.02	35.24	dB
NFmin	1.92	1.80	1.95	dB
NF	2.34	2.27	2.38	dB
iCP1dB	-17.99	-18.33	-36.15	dBm
oCP1dB	-1.85	-1.23	-1.92	dBm
iIP3	-0.68	-1.25	-0.74	dBm
oIP3	8.98	8.41	8.91	dBm
Saturation Power	9.46	9.675	6.68	dBm

Gain compression @ Psat	36.31	36.69	34.19	dBm

Table 7: 110 um LNAs parameters

The NFmin is decreased following the ω_t relation but the difference between the optimum noise impedance and the input impedance is increased.

3.2. Decreases Noise Figure

Changing the topology architecture of the mosfets is possible decrease the noise figure.

Keeping the same Wtot of the mosfet but changing the w of the single structure (from 10 µm to 5 µm) and doubling the fingers number, the noise figure decreases (Table 8).

	Double stage	**Double stage**	**Unity**
W mos	10	5	µm
Finger number	14	28	
MN1, MN2, MN4, MN5 size	140	140	µm
MN3 size	10	10	µm
Rref	6610	6609	Ω
Ls	258	269	pH
Lg	4.32	4.21	nH
Ld	4.23	4.11	nH
Cd	0.23	0.218	pF
Cd2	0.143	0.125	pF
Ld2	3.6	3.75	nH
Zin	50.03 + j0.13	50.08 - j0.02	Ω
Zout	50.11 – j0.04	49.96 – j0.34	Ω
Zon	92.52 + j16.07	85.81 + j19.51	Ω
Gt	32.31	35.77	dB
NFmin	2.097	1.85	dB
NF	2.367	2.07	dB
iCP1dB	-32.07	-36.97	dBm
oCP1dB	-0.761	-2.20	dBm
iIP3	0.93	-5.39	dBm
oIP3	10.59	4.27	dBm
Saturation Power	7.63	7.1	dBm
Gain compression @ Psat	46.66	53.77	dBm

Table 8: Simulation results of 5 um and 10 um mosfets

Another effect of noise figure decreasing can be observed using parallel mosfets instead fingered mosfets.

	Double stage	**Double stage**	**Unity**
W mos	10	5	µm
N parallel mos	1	4	
Finger number	14	7	
MN1, MN2, MN4, MN5 size	140	140	µm
MN3 size	10	10	µm
Rref	6610	6637	Ω

Ls	258	250	pH
Lg	4.32	3.96	nH
Ld	4.23	3.78	nH
Cd	0.23	0.219	pF
Cd2	0.143	0.093	pF
Ld2	3.6	3.98	nH
Zin	50.03 + j0.13	50.36 - j0.47	Ω
Zout	50.11 – j0.04	49.94 – j1.52	Ω
Zon	92.52 + j16.07	77.53 + j27.19	Ω
Gt	32.31	42.62	dB
NFmin	2.097	1.59	dB
NF	2.367	1.78	dB
iCP1dB	-32.07	-47.48	dBm
oCP1dB	-0.761	-5.86	dBm
iIP3	0.93	-5.20	dBm
oIP3	10.59	4.46	dBm
Saturation Power	7.63	5.82	dBm
Gain compression @ Psat	46.66	91.4	dBm

Table 9: Simulation results parallel mosfets

This effect could be due to the value of Cgs used in the simulating mos model. Without the layout of parallel mosfets the simulator cannot use the real Cgs.

All the data are taken with simulations so parasitic effects of real connections are neglected. Layout and post-Layout simulations has to be done to obtain more accuracy values.

Reference

[1] Q. Xu, Z. Lai, C. Shi e R. Zhang, «A 5.15-5.825GHz CMOS Down-Conversion Mixer for WLAN 802.11a,» in *Wireless Communications, Networking and Mobile Computing (WiCOM), 2011 7th International Conference on*, 2011.

[2] E. D. Charles Razzell, «System Noise-Figure Analysis for Modern Radio Receivers,» Maxim Integrated Tutorial 5594, 2013.

[3] D. Shaeffer e T. Lee, «A 1.5-V, 1.5-GHz CMOS low noise amplifier,» *IEEE Journal of Solid-State Circuits,* vol. 32, n. 5, 1997.

[4] T. Dickson, K. Yau, T. Chalvatzis, A. Mangan, E. Laskin, R. Beerkens, P. Westergaard, M. Tazlauanu, M.-T. Yang e S. Voinigescu, «The Invariance of Characteristic Current Densities in Nanoscale MOSFETs and Its Impact on Algorithmic Design Methodologies and Design Porting of Si(Ge) (Bi)CMOS High-Speed Building Blocks,» *IEEE Journal of Solid-State Circuits,* vol. 41, n. 8, 2006.