Psi or Theta: Which One Should You Choose?

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Many device data sheets now list both of these thermal characterization parameters, but to apply them accurately in power-supply designs, engineers must understand the subtle differences in how these terms are defined.

Over the years, standards organizations have undertaken numerous efforts to standardize the test methods that are used to characterize the thermal performance of semiconductor devices. Groups such as Semiconductor Equipment and Materials International (SEMI), the Electronic Industries Alliance (EIA) and the Joint Electron Device Engineering Council (JEDEC) have developed several standards or specifications that define methods of measuring a variety of thermal characterization parameters.

For example, the SEMI organization drafted standards for measuring the thermal resistance of ceramic packages, integrated circuit packages and semiconductor packages under different environmental and test conditions. These standards defined the familiar theta (θ) terms for *thermal resistance* such as θ_{JA} and θ_{JC}.

But recognizing certain limitations of these standards, EIA and JEDEC later came along and defined their own standards for measuring the performance of semiconductor devices. In the process, they clarified the applicability and narrowed the scope of the existing theta terms for thermal resistance, while also creating a new set of *thermal characterization parameters*, symbolized by the Greek letter psi (Ψ). As with theta, the psi terms usually carry subscripts that reflect measurement conditions.

As the EIA/JEDEC standards describe, the psi and theta terms are related but have different meanings and implications for use. Now that both terms are appearing more frequently on device data sheets, it's imperative that system designers understand the distinctions between the terms and how these terms are defined, so that they understand how the device vendors are characterizing their parts.

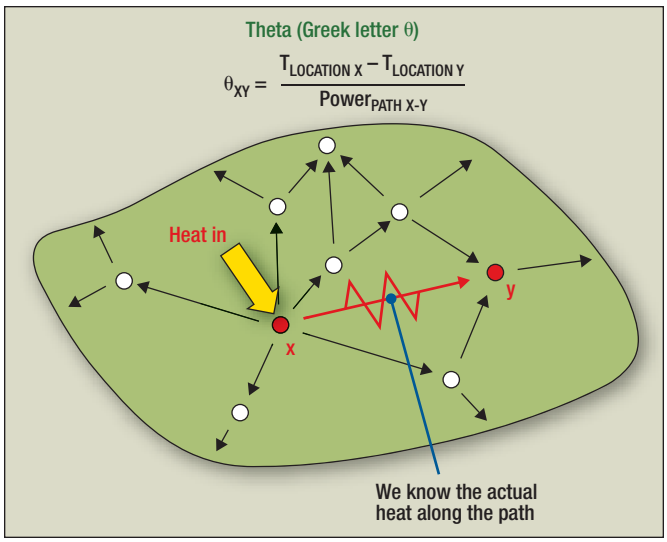

Fig. 1. *Theta defined, showing that you have to know the heat flowing along the specific path from location x to location y to properly use the term.*

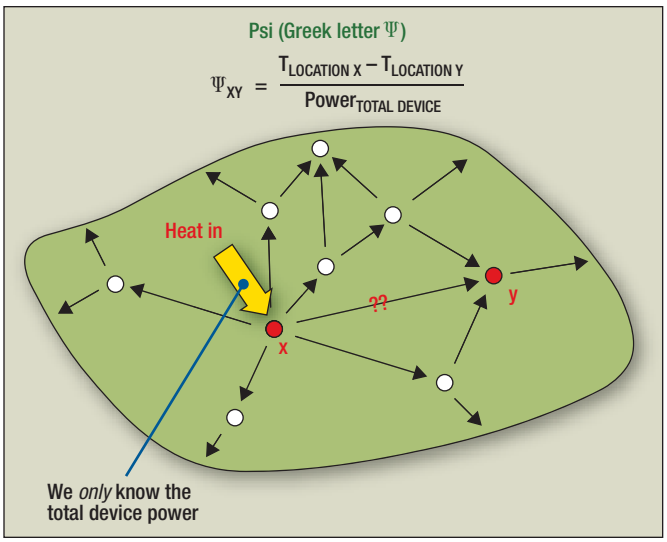

Fig. 2. *Psi defined, showing that when you don't know the heat flowing along the specific path from location x to location y, and all you know is the total heat into the system, you have a psi, not a theta.*

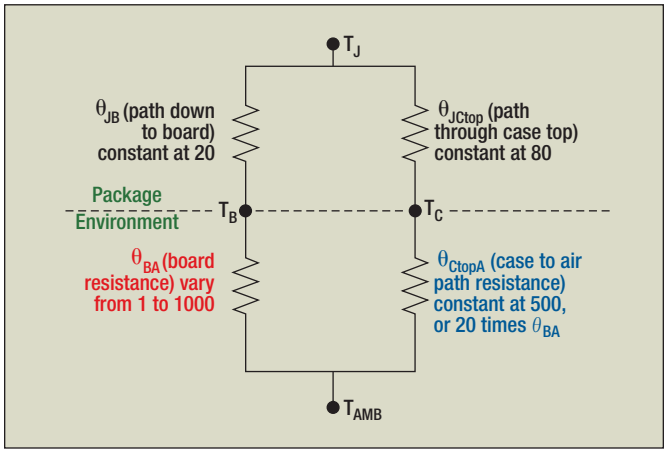

Fig. 3. *Four-resistor network illustrates how psi values change depending on the external environment, even when the package is constant.*

This article will first review, in some detail, the nuances of the standards themselves. It will then illustrate, by using a relatively simple system model, why these seemingly subtle differences in definitions between theta and psi are, in fact, profound. Armed with that knowledge, designers can make more accurate predictions about the thermal performance of the semiconductor devices in their systems.

Thermal Parameters Defined

Many of the now-familiar thermal-resistance parameters were originally defined by the SEMI organization. Three standards in particular are worth noting. In quoting excerpts from these standards, I have italicized certain passages to highlight some of their limitations.

1. SEMI G30-88 "Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages." This test method deals *only with junction-to-case or mounting surface measurements* of thermal resistance and *limits itself to heatsink and fluid bath testing* environments. The heatsink mounting method for measuring *junction-to-case thermal resistance is a conservative* measure of the package's ability to transfer heat to the ambient environment, because heatsinking is provided only on one side of the package, whereas the fluid bath mounting method has the potential for equally cooling both sides of the package.

2. SEMI G38-0996 "Test Method for Still- and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of Integrated Circuit Packages." This test method deals *only with junction-to-ambient* measurements of thermal resistance and *limits itself to still- and forced-air convection testing environments.*

3. SEMI G68-0996 "Test Method for Junction-to-Case Thermal Resistance Measurements in an Air Environment for Semiconductor Packages." The measurement *results are usually different from the results obtained by testing in the fluid bath environment* described in SEMI G30-88 and in SEMI G43-87 "Test Method for Junction-to-Case Thermal Resistance Measurements of Molded Plastic Packages," not summarized here.

From these definitions, it should be clear that it is very difficult to define a thermal parameter that's going to apply to a package under all circumstances. Yet, for some reason, device manufacturers — even the ones following these standards — tend to gloss over this fact in their data sheets.

However, in the industry at large there was a recognition that the SEMI standards were inadequate. Consequently, in the early 1990s, EIA/JEDEC (www.jedec.org), the developer of standards for the solid-state industry, drafted its own comprehensive thermal standards.

As can be seen in the following excerpt from JESD51-2 "Integrated Circuits Thermal Test Method Environmental Conditions — Natural Convection (Still Air)," published in 1995, JEDEC recognized the same issues as SEMI:

"The purpose of this document is to outline the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient (θ_{JA}) thermal resistance measurement in natural convection. The intent of θ_{JA} measurements is solely for a thermal performance comparison of one package to another in a standardized environment. *This methodology is not meant to and will not predict the performance of a package in an application-specific environment.*"

So, how did JEDEC improve the situation? In my view, the most significant improvement was the definition of some new terms. In particular, farther into JESD51-2, § 4.3 states:

"... The junction-to-top center-of-package thermal characterization parameter, Ψ_{JT}, is calculated using the following equation: $\Psi_{JT} = (T_{Jss} - T_{Tss})/ P_H$. ... The relationship between the junction-to-ambient thermal resistance, θ_{JA}, and the junction-to-top center-of-package thermal characterization parameter, Ψ_{JT}, is described by: $\theta_{JA} = \Psi_{JT} + \Psi_{TA}$, where Ψ_{TA} equals thermal characterization parameter from top surface of package-to-air (°C/W). ... *The thermal characterization parameters, Ψ_{JT} and Ψ_{TA}, have the units °C/W but are mathematical constructs rather than thermal resistances because not all of the heating power flows through the exposed case surface. ... Also, Ψ_{TA} is very dependent on the application-specific environment.*"

It took another decade, but the logical extension of Ψ to other points of interest was codified in 2005, when JEDEC published JESD51-12 "Guidelines for Reporting and Using Electronic Package Thermal Information," and in which can be found, among other statements:

"... The purpose of the JESD51 standards is to compare the thermal performance of various packages under standardized test conditions. While standardized thermal test information cannot apply directly to the many specific applications, the standardized results can help compare the relative thermal performance of different packages. A more meaningful comparison is possible if the test conditions are understood along with the factors affecting package thermal performance. Brief discussions of key topics are included in this guideline."

Within the guidelines, it is noted that Ψ_{JB} was not in-

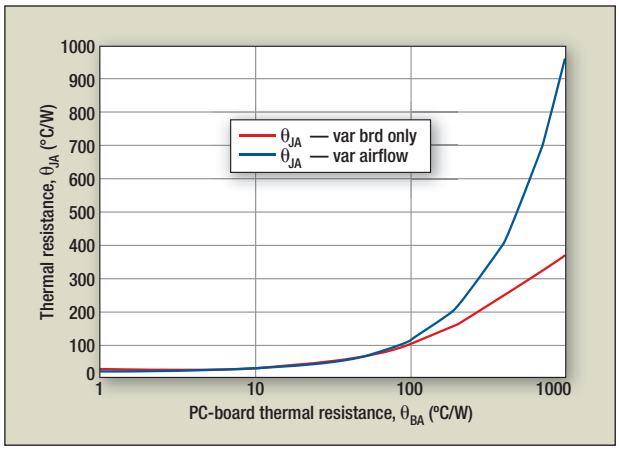

Fig. 4. *Four-resistor network (of Fig. 3) results in these widely varying θ_{JA} values, even when the package contribution is fixed.*

cluded in the natural convection standard because it had not yet been defined, but that it may be added in the future. JESD51-12 further went on to clarify some existing terminology, in particular θ_{JC} and θ_{JB}:

"The conduction thermal resistances θ_{JCx} and θ_{JB} are measured with nearly all of the component power dissipation flowing through either the top or the bottom of the package. The values may be useful for comparing packages but the test conditions don't generally match the user's application. … θ_{JCx} is the junction-to-case thermal resistance. The 'x' indicates the case surface where T_{Case} is measured and through which the heat is forced to flow during the θ_{JCx} measurement, 'top' for the top surface or 'bot' for the bottom surface. … Ideally, during θ_{JCx} measurement, close to 100% of the power flows from the junction to the 'x' case surface. The θ_{JCx} nomenclature is used to avoid the confusion associated with θ_{JC}. Historically, the θ_{JC} case surface is defined as the 'outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk.' This could be either the top or bottom surface, but it is not always clear which surface was used when a θ_{JC} value is reported."

In § 5.2.3 of the JESD51-12 Guidelines, Ψ_{JT} and Ψ_{JB} thermal characterization parameters are discussed:

"The thermal characterization parameters Ψ_{JT} and Ψ_{JB} are measured by suppliers at the same time and in the same environments as θ_{JA} or θ_{JMA}. Users can apply the Ψ equations to estimate the component junction temperature in their application by measuring a component temperature in the application environment and using the appropriate Ψ thermal characterization parameter. This estimated junction temperature can then be compared with a junction temperature specification. A component power estimate is required. … Using Ψ_{JT} or Ψ_{JB} values together with package top or board temperature measurements in a system requires good temperature measurement technique, comparable to that used when the supplier measured Ψ_{JT} or Ψ_{JB}. … When a heatsink or added heat spreader is present, neither Ψ_{JT} nor Ψ_{JB} can be used to estimate the junction temperature. It can be approximated using θ_{JCtop}, measuring the heatsink temperature in the application as close to the package interface as possible, and accounting for the temperature difference across the heatsink to case interface. Alternatively, some suppliers may provide a junction-to-sink Ψ_{JS} thermal parameter that may be used analogously to Ψ_{JT}, recognizing that the Ψ_{JS} value is dependent on the package-to-heatsink interface."

A Closer Examination

Figs. 1 and **2** introduce a very generic "thermal system" that illustrates what's different between the definitions of θ and Ψ. Referring to **Fig. 1**, if you can define the path along which heat flows and quantify the heat along that path, *only* then can you call it θ. With this restriction, it may be seen that the traditional definitions of θ_{JA} and θ_{JC} are applicable. Regarding θ_{JA}, all the heat that can flow must originate at the junction and end up at ambient (even if the path isn't pinned down, at least you know the heat can't sneak away to somewhere not encompassed by the system). Regarding θ_{JC}, you can presume that something approaching 100% of total device heat is flowing out through the heatsink, which it is supposed to do. Of course, you have to know what location on the package, exactly, is meant by the word "case" in the specifications.

On the other hand, referring to **Fig. 2**, if all you can do is

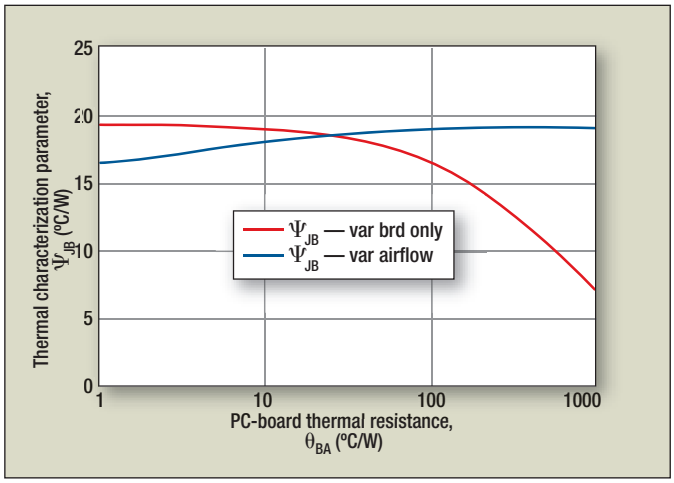

Fig. 5. *Four-resistor network (of Fig. 3) results in these widely varying Ψ_{JB} (junction to board) values, even when the package contribution is fixed. Observe that over certain limited conditions, Ψ_{JB} actually approximates θ_{JB} (20°C/W).*

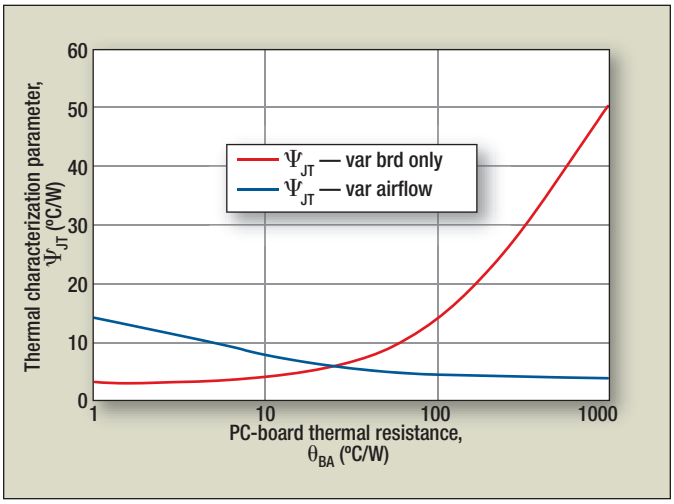

Fig. 6. *Four-resistor network (of Fig. 3) results in these widely varying Ψ_{JT} (junction to case-top) values, even when the package contribution is fixed. Here, observe that Ψ_{JT} never even comes close to the actual path resistance θ_{JCtop} (80°C/W) over any conditions explored in this simple model.*

measure the total device power and you have no idea of how much of it flows up, down, out the leads or through the air gap (pretty typical in the semiconductor packaging thermal lab), yet you really would like to measure the temperature at one or more points around the boundary of the package (which is actually pretty easy), then you can't call it a θ, but must instead call it a Ψ. Thus, JEDEC's new terms Ψ_{JT}, Ψ_{TA}, Ψ_{JL} and Ψ_{JB} are all concessions to the reality that it's easy to measure temperature and really difficult to measure heat flux — especially on miniscule semiconductor devices.

Still, you may be asking, why is this distinction between θ and Ψ so important? Take a look at the simple four-resistor package model shown in **Fig. 3**. I've used θ's here for the four individual resistors, because I'm defining them to be true thermal path resistances. (In particular, I'm using θ_{JCtop} as the true path resistance from the junction to the top of the package, where it's exposed to the air; in a moment, I'll relate it to the original JEDEC-defined Ψ_{JT} to represent the characterization parameter to the top center of the plastic case.)

As you see, what I've really done is to create a two-resistor "compact thermal model" of the package, along with two external resistances that digest the entire external system behavior into a very minimal set of parameters.

Taking the system as a whole, the overall thermal resistance, junction to ambient, can be written as follows:

$$\theta_{JA} = \frac{T_J - T_{AMB}}{Q_{TOTAL}} = \frac{1}{\left(\frac{1}{\theta_{JB} + \theta_{BA}}\right) + \left(\frac{1}{\theta_{JCtop} + \theta_{CtopA}}\right)}$$

It takes a little more effort, but if you work it out, you'll also be able to derive the following:

$$\Psi_{JB} = \frac{T_J - T_B}{Q_{TOTAL}} = \frac{\theta_{JB}}{1 + \left(\frac{\theta_{JB} + \theta_{BA}}{\theta_{JCtop} + \theta_{CtopA}}\right)}$$

$$\Psi_{JT} = \frac{T_J - T_B}{Q_{TOTAL}} = \frac{\theta_{JC}}{1 + \left(\frac{\theta_{JC_{TOP}} + \theta_{CtopA}}{\theta_{JB} + \theta_{BA}}\right)}$$

What this says, if you think about it, is that even when the two-package thermal resistances are absolutely and truly constant (the two-parameter compact thermal model values θ_{JB} and θ_{JCtop}), the corresponding Ψ values Ψ_{JB} and Ψ_{JC} are not constants (unless the overall ratio of the two individual paths happens to remain constant).

To put some meat onto this skeleton, look at **Figs. 4**, **5** and **6**. All I've done to generate these graphs is hold θ_{JB} and θ_{JCtop} constant, and let θ_{BA} and θ_{CtopA} vary. (For one scenario in each graph, I let the ratio of θ_{CtopA} to θ_{BA} be fixed — and called the plot "var airflow." In the other scenario, I held θ_{CtopA} constant and allowed θ_{BA} to vary by itself — and called the plot "var brd only.")

Now you might not have as much as three orders of magnitude of possible variation in your particular application board or airflow. But that's not totally outrageous over all possible users and applications of a particular device. The point is that Ψ_{JT}, in particular, can easily vary by 300% in a variable airflow situation and by more than 1000% when the board resistance alone changes by a factor of 1000.

Unfortunately, Ψ_{JT} is the value very often reported by another name in data sheets in which vendors haven't been careful to define their terms; through oversight or unfamiliarity with the newer JEDEC standards, it might even be called θ_{JC}. So if you wondered what that Ψ_{JT} parameter meant when you saw it recently, now you know. And if you aren't sure how your device supplier measured and reported its data sheet thermal values, now you should care! **PETech**