UWB CMOS Monocycle Pulse Generator

Fabio Zito, Domenico Pepe, *Member, IEEE*, and Domenico Zito, *Member, IEEE*

***Abstract*—A low-complexity fully integrated ultrawideband (UWB) monocycle pulse generator realized in 90-nm CMOS technology by ST-Microelectronics is presented. The circuit provides a monocycle pulse when activated by a negative edge of an external trigger signal provided by a microcontroller by exploiting the operating principle of nonlinear waveform shapers. This pulse generator represents a building block of an innovative wearable system-on-chip UWB radar on silicon for cardiopulmonary monitoring. On-chip measurements show that the pulse generator provides monocycle pulses with a duration time equal to 380 ps and a peak-to-peak amplitude of 660 mV (including the losses of the microprobes, cables, and electrostatic-discharge-protected pads), which are in very good agreement with the postlayout simulations. The power consumption is 19.8 mW from a 1.2-V power supply.**

***Index Terms*—Pulse generator, radio frequency complimentary metal–oxide–semiconductor (RF-CMOS), system on chip, ultrawideband (UWB) radar**

I. Introduction

In February 2002, the FCC released permission for the marketing and operations of a new class of products incorporating ultrawideband (UWB) technology [1]. Unlike traditional narrowband RF transceivers, UWB devices operate by transmitting very short electromagnetic pulses (from tens of picoseconds to a few nanoseconds). Thus, the spectrum of a UWB signal results to be widespread over a large frequency band (e.g., several gigahertz) with a very low power spectral density (PSD). In detail, the FCC, through a modification of the 47 CRF Part 15 regulations [2], decided to allocate for UWB systems a 7.5-GHz unlicensed band (for the first time, in a nonexclusive way) in the range of the RF spectrum 3.1–10.6 GHz. Asia and Europe have recently adopted similar regulations for UWB applications in the same frequency band [3], [4]. The mask of the maximum spectral density of transmitted power allowed for UWB devices has been set to a very low level (-41.3 dBm/MHz). UWB devices can be employed for several applications: ground-penetrating radars, medical imaging, wall imaging, through-wall imaging, surveillance, and high-data-rate communications, which are of large interest for the realization of low-cost mass-market wireless interface.

Due to the latest advances in silicon technologies, particularly CMOS (e.g., the 90-nm CMOS process by ST-Microelectronics includes MOSFETs with a cutoff frequency of up to 150 GHz), modern standard processes offer the potential required for the realization of miniaturized (i.e., system-on-chip) devices for many emerging applications, as well as UWB.

One of the most important challenges for the development of such system-on-a-chip (SoaC) in silicon, CMOS most of all, is represented by the on-chip generation of UWB pulses [5]–[8].

UWB pulse generators can primarily be classified in accordance with the three main signal categories: 1) pulse (e.g., Gaussian); 2) monocycle pulse; and 3) multicycle pulse. Monocycle pulses [9] are preferred to simple pulses since they have no dc components, which could represent a limit for the spectral mask compliance and the radiation efficiency of the antenna, as well as the case of the UWB frequency range 3.1–10.6 GHz. Multicycle pulses [10], [11] are obtained by amplitude modulation, or controlled fast startup, of oscillator circuits, which are for this reason commonly called as carrier-based pulse generators. Multicycle pulses can also be obtained by combining more single pulses, as reported in [12]. In short, for monocycle pulses of duration T_0, the maximum PSD is placed at frequency f_0 (i.e., $1/T_0$); for multicycle pulses based on a carrier modulated with pulse of duration time T_M ($T_M = NT_0$, where N is the number of cycles), the maximum output power spectrum is located at the carrier frequency $(1/T_0)$, whereas the bandwidth of the relevant spectrum is approximately equal to $1/T_M$ [13]. For this reason, multicycle pulses can be conformed to the spectrum mask in an easier way than monocycle pulses. However, in the presence of strong interferes (e.g., echoes) in the communication channel and in the case in which very short pulses are required [7], [13], [14], monocycle pulse are preferred to multicycle, as in case [15].

In particular, for the UWB monocycle pulse generator, the main design challenges consist of reaching a very short duration time for mask compliance, the adequate amplitude to drive directly the antenna without requiring any additional amplification, and the full integration on silicon.

The techniques currently adopted for the generation of monocycle pulses on silicon are mainly based on Gaussian filters and digital circuits. Gaussian filters are implemented by cascading small-signal complex analog filters, which provide pseudo-Gaussian monocycle pulses by filtering small signals (typically, triangular pulses) internally preformed by means of analog/digital circuitry. Such monocycle pulses will then be amplified by additional output stages. For this reason, the most relevant solution reported in the literature provides a

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F. Zito is with the Department of Information, Mathematics, Electronics and Transportation (DIMET), "Mediterranea" University of Reggio Calabria, 89100 Reggio Calabria, Italy.

D. Pepe is with Tyndall National Institute, Lee Maltings, Cork, Ireland.

D. Zito is with the Department of Microelectronic Engineering and the Tyndall National Institute, University College Cork, Cork, Ireland (e-mail: domenico.zito@tyndall.ie).

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monocycle with low peak-to-peak amplitude and requires significant power consumption [6]. Monocycle pulse generators based on digital circuits are typically implemented by using logic programmable circuits and additional buffers to properly drive the load (i.e., the antenna) [16], [17]. The most relevant solutions in the literature show large flexibility in terms of programmability, low peak-to-peak amplitude, and moderate power consumption. These aspects can be recognized at first glance by summarizing the performance of the most relevant works of the literature, which are reported hereinafter.

In [6], a duration time close to 375 ps, a peak-to-peak amplitude of 175 mV, and a power consumption of 45 mW from a 1.8-V supply voltage are obtained with a fully integrated solution in a 0.18-μm Bi-CMOS process by exploiting the Gaussian filter approach.

In [12], a monocycle pulse with a duration time of 500 ps and a peak-to-peak amplitude close to 100 mV from a 1.8-V supply voltage are obtained for a fully integrated solution in 0.18-μm digital CMOS technology by exploiting distributed devices and analog and digital circuits.

In [16], a duration time of 750 ps, a peak-to-peak amplitude of 1.8 mV, and a power consumption of 27.4 mW from a 3.3-V supply voltage are obtained with a fully integrated solution in a 0.35-μm SiGe-CMOS process and by exploiting the digital circuit approach.

In [17], a duration time of 280 ps, a peak-to-peak amplitude of 123 mV, and a power consumption of 12.6 mW from a 1.8-V supply voltage are obtained for a fully integrated solution in a 0.18-μm CMOS process by exploiting the digital circuit approach.

All these solutions provide monocycle pulse with limited amplitude, which could not be enough for many applications, as well as in [15].

A novel fully integrated pulse generator implemented with low-complexity analog and digital circuits and by using only transistors, resistors, and capacitors was recently presented in [18] as the basic circuit idea. The analytical description, the detailed design methodology, and the proof of the concept through test-chip implementation and measurements were not reported therein. This paper deals with all these open issues and provides the final validation through experimental results on test chips.

The circuit provides a pulse with peak-to-peak amplitude close to 1 V on a 100-Ω load resistance and a duration time of a few hundreds of picoseconds, with an associated low-power consumption of a few tens of milliwatts from a supply voltage of 1.2 V. Note that the peak-to-peak amplitude is close to the supply voltage. In particular, the proposed solution is a part of the transmitter of an innovative SoaC CMOS UWB radar for cardiopulmonary monitoring [15], in which such performance are required. In spite of this design framework, the novel pulse generator can be useful for a large number of applications, in which monocycle pulses are required [7], [13], [14].

This paper is organized as follows: In Section II, the operating principle and the design criteria of the fully integrated UWB pulse generator are reported. In Section III, the design synthesis in a standard 90-nm CMOS technology is reported and discussed. In Section IV, the results of the experimental characterization are reported. Finally, in Section V, the conclusions are drawn.

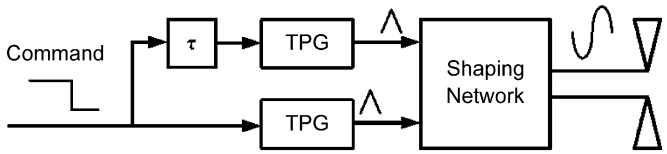

Fig. 1. Block diagram of the novel pulse generator. TPG is the triangular pulse generator, whereas τ is the delay building block.

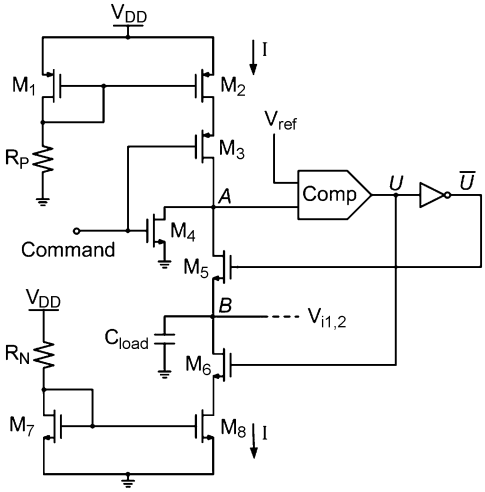

Fig. 2. Simplified circuit of the triangular pulse generator. The triangular pulse (V_i) is provided at node B. $V_{\rm ref}$ is an internal voltage reference.

II. UWB Pulse Generator

The idea [18] consists of driving a CMOS source-coupled differential pair (i.e., the shaping network) by means of a triangular monocycle pulse. The block diagram of the pulse generator is shown in Fig. 1. The circuit provides a monocycle pulse at each occurrence of the negative edge of a digital control signal provided by a microcontroller (i.e., the signal *Command*).

The triangular monocycle pulse is realized by means of the combination of two triangular pulses, both obtained by means of two identical triangular pulse generators, one of those is activated after a proper delay (τ).

When the shaping network is driven by a triangular monocycle, it provides a differential output voltage on the load resistance (i.e., the antenna) that is very close to a sinusoidal monocycle $(s(t))$, in accordance with the principle of the nonlinear wave shapers [19]. Note that, since the triangular pulses are typically obtained by charging the capacitance with a constant current, such as in our case, the triangular pulse generator cannot be exploited to directly drive the antenna, and then a circuit with buffer capability (as well as the shaping network) is needed anyway. In Section III, we will detail this feature by providing a demonstration of the operating principle, which is not reported therein [19].

A. Triangular Pulse Generator

Each triangular pulse is obtained by the circuit (i.e., triangular pulse generator) shown in Fig. 2 [13]. The command signal of the second triangular pulse generator is derived by the same command digital signal by introducing a delay time (τ) realized by means of an additional buffer properly sized.

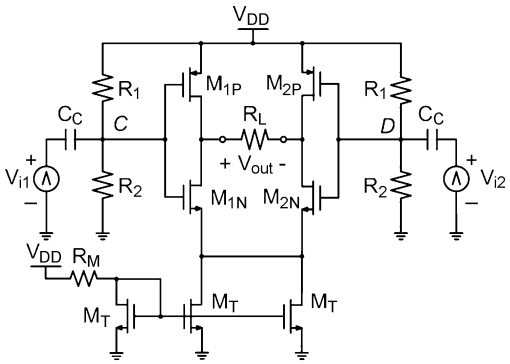

Fig. 3. Simplified schematic of the shaping network. The load resistance R_L represents the antenna.

In practice, the triangular pulse generator exploits the concept of charging and discharging a capacitor by means of a constant current. By acting on the charge current (i.e., I, see Fig. 2) and delay time τ, a triangular pulse with a variable duration time can be generated. The operating principle is detailed hereinafter.

When the negative edge of the digital signal *Command* occurs, then the transistor M_4 is switched off and the transistor M_3 is switched on. As long as the voltage at node A is lower than $V_{\rm ref}$, the output of the comparator (U) is in the low state (i.e., 0 V). Thus, the transistor M_5 is on, whereas the transistor M_6 is off. The constant current flows through M_3 and M_5 and then into $C_{\rm load}$. Thus, the voltage at node B grows up linearly, and the voltage at node A rises. When the voltage at node A becomes equal to $V_{\rm ref}$ (i.e., the threshold voltage of the comparator), then the output of the comparator becomes high (i.e., 1.2 V), M_5 turns off, and M_6 turns on. The capacitor $C_{\rm load}$ begins its discharge at constant current through the transistor M_6, and the voltage at node B linearly decreases, in principle, until it reaches its minimum value (i.e., 0 V).

B. Shaping Network

The shaping network provides a differential output voltage (on the antenna load) that is very close to a sinusoidal monocycle $(s(t))$ when it is driven by the triangular pulse generator described in Section II-A.

The expressions of a sinusoidal monocycle $s(t)$ and its Fourier transform $S(f)$ are reported hereinafter

$$s(t) = A\sin(\omega_0 t) rect\left(\frac{t}{T_0}\right) \tag{1}$$

$$S(f) = j\frac{A}{2}T_0\left(\frac{\sin\left(\pi T_0(f+f_0)\right)}{\pi T_0(f+f_0)} - \frac{\sin\left(\pi T_0(f-f_0)\right)}{\pi T_0(f-f_0)}\right) \tag{2}$$

where A is the amplitude, and T_0 is the duration time.

As for the operating principle of the shaping network (see Fig. 3), the idea consists of driving the differential pair by means of a triangular monocycle pulse. Then, by this unbalance of the differential pair, the monocycle pulse is obtained on the output load (i.e., the antenna).

In detail, when the triangular pulses are not applied to the inputs of the CMOS differential pair, the voltages at nodes C and D are at their dc level $(V_C = V_D)$. When the large triangular pulse (i.e., V_{i1}) starts to be applied to node C (the voltage at the node D is at its dc level), transistors M_{2P} and M_{1N} are switched on, whereas M_{2N} and M_{1P} are switched off. During this time, the CMOS differential pair is unbalanced, and the drain currents of M_{2P} and M_{1N} flow through the load R_L. When the triangular pulse V_{i1} ends (the voltage at node C is returned at the dc level), the second large triangular pulse (i.e., $V_{i2}(t) = V_{i1}(t-\tau)$, where τ is the duration time of the triangular pulse) starts to be applied to node D, the transistors M_{2P} and M_{1N} are off, whereas M_{1P} and M_{2N} are switched on, and then the drain currents of M_{1P} and M_{2N} flow through the load R_L as in the previous case but in the opposite direction.

III. Design Criteria

The mask compliance (including adequate margins) requires proper choices for the amplitude (A), the duration time (T_0), and the pulse repetition frequency $(f_{\rm PR})$. In several practical cases, for instance, in the case of radar systems, the minimum $f_{\rm PR}$ is related with the signal-to-noise ratio desired at the output of the receiver [15]. Therefore, a tradeoff between A, T_0, and $f_{\rm PR}$ is required. A reasonable choice could consist of considering the maximum $f_{\rm PR}$ required for the communication system and then deriving the duration time for the best matching with the selectivity of the communication channel (i.e., system bandwidth) and the mask requirements and finally the amplitude of the monocycle pulse. Therefore, in regard to the design of the pulse generator circuit, the amplitude and the duration time of the output sinusoidal-like monocycle represent the specifications. In principle, the duration time directly derives from that of the triangular monocycle pulse. In the practical case, the charge and discharge processes cause some voltage drift, which could however partially be compensated at the design level. Moreover, by considering that the triangular pulse generator previously highlighted can provide a triangular pulse with a maximum amplitude close to $V_{\rm DD}/2$, then the design of the pulse generator requires some effective criteria to accurately accomplish the overall circuit specifications. In particular, from this, it derives that the shaping network demands reliable design criteria. To accomplish this task, first, the general design criteria are summarized. Then, in Section IV, the criteria will then be rearranged for the case of interest (UWB 3.1- to 10.6-GHz applications in 90-nm CMOS).

A. MOSFET Source-Coupled Differential Pair

The trans-characteristic of the source-coupled differential pair in Fig. 4 can be obtained by a large-signal analysis at low frequency (i.e., capacitive effects are neglected) [20], and this is summarized hereinafter for reasons of self-consistency with the following sections (see Sections III-B and IV-A).

This assumes that the current tail is ideal (i.e., $R_{BIAS} \to \infty$), each transistor operates in the saturation region when the differential pair is completely switched (R_D does not limit the drain current), the drain-to-source resistance $(R_{\rm ds})$ of the MOSFETs of the common-source differential pair is large enough to be neglected, and by considering that the drain current (I_d) of each

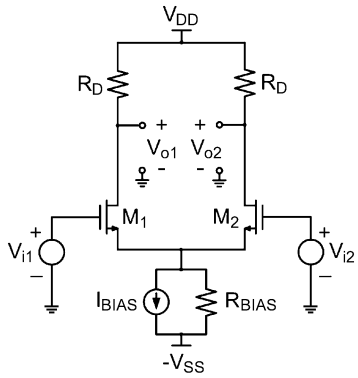

Fig. 4. n-MOSFET source-coupled differential pair.

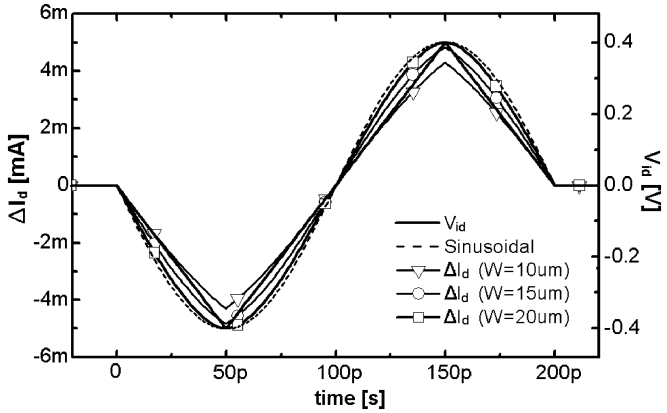

Fig. 5. Output current obtained by (7) of an n-MOSFET differential pair, for several values of W, when an input triangular monocycle pulse $V_{\rm id}$ is applied.

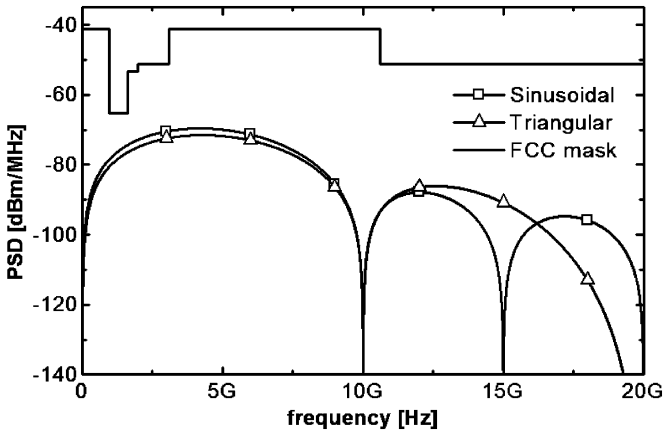

Fig. 6. PSD of a train of triangular monocycle pulses and a train of sinusoidal monocycle pulses with 1-Vpp amplitude and 200-ps duration time each for a pulse repetition frequency ($f_{\rm PR}$) of 1 MHz.

transistor is related to its gate–source voltage by the well-known approximate square law for long-channel n-MOSFETs.

The analysis reported in [20] derives that both M_1 and M_2 operate in the active region if $|V_{\rm id}| \leq \sqrt{2}V_{\rm OV}$, where $V_{\rm OV}$ is the overdrive voltage

$$V_{\rm OV} = (V_{\rm gs} - V_T)|_{V_{\rm id}=0} = \sqrt{\frac{2I_D}{k'(W/L)}} \tag{3}$$

where I_D is equal to $I_{\rm BIAS}/2$, k' is equal to $\mu_n C_{OX}$, W and L are the width and length of the n-MOSFETs, $V_{\rm gs}$ is the gate–source voltage, and V_T is its threshold voltage. Then, $V_{\rm OV}$ is proportional to $\sqrt{I_D}$, and the operating range of the source-coupled pair can be arranged by choosing the bias current and/or the aspect ratio of the MOSFETs.

The output voltage $V_{\rm od} = V_{o1} - V_{o2}$ of the source-coupled differential pair is given by $-\Delta I_d R_D$, where ΔI_d is the difference between the drain currents of M_1 and M_2, which are expressed as follows:

$$\Delta I_d = I_{d1} - I_{d2} = \frac{k'}{2}\frac{W}{L}V_{\rm id}\sqrt{\frac{4I_{\rm BIAS}}{k'(W/L)} - V_{\rm id}^2} \tag{4}$$

which is a nonlinear memoryless I–V transfer characteristic. Finally, if the n-MOSFET source-coupled differential pair is driven by a triangular monocycle pulse with a peak amplitude over the knee of the operating range in the active region, then the output waveform saturates in the proximity of the top of the triangular pulse and the sinusoidal-like output monocycle pulse is obtained.

B. Sinusoidal-Like Monocycle Pulse Generation

Here, our aim is to show how a sinusoidal-like monocycle can be obtained at the output of the n-MOSFET source-coupled differential pair described by the trans-characteristic above [see (4)] when it is driven by a triangular monocycle pulse.

In particular, we consider hereinafter that our target consists of obtaining a 1-V peak-to-peak monocycle pulse with a pulse duration of 200 ps on a 100-Ω load resistance by starting from a triangular monocycle pulse with a 0.8-V peak-to-peak amplitude.

To obtain a 1-V peak-to-peak monocycle pulse on a 100-Ω space resistor (i.e., a peak voltage equal to 0.5 V), a total bias current equal to 5 mA is required. Fig. 5 reports the ΔI_d obtained by (4) for different width W when the triangular monocycle is applied to the input of the differential pair (i.e., $V_{\rm id}$ is the triangular monocycle pulse above) by considering the parameters $C_{\rm ox}$, L, and μ typical for a modern CMOS technology (e.g., 90-nm). Fig. 5 shows that in the case of $W = 20$ μm, ΔI_d reaches the value of the total bias current when $V_{\rm id}$ reaches its peak value (i.e., 0.4 V). Moreover, from Fig. 5, note that the shape of the monocycle obtained at the output of the differential pair is very close to a sinusoidal monocycle pulse.

As for the difference in the frequency domain between the spectra of the triangular and sinusoidal monocycle pulses, the PSDs of a train of triangular monocycle pulses [i.e., before a shaping network described by (4)] and a train of sinusoidal monocycle pulses [i.e., after a shaping network described by (4)] with the same amplitude (1 Vpp) and duration time (200 ps) for a pulse repetition frequency ($f_{\rm PR}$) of 1 MHz are reported in Fig. 6. Note that there is only a slight quantitative and qualitative difference between the spectra of the sinusoidal and triangular monocycle pulses in the range of interest in spite of the significant difference in the time domain. In practice, all the pulse shapes in between (see Fig. 5) the sinusoidal and triangular monocycle pulses have very similar spectra in the band of interest.

IV. UWB Monocycle Pulse Generator in 90-nm CMOS

The parasitic capacitances of MOSFETs introduce memory effects and losses that limit the application at high frequency. In fact, with the same drain current, the shorter the channel length, the faster the switching time of the differential pair. This means that, in principle, a shorter duration time of the pulse can be obtained by using devices with a shorter channel. The shorter the duration time, the higher the frequency range of the relevant part of the spectrum. Here, we deal with the design of a UWB (3.1–10.6 GHz) monocycle pulse generator in 90-nm CMOS technology by ST-Microelectronics. The specifications required are the following: 1) a 1-V peak-to-peak amplitude and 2) a 300-ps duration time. However, as aforementioned, the design criteria reported for long-channel MOSFETs have to be rearranged in the case of short-channel MOSFETs first.

A. Short-Channel MOSFETs Source-Coupled Differential Pair

The equations for the source-coupled differential pair summarized in Section III-A can be rewritten in the case of short-channel transistors.

In detail, for short-channel n-MOSFETs, the drain current (I_d) of each transistor is related to its gate–source voltage by the approximate linear law

$$I_d = \frac{k'}{2} W (V_{\rm gs} - V_T) E_{\rm SAT} \tag{5}$$

where $E_{\rm SAT}$ is the saturation electric field of the velocity of the carriers. In this case, the overdrive voltage is expressed as follows:

$$V_{\rm OV} = \frac{2 I_D}{k' W E_{\rm SAT}} \tag{6}$$

which shows that, unlike the case of the long-channel device [see (3)], $V_{\rm OV}$ is directly proportional to I_D. Then, ΔI_d is expressed as follows:

$$\Delta I_d = I_{d1} - I_{d2} = \frac{k'}{2} W E_{\rm SAT} V_{\rm id}. \tag{7}$$

In contrast with (4), the I–V characteristic for short-channel MOSFETs results in being linear. However, (4) lies the real behavior, and the saturation also occurs in this case. In fact, the currents I_{d1} and I_{d2} versus $V_{\rm id}$ of the source-coupled differential pair for short-channel MOSFETs are shown in Fig. 7. For a comparison, ΔI_d obtained by (4), long-channel ($L = 1\ \mu$m) and short-channel ($L = 90$ nm) MOSFET differential pairs are reported in Fig. 8. Note how (4) represents an excellent approximation of the real trans-characteristic in the case of long channel. Then, due to the saturation occurring in the real trans-characteristic, the design criteria reported in Section III can be extended to the short-channel case. Fig. 9 reports ΔI_d obtained by a short-channel differential pair for several W, whereas it is driven by a triangular monocycle pulse with 0.4-V peak amplitude and 200-ps duration time.

Finally, also in this case, the knee of the operating range in the active region depends on the overdrive voltage of the source-coupled differential pair, which has to be sized in accordance with the amplitude of the output voltage provided by the triangular pulse generator. Note that, due to the linear relationship [see (7)], the simple mathematical approach used for the demonstration in Section III-B fails in this case. However, the least-square method could be used for the demonstration of the sinusoidal-like shaping (see Appendix I). In spite of such a method allowing us to obtain an analytical representation of a given I–V nonlinear trans-characteristic, in this case, we lose the explicit dependence from W, which represents the relevant parameter for the design. Last but not least, as shown in

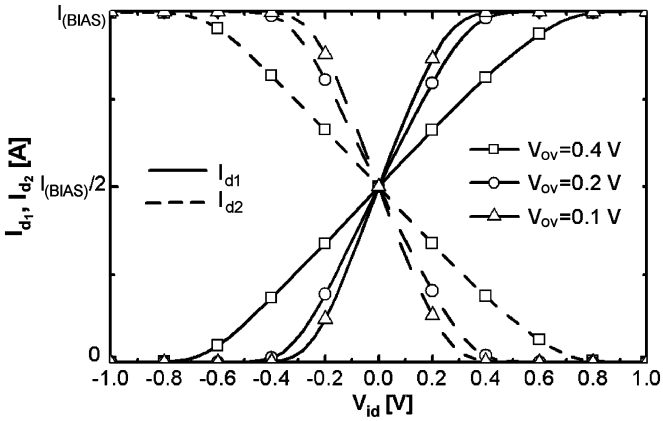

Fig. 7. I_{d1} and I_{d2} versus $V_{\rm id}$ of the n-MOSFET source-coupled pair in 90-nm CMOS by STM (Cadence simulations).

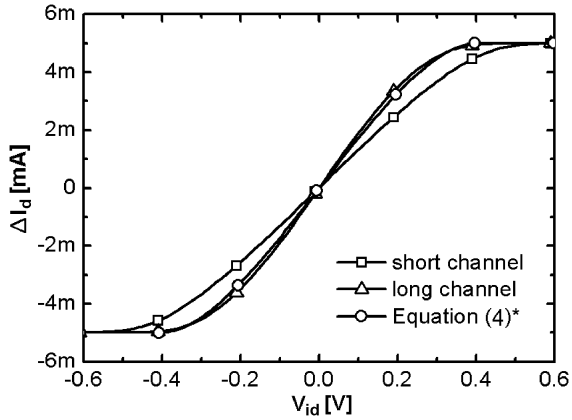

Fig. 8. ΔI_d versus $V_{\rm id}$ obtained by (5), long-channel ($L = 1\,\mu$m) and short-channel ($L = 90$ nm) MOSFET differential pair, for W/L fixed. $^*\Delta I_d$ has been considered equal to $I_{\rm BIAS}$ for $|V_{\rm id}| > 0.4$ V.

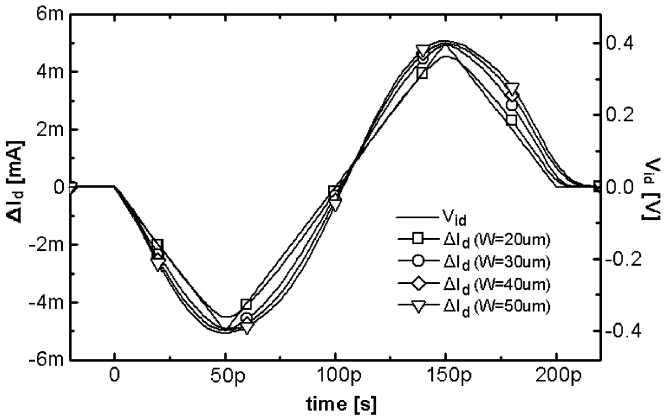

Fig. 9. Output current of a short-channel n-MOSFET differential pair, for several values of W, when an input triangular monocycle pulse $V_{\rm id}(t)$ is applied.

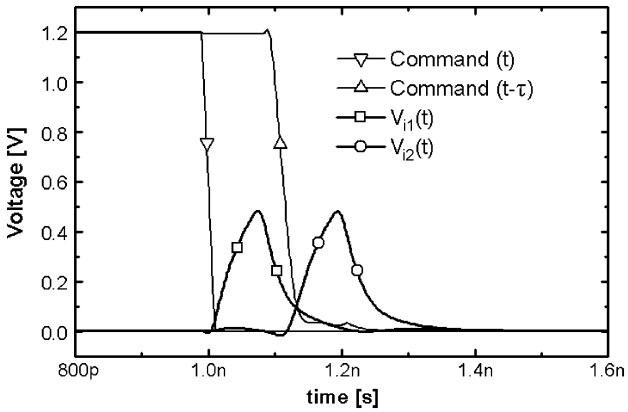

Fig. 10. Triangular pulses at the inputs of the shaping network by postlayout simulations. Note that they are delayed approximately of the triangular pulse time width.

TABLE I
TRIANGULAR PULSE GENERATOR: MOSFET AREA SIZING

Transistor	W [μm]
M_1, M_2, M_3	30
M_4	5
M_5, M_6	8
M_7, M_8	15
M_P	4
M_N	2

Section IV-C, the design aimed at the achievement of a monocycle pulse as much as sinusoidal as possible is largely beyond the scope of this paper, particularly by considering the spectral similarity in 3.1–10.6 GHz (see Fig. 6). Therein, a design approach by means of a computer-aided design tool will be considered, resulting in a more direct and intuitive approach.

B. Design of the Triangular Pulse Generator

In the triangular pulse generator, the comparator has been realized by means of a cascade of two CMOS inverters.

The reference voltage of the comparator is equal to $V_{\rm DD}/2$, which has been obtained by sizing the width of the p-MOSFETs M_P as two times larger than the n-MOSFET's M_N width. The delay (i.e., τ, see Fig. 1) has been implemented by means of a cascade of 12 CMOS inverters (as well as those adopted in the comparator circuit). The propagation time (i.e., τ) of the delay generator is close to 125 ps (i.e., approximately equal to the relevant duration time of each triangular pulse). The two triangular pulses, provided by the two TPGs, at the inputs of the shaping network are shown in Fig. 10.

The maximum value of the amplitude of the triangular pulse is close to $V_{\rm DD}/2$. In particular, the postlayout simulations show that a triangular pulse with an amplitude of 530 mV (open load) can be obtained from a 1.2-V supply voltage. The capacitor $C_{\rm load}$ has been sized to 100 fF for reasons of reliability. The transistor area sizing for the triangular pulse generator is summarized in Table I (the channel length is 90 nm).

C. Design of the Shaping Network

The schematic of the shaping network is shown in Fig. 3. The input voltage of the shaping network is equal to $V_{\rm id}(t) = V_C(t) - V_D(t)$. The trans-characteristic of the shaping network in Fig. 3 is very close to that of the n-MOSFET source-coupled differential pair; in particular, it results in

$$V_{\rm out} = -R_L \Delta I_d = -R_L \frac{k'}{2} W E_{\rm SAT} V_{\rm id} \tag{8}$$

where R_L is the load resistance, ΔI_d is the current into the load, and W is the n-MOSFETs width. It is worth mentioning that the p-MOSFET's width is double of the n-MOSFETs width to compensate the different mobilities of the electrons and holes into the channel and then to reach an almost perfect balance of the trans-characteristic. In the previous sections, we saw that if the large triangular pulse overdrives the shaping network over the saturation knee of the transfer characteristic, then the nonlinear distortion produces a sinusoidal-like monocycle. In particular, the proximity to an ideal sinusoidal monocycle pulse does not represent the first aim of our work, which is mainly related with the opportunity of obtaining a large monocycle pulse. The approximation to the sinusoidal monocycle will be considered as a secondary aspect of the pulse generator design, and this will be scaled down with respect to the design reliability issue, as shown hereinafter as far as the choice of the transistor sizing (i.e., width).

Anyway, if we consider that the load impedance and the input and output voltage swings are the design entries for the accomplishment of the overall circuit specifications, then two parameters have to be sized: 1) the drain current and 2) the channel width of the CMOS transistors.

When the triangular pulse generator drives the shaping network in Fig. 3, the peak value of the triangular pulse (530 mV, obtained by postlayout simulations) is reduced to a value of 480 mV, and the gate voltage of the CMOS transistors is unbalanced, with respect to its dc value, for a maximum value (V_S) close to 440 mV (i.e., due to the capacitive partition). By the knowledge of the peak amplitude of the signal on the gate of the MOSFETs of the shaping network (i.e., the value for which the transistor is completely switched off while the others drain the entire bias current), the overdrive voltage required can be derived as follows:

$$\begin{aligned} V_S \approx 440\ \text{mV} \geq |V_{\rm id}|_{\rm MAX} = 2V_{\rm OV} \\ \Rightarrow V_{\rm OV} \leq \frac{440\ \text{mV}}{2} = 220\ \text{mV}, \end{aligned} \tag{9}$$

The output pulse amplitude is equal to $|V_{\rm od}|_{\rm MAX} = R_L I_{\rm BIAS}$, where R_L represents the antenna load resistance (i.e., 100 Ω). By considering the requirement in terms of pulse amplitude (i.e., 1-V peak-to-peak), then the bias current required can be derived as follows:

$$I_{\rm BIAS} = \frac{|V_{\rm od}|_{\rm MAX}}{R_L} \approx 5\ \text{mA}. \tag{10}$$

Thus, if a monocycle pulse of about 1-V peak-to-peak $(V_{\rm pp})$ is required on a 100-Ω differential antenna, then the drain cur-

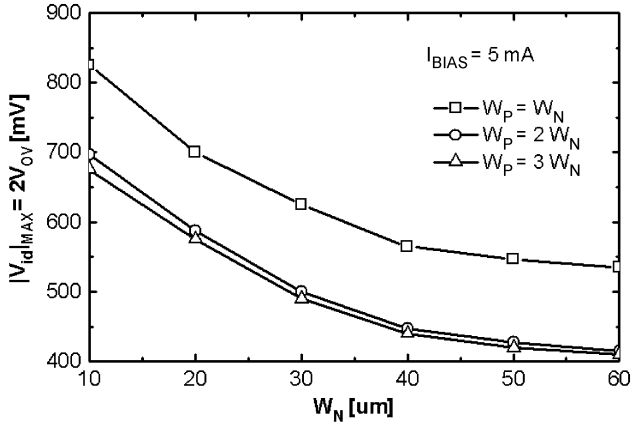

Fig. 11. $|V_{\rm id}|_{\rm MAX}$ versus the n-MOSFET width of the shaping network for several ratios between the p-MOSFET width (W_P) over the n-MOSFET width (W_N).

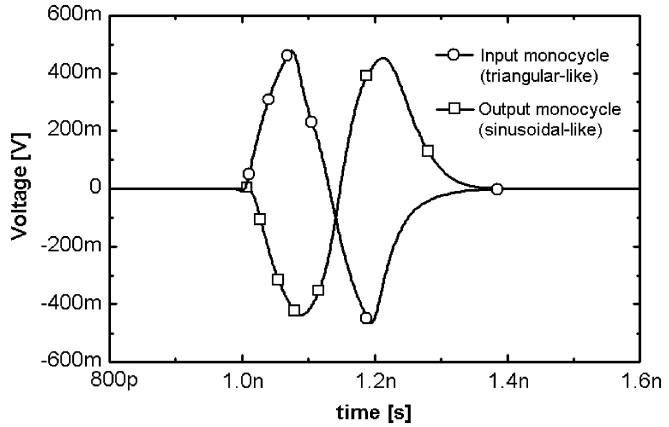

Fig. 12. Input (triangular) and output (sinusoidal-like) monocycles of the shaping network obtained by postlayout simulations (pads inclusive).

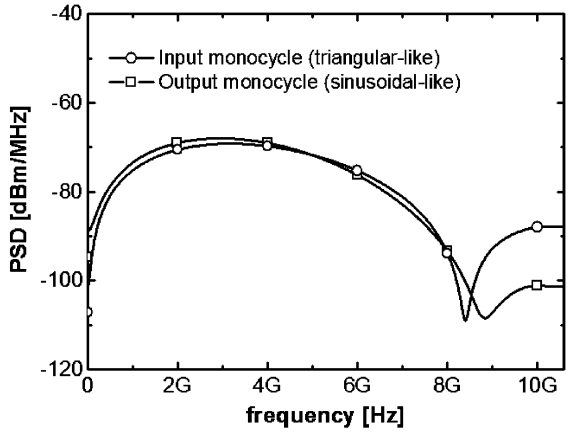

Fig. 13. PSD of trains of monocycle pulses at the input (triangular-like) and output (sinusoidal-like) of the shaping network obtained for a $f_{\rm PR}$ of 1 MHz. For a comparison of the shapes, both PSDs have been evaluated for a standard 50-Ω load.

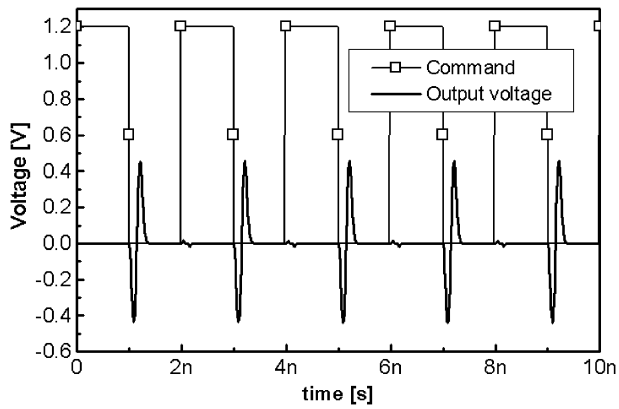

Fig. 14. Sequence of pulses obtained by the application of a square-wave signal *Command*.

rent has to amount to 5 mA. It is worth noting that the current consumption, then the power consumption, depends on the peak-to-peak amplitude required on a specific load resistance. The lower the peak-to-peak amplitude and the higher the load resistance, the lower the power consumption. $|V_{\rm id}|_{\rm MAX}$ is clearly a function of the width of the n-MOSFETs of the shaping network. Since the proximity to the sinusoidal shape can be considered even as a secondary aspect in our design, the choice of W can be carried out by considering the design reliability issue preferably. Fig. 11 reports this dependency for several ratios between the p-MOSFET's width (W_P) over the n-MOSFET's width (W_N).

Note that to have $|V_{\rm id}|_{\rm MAX} \approx 440$ mV, the ratio W_P/W_N must be at least equal to 2 and the width of the n-MOS transistors must be nearly equal to 40 μm. Then, for reasons related with an adequate reliability margin, W_N has been sized to 60 μm and W_P to 120 μm. This choice guarantees that the triangular pulse overdrives the shaping network in spite of the spreading of the process parameters.

The monocycle pulse obtained by postlayout simulations is shown in Fig. 12, which is in accordance with the value predicted in (8). In spite of this choice of W not primarily considering the proximity to the ideal sinusoidal monocycle, we can observe that the monocycle pulse obtained has a satisfactory sinusoidal-like shape. Their spectra are shown in Fig. 13.

The sequence of the pulses obtained, each at the negative edge of the signal *Command*, is shown in Fig. 14. For the sake of clarity, the signal command is obtained by buffering the signal (e.g., provided by a signal generator) through four minimum-size inverters.

As an additional consideration, it is worth noting that both the triangular pulse generator and the shaping network provide monocycle pulses with comparable peak-to-peak amplitude. However, even if they have very similar frequency spectra, only the shaping network is capable of driving the antenna. In other terms, the shaping network allows us to transit from two triangular pulses (one is delayed) to a monocycle pulse—i.e., the differential output signal—and acts also as a regenerative buffer toward the antenna load.

The energy of each monocycle pulse amounts to approximately 0.3 pJ. It is possible to demonstrate that the PSD of a train of such pulses generated with a repetition frequency equal to 1 MHz is compliant with the FCC mask (this is not reported for reasons of space). Moreover, as for the compliance, it is worth mentioning that the mask is referred to the PSD of the power radiated by the antenna. Note that the PSD is always lower than -65.3 dBm/MHz for medical applications [2] (see FCC mask in Fig. 6), which is the lowest value of the FCC mask over the

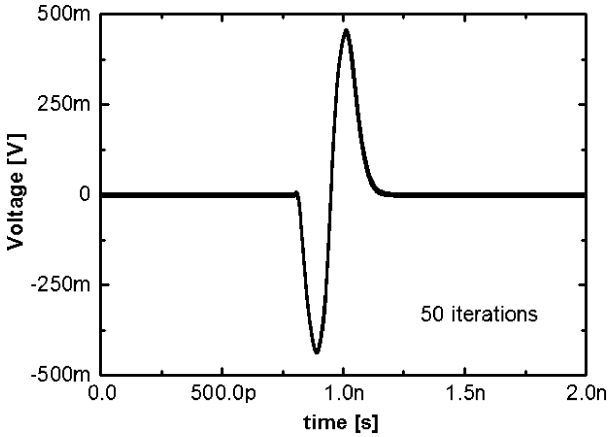

Fig. 15. Output voltages versus time obtained by means of a 50-iterations Monte-Carlo analysis.

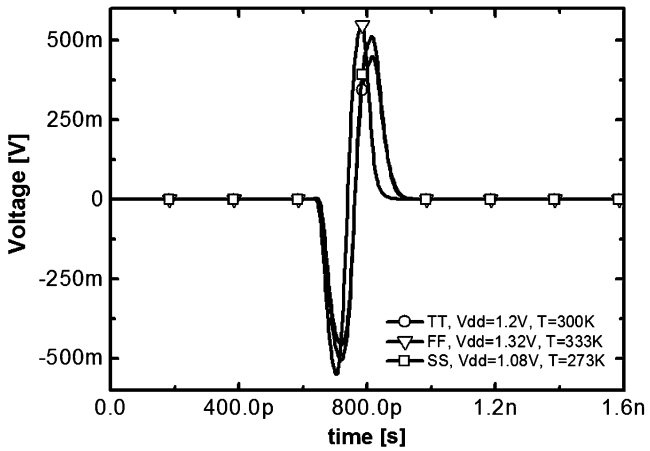

Fig. 16. Output voltages versus time obtained for PVT corner analyses.

frequency spectrum. In practice, the antenna introduces a bandwidth restriction (i.e., filtering), which leads to a larger compliance.

The supply voltage is equal to 1.2 V, and the total power consumption amounts to 19.8 mW (including the biasing circuitry).

Monte-Carlo simulations were carried out to verify the robustness of the circuit to process parameter variations and mismatches. The results are shown in Fig. 15. Note that the results of 50 iterations are very close to each other (the curves are indistinguishable practically), showing the excellent robustness of the design of the novel pulse generator proposed herein. The output pulses obtained for process–voltage–temperature (PVT) corner analyses are reported in Fig. 16.

V. Experimental Results

The test chips have been realized through the multiwafer projects by Circuits Multi-Projets. The test-chip micrograph is shown in Fig. 17. The experimental characterization of the test chip has been carried out by means of on-wafer measurements by exploiting ground–signal–ground–signal–ground (GSGSG) microprobes with a 100-μm pitch by Cascade. The electrostatic-discharge-protected pads (standalone) have shown a characteristic parasitic capacitance of about 240 fF (measured), which is in very good agreement with postlayout simulation results.

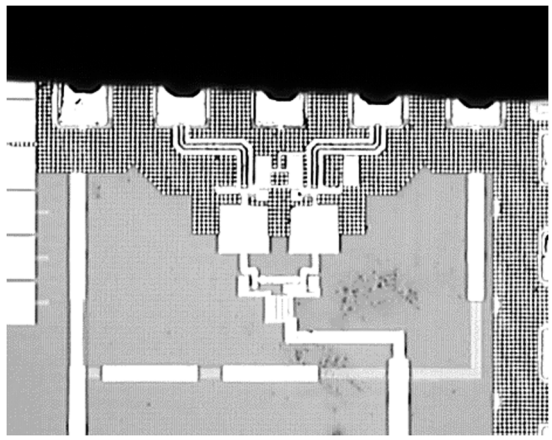

Fig. 17. Die micrograph of the test chip. The total area amounts to approximately 0.25 mm^2.

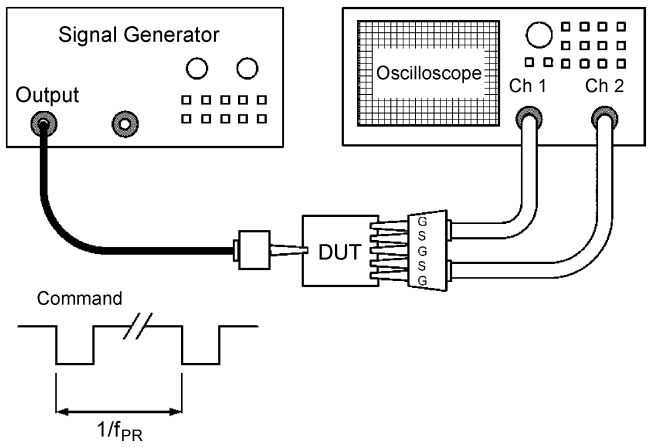

Fig. 18. Scheme of the measurement setup of the pulse generator. The signal *Command* has a period equal to $1/f_{\rm PR}$, where $f_{\rm PR}$ is the pulse repetition frequency.

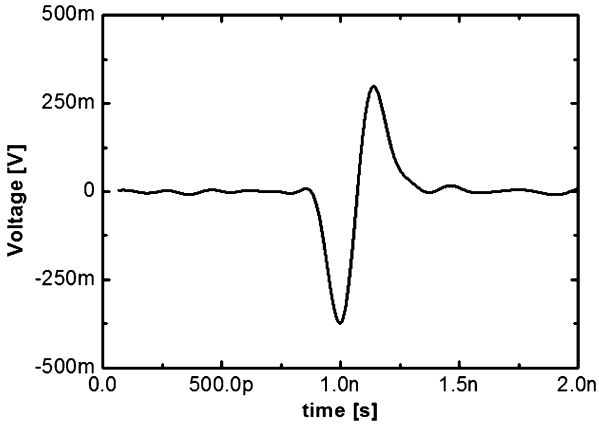

Fig. 19. Monocycle pulse provided by the pulse generator. This has been measured by means of a dual-channel real-time digital oscilloscope (channel 1–channel 2, 50-Ω input impedance each).

The digital command signal, which activates the triangular pulse generator (then, the UWB pulse generator), consists of a square wave with an amplitude equal to 1.2 V and a pulse repetition frequency $(f_{\rm PR})$ from 1 to 10 MHz. This has been provided by a signal generator Agilent 81110A Pattern Generator. The output signal of the pulse generator has been captured on two 50-Ω impedance channels of the Infinium 5485A real-time

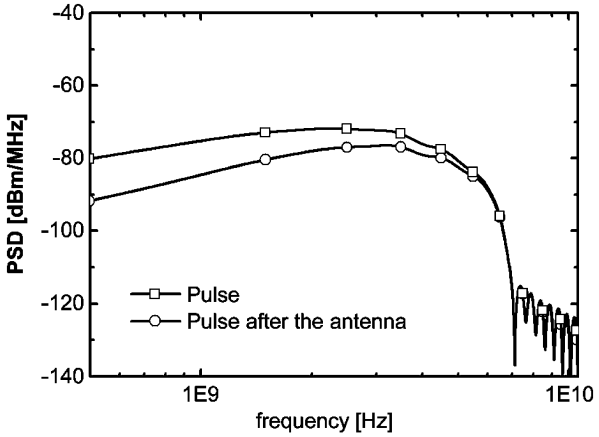

Fig. 20. Spectrum of the measured pulse before and after an ideal UWB antenna filtering (i.e., a first-order bandpass 3.1- to 10.6-GHz Butterworth filter) for a pulse repetition frequency of 1 MHz. The drop of the PSD after 6 GHz is due to the band limit (i.e., 6 GHz) of the oscilloscope.

digital oscilloscope (20 Gs/sec, 6-GHz bandwidth) by Agilent Technologies. The measurement setup is shown in Fig. 18. The pulse provided by the pulse generator is shown in Fig. 19. The overall power consumption amounts to 19.8 mW. Note that the pulse has a peak-to-peak amplitude of about 660 mV and a relevant duration time of about 380 ps. The same performance has been measured on several test chips, confirming definitively the predictions of the Monte-Carlo analyses.

The reduction of the amplitude is due to the attenuation over the frequency range of 1–10 GHz of the cables (0.2–1 dB), the dc blocks (0.2 dB), the microprobes (0.2–0.4 dB), and the connectors (0.2 dB) used to capture the output waveform. If we consider the average attenuation (i.e., 1.3 dB), it means that 660 mV on the oscilloscope approximately corresponds to 900 mV on chip, which is in very good agreement with the postlayout simulation results.

The PSD of the measured pulse, for a pulse repetition frequency $(f_{\rm PR})$ of 1 MHz, is shown in Fig. 20, which also reports the PSD of the sequence of pulses after an ideal UWB antenna filtering (i.e., a first-order bandpass of 3.1- to 10.6-GHz Butterworth filter) directly related with the power radiated.

The voltage efficiency, which is defined as the ratio between the peak-to-peak amplitude of the pulse generated and the supply voltage of the circuit, amounts to

$$\eta_V = \frac{V_{\rm pp}}{V_{\rm DD}} = 55\%. \tag{11}$$

By considering the monocycle approximately equal to a sinusoidal monocycle, the energy of the pulse amounts to

$$E_P = \int_0^{T_0} \frac{V_{\rm out}^2(t)}{R_L} dt \simeq \int_0^{T_0} \frac{V_{\rm MAX}^2}{R_L} \cos^2(\omega_0 t) dt = \frac{V_{\rm MAX}^2 T_0}{2R_L} = 0.21 \text{ pJ} \tag{12}$$

where $V_{\rm MAX}$ is the peak voltage (i.e., 330 mV), R_L is the load resistance (i.e., 100 Ω), and T_0 is the pulse duration (380 ps).

Due to the different applications (e.g., data communication, sensing, etc.) and standard regulations, a more extensive metric is represented by the energy efficiency per pulse [11], [22], which is defined as the ratio between the energy of the pulse generated and the energy consumed by the circuit per single pulse. This is independent from data rate and is expressed as

$$\eta_E = \frac{E_P}{E_C} \tag{13}$$

where

$$E_C = \int_0^{T_0} P_C(t) dt = \int_0^{T_0} \left[P_{\rm DC} + P_d(t)\right] dt \tag{14}$$

where P_C is the overall power consumption, which includes both static $P_{\rm DC}$ (i.e., dc) and dynamic P_d contributions.

In our case, by considering the overall power consumption P_C, we obtain that the energy consumed by the circuit during time T_0 is equal to 8.14 pJ so that the energy efficiency η_E amounts approximately to 2.6%.

TABLE II
SUMMARY OF PERFORMANCE AND COMPARISON WITH THE SOA

Work	T_0 [ps]	V_{PP} [mV]	V_{DD} [V]	P_{DC} [mW]	η_V [%]	η_E [%]	R_L [Ω]
[6]	375	175	1.8	45	9.7	0.08	100
[12]	500	100	1.8	-	-	-	50
[16]	750	1.8	3.3	27.4*	0.06	1.5E-5	100
[17]	280	123	1.8	12.6	6.8	0.003	5K
Our	380	660	1.2	19.8	55	2.6	100

*reference in [21].

The summary of the state of the art (SoA) for the monocycle pulse generators fully integrated on silicon [6], [12], [16], [17], which are based on different approaches and provide Gaussian-like monocycle pulses, is reported in Table II. As for the power consumption, for our work we have considered the overall power consumption, static and dynamic, biasing circuitry inclusive, whereas for all the others we considered the values quoted in the paper, which is in some case referred to dc power consumption only and/or does not include the power consumption of the bias circuitry. Note that this novel solution exhibits the widest pulse peak-to-peak amplitude on standard load impedances (i.e., 660 mV), the highest voltage and energy efficiencies, and one of the shortest duration time.

Finally, note that the design of this pulse generator can be implemented in CMOS or bipolar technologies, and several extensions in terms of functionality (e.g., duration time and polarity control) can be added on the circuit by introducing programmable delays. Moreover, a power-saving strategy can be implemented by turning off the circuitry during the time between two consecutive pulses.

VI. CONCLUSION

A fully integrated monocycle pulse generator of a UWB 3.1- to 10.6-GHz CMOS transmitter for SoaC pulse radar for health-care monitoring has been presented. The circuit provides a 660-mV sinusoidal-like monocycle with a duration time of about 380 ps when it is activated by a negative edge of a low-frequency (i.e., the pulse repetition frequency) command signal (i.e., provided by a microcontroller). The overall power

consumption amounts to 19.8 mW. The operating principle, based on a large-signal approach, has been highlighted, and the design criteria has been derived and discussed accurately. The pulse generator has been implemented in 90-nm CMOS process by ST-Microelectronics, and the experimental characterization of the test chips has been carried out on several samples by means of microprobing on wafer. The experimental results are in very good agreement with postlayout simulations, demonstrating definitively the relevancy of the circuit performance and the design robustness.

Due to the large-signal approach, the comparison with the SoA shows that the new circuit represents the most efficient solution for monocycle pulse generators in the literature, which is in many cases based on a small-signal approach instead.

Appendix I
Application of the Least Squares Method

For a given trans-characteristic obtained by means of simulation or measurement, we can obtain a polynomial approximation as well as the following:

$$\Delta I_d(V_{\rm id}) = aV_{\rm id}^2 + bV_{\rm id} + c. \tag{15}$$

For instance, by the knowledge of 20 points (i.e., samples) of the trans-characteristic, the coefficients a, b, and c can be determined by solving the following linear system:

$$\begin{bmatrix} y_1 \\ y_2 \\ \cdots \\ y_{20} \end{bmatrix} = \begin{bmatrix} x_1^2 & x_1 & 1 \\ x_2^2 & x_2 & 1 \\ & \cdots & \\ x_{20}^2 & x_{20} & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{16}$$

$$X = (A^H A)^{-1} A^H Y \tag{17}$$

where Y is the vector of ΔI_d, A the matrix of $V_{\rm id}$, and H is for Hamilton's operator.

Acknowledgment

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Fabio Zito received the B.Sc., M.Sc., and Ph.D. degrees in electronic engineering from "Mediterranea" University of Reggio Calabria, Reggio Calabria, Italy, in 2003, 2006, and 2010, respectively.

He worked on pulse generator design in 90-nm CMOS technology for ultrawideband (UWB, 3.1–10.6 GHz) cardiopulmonary monitoring with the University of Pisa, Pisa, Italy. He is currently with the Department of Information, Mathematics, Electronics and Transportation (DIMET), "Mediterranea" University of Reggio Calabria. His research interests concern the design of VLSI systems for radio-frequency identification devices.

Domenico Pepe (S'08–M'09) received the B.Sc. and the M.Sc. degrees in electronic engineering from the University of Pisa, Pisa, Italy, in 2002 and 2005, respectively, and the Ph.D. degree from the University of Pisa, in joint supervision with the University of Bordeaux 1, Bordeaux, France, in 2009.

During his Ph.D., he worked on the design of an ultrawideband radar transceiver for cardiopulmonary monitoring in 90-nm CMOS technology. In 2007, he worked in cooperation with the IMS Laboratory, Bordeaux, on the design of 60-GHz LNA in 65-nm CMOS technology. He is currently a Postdoc Research Fellow with Tyndall National Institute, Cork, Ireland. His research interests are in the areas of radio-frequency and millimeter-wave integrated-circuit design.

Domenico Zito (S'00–M'04) received the M.Sc. degree in electronic engineering and the Ph.D. degree in information engineering from the University of Pisa, Pisa, Italy, in 2000 and 2004, respectively.

In the Spring 2001, he was with the RF Advanced Design Center, University of Catania, Catania, Italy, within STMicroelectronics. In 2002, he was with the RFIC Design Team within the Drive Unit, Austriamicrosystems, Graz, Austria. In 2005, he was an Assistant Professor of electronics with the University of Pisa, where from 2003 he held the courses of microwave integrated circuits and electronics for telecommunications (experimental part), and the course of wireless transceiver Design (theory and experimental parts). Since March 2009, he has been with University College Cork (UCC), Cork, Ireland and Tyndall National Institute, Cork, Ireland, as a Stokes Lecturer in microelectronic engineering, in the area of analog, RF, and mixed signals. He is an expert evaluator of EU. He was involved in the European Network of Excellence in Wireless Communications (NEWCom, FP 6th) and several national research projects, and is currently involved in EU projects as WP Leader and Principal Investigator. He is the author of more than 50 papers in peer-reviewed international journals and conference proceedings (six invited papers), one chapter of book, one book (edited) and two patents. His primary interests relate the design of system-on-chip radio-frequency microwave and millimeter-wave front-ends in standard CMOS and Bi-CMOS technologies. They include also CAD tool analyses, circuit modeling and EM design, and experimental characterization.

Dr. Zito is in the Reviewers' Board of several peer-reviewed international journals and is serving as a member and Chair of the Technical Program Committee and special sessions organizer in IEEE international conferences. He received best paper nominations from IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) 2006 and European Microwave Integrated Circuits (EuMIC) 2006 conferences, two awards in Ph.D. Research In Micro-Electronics and Electronics (PRIME) 2005 and 2007 conferences, and the First Price by EU at European Wireless Business Idea Competition "Mario Boella" in December 2005.